74AHC257; 74AHCT257

Quad 2-input multiplexer; 3-state
Rev. 4 — 7 March 2024

Product data sheet

1. General description

The 74AHC257; 74AHCT257 is a quad 2-input multiplexer with 3-state outputs. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

2. Features and benefits

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- · Non-inverting data path
- Wide supply voltage range from 2.0 V to 5.5 V
- Input levels:
 - For 74AHC257: CMOS level
 - For 74AHCT257: TTL level
- Overvoltage tolerant inputs to 5.5 V
- · High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

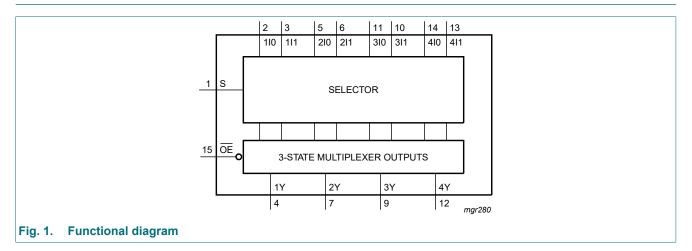
3. Ordering information

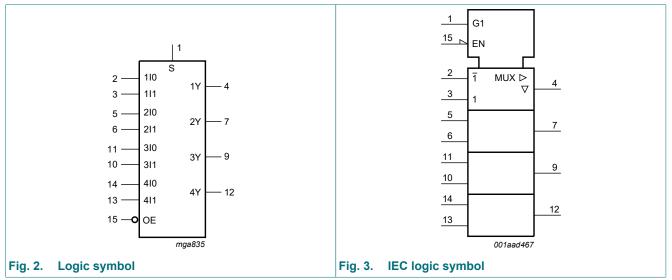
Table 1. Ordering information

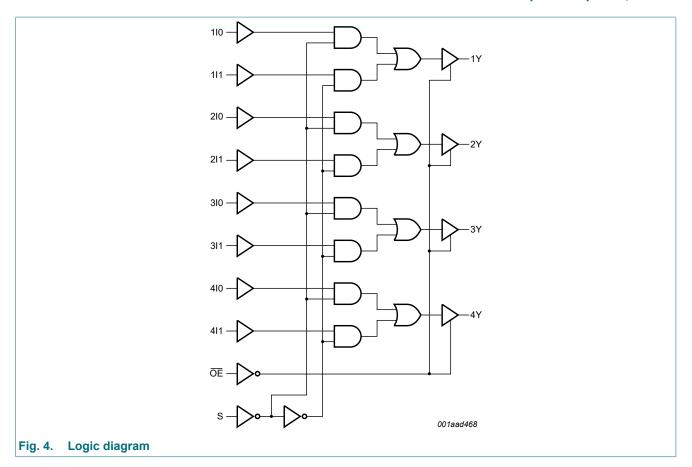
Type number	Package			
	Temperature range	Name	Description	Version
74AHC257D 74AHCT257D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC257PW 74AHCT257PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1



4. Functional diagram

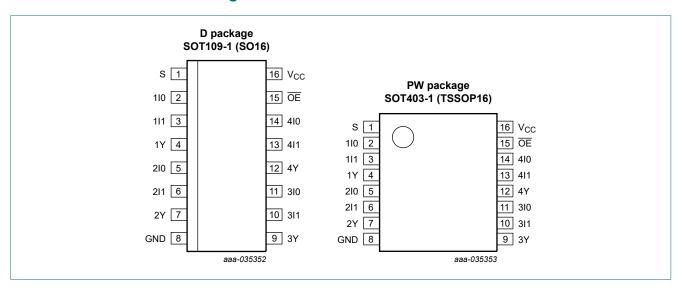






5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
110	2	data input from source 0
111	3	data input from source 1
1Y	4	multiplexer output
210	5	data input from source 0
211	6	data input from source 1
2Y	7	multiplexer output
GND	8	ground (0 V)
3Y	9	multiplexer output
311	10	data input from source 1
310	11	data input from source 0
4Y	12	multiplexer output
411	13	data input from source 1
410	14	data input from source 0
ŌĒ	15	output enable input (active LOW)
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care; \ Z = high-impedance \ OFF-state.$

Control		Input		Output
OE	s	nI0	nl1	nY
Н	Х	Х	X	Z
L	Н	Х	L	L
		X	Н	Н
	L	L	X	L
		Н	X	Н

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V}$ [1]	-20	-	mA
I _{OK}	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$ [1]	-20	+20	mA
Io	output current	$V_O = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-25	+25	mA
I _{CC}	supply current		-	+75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$ [2]	-	500	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
74AHC257	,		<u> </u>			
V _{CC}	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.0 V to 3.6 V	-	-	100	ns/V
		V _{CC} = 4.5 V to 5.5 V	-	-	20	ns/V
74AHCT25	57			1		,
V _{CC}	supply voltage		4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

^[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C. For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C	to +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74AHC2	57							·		
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	I _O = -50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
		$I_O = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level	V _I = V _{IH} or V _{IL}								
	output voltage	I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
l _{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.25	-	±2.5	-	±10.0	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μA
C _I	input capacitance	V _I = V _{CC} or GND	-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF
74AHCT	257									
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	Ι _O = -50 μΑ	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	Ι _Ο = 50 μΑ	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V

Symbol	Parameter	Conditions		25 °C		-40 °C 1	to +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{OZ}		$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.25	-	±2.5	-	±10.0	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μA
ΔI _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V};$ other pins at V_{CC} or GND; $I_O = 0 \text{ A}; V_{CC} = 4.5 \text{ V} \text{ to } 5.5 \text{ V}$	-	-	1.35	-	1.5	-	1.5	mA
Cı	input capacitance	V _I = V _{CC} or GND	-	3	10	-	10	-	10	pF
Co	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions		25 °C		-40 °C 1	to +85 °C	-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
74AHC2	57									
t _{pd}	propagation	nl0, nl1 to nY; see Fig. 5 [2]								
	delay	V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.2	9.3	1.0	11.0	1.0	12.0	ns
		C _L = 50 pF	-	6.0	12.8	1.0	14.5	1.0	16.0	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	2.9	5.9	1.0	7.0	1.0	7.5	ns
		C _L = 50 pF	-	4.2	7.9	1.0	9.0	1.0	11.5	ns
		S to nY; see Fig. 5 [2]								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.2	11.0	1.0	13.0	1.0	14.0	ns
		C _L = 50 pF	-	7.4	14.5	1.0	16.5	1.0	18.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.5	6.8	1.0	8.0	1.0	8.5	ns
		C _L = 50 pF	-	5.0	8.8	1.0	10.0	1.0	12.5	ns
t _{en}	enable time	OE to nY; see Fig. 6 [3]								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.5	10.5	1.0	12.5	1.0	13.5	ns
		C _L = 50 pF	-	6.4	14.0	1.0	16.0	1.0	17.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.2	6.8	1.0	8.0	1.0	8.5	ns
		C _L = 50 pF	-	4.5	8.8	1.0	10.0	1.0	12.5	ns

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	Min	Max	
t _{dis}	disable time	OE to nY; see Fig. 6	[4]								
		V _{CC} = 3.0 V to 3.6 V									
		C _L = 15 pF		-	5.1	9.5	1.0	11.0	1.0	11.5	ns
		C _L = 50 pF		-	7.2	12.0	1.0	13.5	1.0	14.5	ns
		V _{CC} = 4.5 V to 5.5 V									
		C _L = 15 pF		-	3.4	6.5	1.0	7.0	1.0	8.5	ns
		C _L = 50 pF		-	4.9	7.9	1.0	9.0	1.0	9.5	ns
C _{PD}	power dissipation	f_i = 1 MHz; V_I = GND to V_{CC}	[5]								
	capacitance	4 outputs switching via input S		-	45	-	-	-	-	-	pF
		1 output switching via input I		-	15	-	-	-	-	-	pF
74AHCT	257; V _{CC} = 4.5	V to 5.5 V					'		1		
	propagation	nl0, nl1 to nY; see Fig. 5	[2]								
	delay	C _L = 15 pF		-	3.7	6.5	1.0	8.0	1.0	9.0	ns
		C _L = 50 pF		-	4.9	8.5	1.0	10.0	1.0	11.0	ns
		S to nY; see Fig. 5	[2]								
		C _L = 15 pF		-	5.1	9.0	1.0	10.5	1.0	11.5	ns
		C _L = 50 pF		-	6.4	10.5	1.0	12.5	1.0	13.5	ns
t _{en}	enable time	OE to nY; see Fig. 6	[3]								
		C _L = 15 pF		-	3.9	8.0	1.0	9.0	1.0	10.0	ns
		C _L = 50 pF		-	5.1	10.0	1.0	11.0	1.0	12.0	ns
t _{dis}	disable time	OE to nY; see Fig. 6	[4]								
		C _L = 15 pF		-	4.5	7.5	1.0	8.0	1.0	8.5	ns
		C _L = 50 pF		-	6.5	9.5	1.0	10.5	1.0	11.5	ns
C _{PD}	power dissipation	f_i = 1 MHz; V_I = GND to V_{CC}	[5]								
	capacitance	4 outputs switching via input S		-	51	-	-	-	-	-	pF
		1 output switching via input I		-	15	-	-	-	-	-	pF

- Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).
- [2] [3] t_{pd} is the same as t_{PLH} and $t_{\text{PHL}}.$
- t_{en} is the same as t_{PZL} and t_{PZH} .
- [4]
- t_{dis} is the same as t_{PLZ} and t_{PHZ} . C_{PD} is used to determine the dynamic power dissipation (P_D in μ W). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

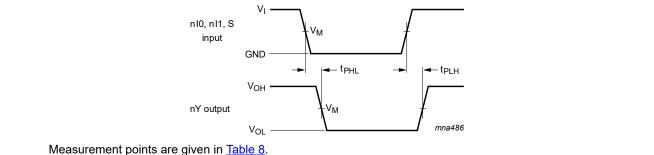
fo = output frequency in MHz;

C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

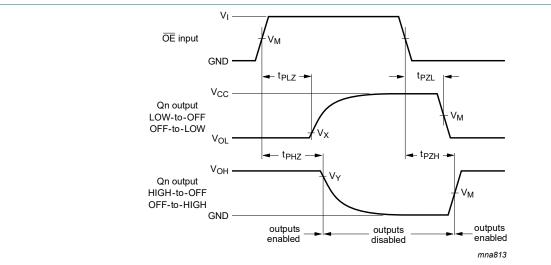
N = number of inputs switching; $\Sigma(C_L \times V_{CC}^{\ 2} \times f_o) = \text{sum of the outputs}.$

10.1. Waveforms and test circuit



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Data inputs and common data select input to output propagation delays



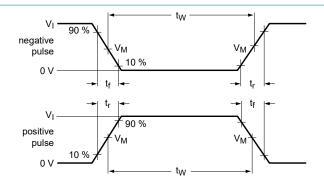
Measurement points are given in Table 8.

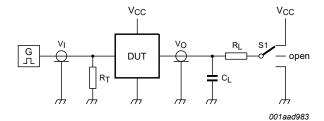
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. **Enable and disable times**

Table 8. Measurement points

Туре	Input	Output				
	V _M	V _M	V _X	V _Y		
74AHC257	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.3 V	V _{OH} - 0.3 V		
74AHCT257	1.5 V	0.5 × V _{CC}	V _{OL} + 0.3 V	V _{OH} - 0.3 V		





Test data is given in Table 9.

Definitions test circuit:

 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = load capacitance including jig and probe capacitance;

R_L = load resistance;

S1 = test selection switch.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Туре	Input		Load		S1 position		
	V _I	t _r , t _f	CL	R _L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
74AHC257	V _{CC}	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}
74AHCT257	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V _{CC}

11. Package outline

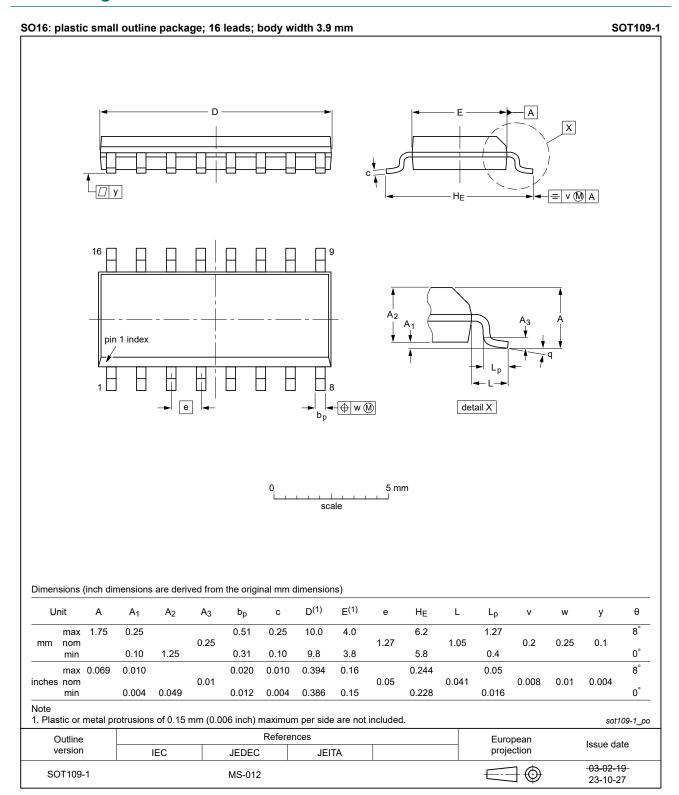


Fig. 8. Package outline SOT109-1 (SO16)

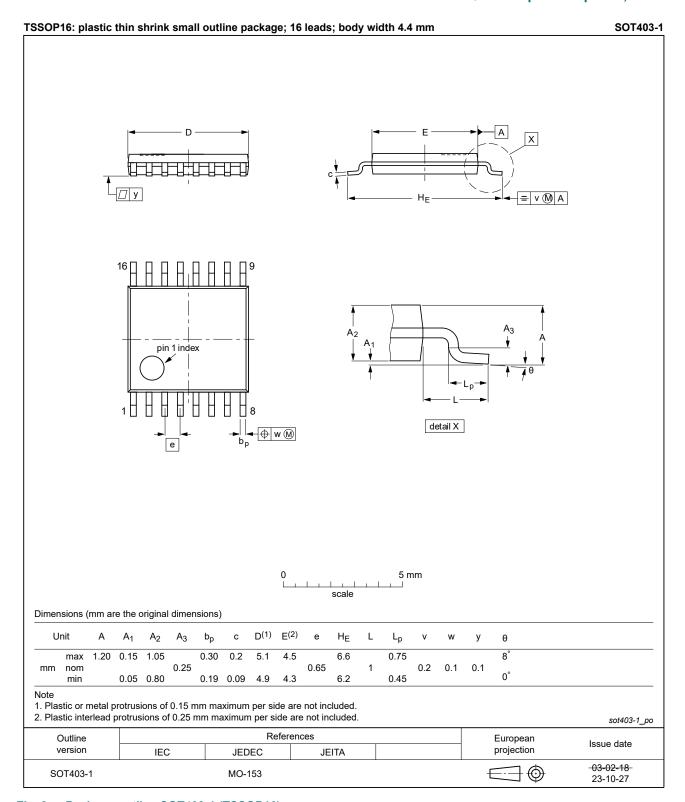


Fig. 9. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description				
CDM	Charged Device Model				
CMOS	mplementary Metal-Oxide Semiconductor				
DUT	Device Under Test				
ESD	ElectroStatic Discharge				
НВМ	Human Body Model				
TTL	Transistor-Transistor Logic				

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74AHC_AHCT257 v.4	20240307	Product data sheet	-	74AHC_AHCT257 v.3		
Modifications:	• <u>Fig. 8, Fig. 9</u> MO-153.	 Fig. 8, Fig. 9: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. 				
74AHC_AHCT257 v.3	20230830	Product data sheet	-	74AHC_AHCT257 v.2		
Modifications:	guidelines of Legal texts Section 1 up Section 2: E	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 updated. Section 2: ESD specification updated according to the latest JEDEC standard. Section 7: Derating values for P_{tot} total power dissipation updated. 				
74AHC_AHCT257 v.2	20080509	Product data sheet	-	74AHC_AHCT257 v.1		
Modifications:	guidelines o Legal texts	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 6: the conditions for input leakage current have been changed. 				
74AHC_AHCT257 v.1	20000403	Product specification	-	-		

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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