## 1. General description

The 74ABT00 is a quad 2-input NAND gate. This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and benefits

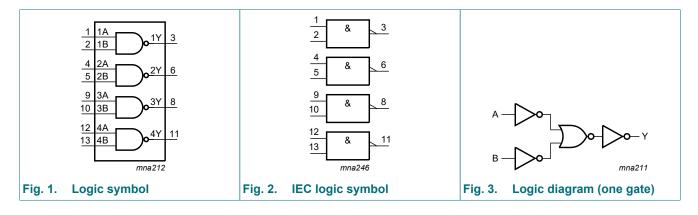
- Supply voltage range from 4.5 V to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- IOFF circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

## 3. Ordering information

#### Table 1. Ordering information

Type number	Package					
	Temperature range	Name	Description	Version		
74ABT00D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<u>SOT108-1</u>		
74ABT00PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<u>SOT402-1</u>		

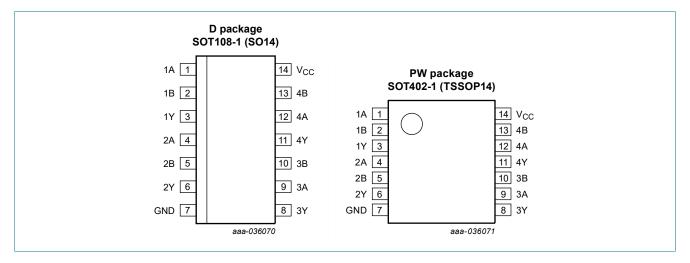
## 4. Functional diagram



# nexperia

## 5. Pinning information

## 5.1. Pinning



## 5.2. Pin description

#### Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

#### Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input	Output	
nA	nB	nY
L	X	Н
X	L	Н
Н	Н	L

## 7. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
VI	input voltage	[1]	-1.2	+7.0	V
Vo	output voltage	output HIGH or LOW [1]	-0.5	+5.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-18	-	mA
I <sub>OK</sub>	output clamping current	V <sub>0</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	output in LOW-state	-	40	mA
Tj	junction temperature		-	150	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 8. Recommended operating conditions

#### Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		4.5	-	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	V
VIH	HIGH-level input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V
I <sub>OH</sub>	HIGH-level output current		-15	-	-	mA
I <sub>OL</sub>	LOW-level output current		-	-	20	mA
Δt/ΔV	input transition rise and fall rate		0	-	5	ns/V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C

## 9. Static characteristics

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C		Unit
			Min	Тур	Max	Min	Max	
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-1.2	-0.9	-	-1.2	-	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = -15 mA; V <sub>I</sub> = <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9	-	2.5	-	V
V <sub>OL</sub>	LOW-level output voltage	$V_{CC}$ = 4.5 V; $I_{OL}$ = 20 mA; $V_I$ = $V_{IL}$ or $V_{IH}$	-	0.35	0.5	-	0.5	V
I	input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	-	±0.01	±1.0	-	±1.0	μA
I <sub>OFF</sub>	power-off leakage current	$V_{CC} = 0 \text{ V}; \text{ V}_1 \text{ or } \text{V}_0 \le 4.5 \text{ V}$	-	±5.0	±100	-	±100	μA
I <sub>CEX</sub>	output high leakage current	HIGH-state; $V_0$ = 5.5 V; $V_{CC}$ = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	5.0	50	-	50	μA
lo	output current	$V_{CC} = 5.5 \text{ V}; V_0 = 2.5 \text{ V}$ [1]	-50	-75	-180	-50	-180	mA
I <sub>CC</sub>	supply current	$V_{CC}$ = 5.5 V; $V_{I}$ = GND or $V_{CC}$	-	2	50	-	50	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; $V_{CC} = 5.5 V$ ; [2] one input at 3.4 V; other inputs at $V_{CC}$ or GND	-	0.25	500	-	500	μA
CI	input capacitance	$V_{I} = 0 V \text{ or } V_{CC}$	-	3	-	-	-	pF

[1] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[2] This is the increase in supply current for each input at 3.4 V.

## **10.** Dynamic characteristics

## Table 7. Dynamic characteristics

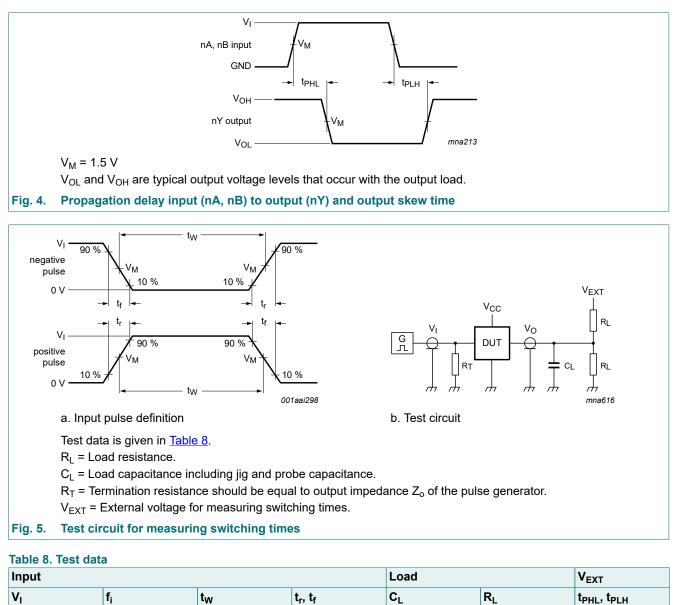
GND = 0 V; for test circuit, see Fig. 5.

Symbol	Parameter	Conditions			-40 °C to +85 °C; V <sub>CC</sub> = 5.0 V ± 0.5 V		Unit	
			Min	Тур	Max	Min	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	nA, nB to nY; see <u>Fig. 4</u>	1.0	2.5	3.6	1.0	4.1	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nA, nB to nY; see <u>Fig. 4</u>	1.0	2.0	2.8	1.0	3.4	ns
t <sub>sk(o)</sub>	output skew time	[1]	-	0.4	0.5	-	0.5	ns

[1] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

## **Quad 2-input NAND gate**

## 10.1. Waveforms and test circuit



1 MHz

500 ns

3.0 V

74ABT00

≤ 2.5 ns

50 pF

500 Ω

open

## 11. Package outline

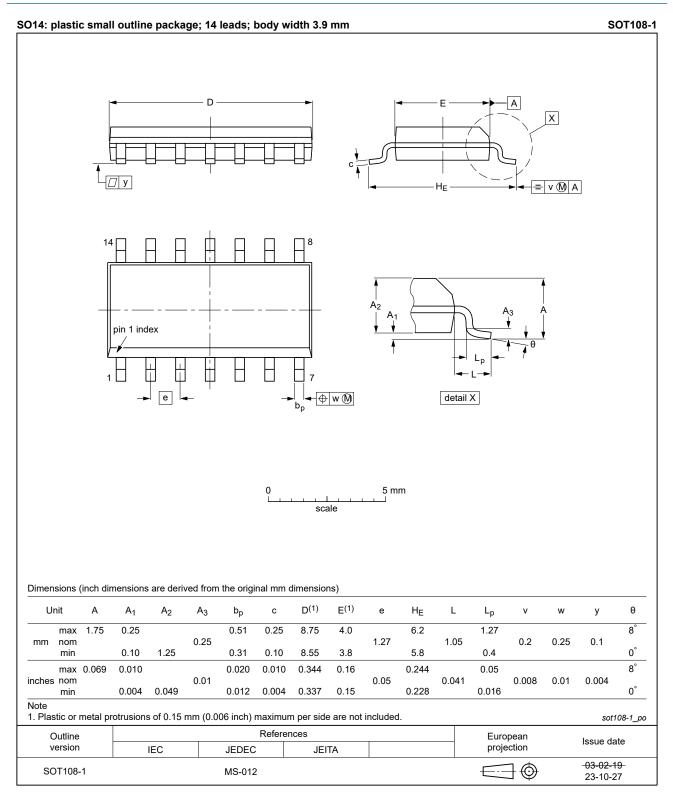


Fig. 6. Package outline SOT108-1 (SO14)

## 74ABT00

## **Quad 2-input NAND gate**

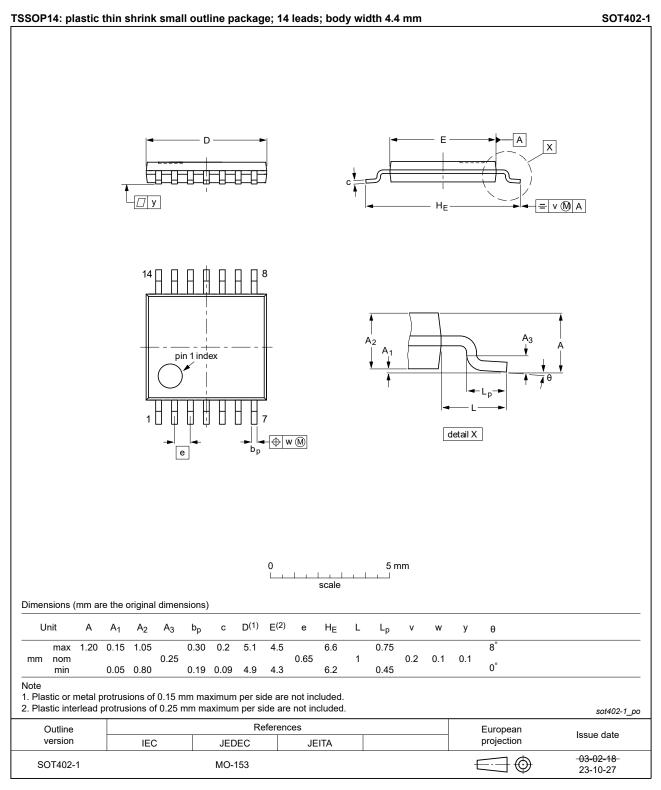


Fig. 7. Package outline SOT402-1 (TSSOP14)

# 12. Abbreviations

Table 9. Abbreviation	Table 9. Abbreviations				
Acronym	Description				
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor				
CDM	Charged Device Model				
DUT	Device Under Test				
ESD	ElectroStatic Discharge				
HBM	Human Body Model				
TTL	Transistor-Transistor Logic				

# 13. Revision history

#### Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74ABT00 v.5.1	20240118	Product data sheet	-	74ABT00 v.4		
Modifications:		<ul> <li><u>Section 2</u>: ESD specification updated according to the latest JEDEC standard.</li> <li><u>Fig. 6</u>, <u>Fig. 7</u>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 a MO-153.</li> </ul>				
74ABT00 v.4	20201005	Product data sheet	-	74ABT00 v.3		
Modifications:	guidelines of Legal texts <ul> <li><u>Section 1</u> a</li> </ul>	of this data sheet has been of Nexperia. have been adapted to the nd <u>Section 2</u> updated. er 74ABT00DB (SOT337-1	new company nar	ne where appropriate.		
74ABT00 v.3	20160811	Product data sheet	-	74ABT00 v.2		
Modifications:	guidelines o	of this data sheet has beer of NXP Semiconductors. have been adapted to the	C C	mply with the new identity ne where appropriate.		
74ABT00 v.2	19950918	Product specification	-	-		

#### Quad 2-input NAND gate

## 14. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
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