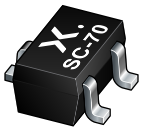

2N7002AKW-Q

60 V, N-channel Trench MOSFET

11 January 2024 Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT323 (SC70) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Extended temperature range T_j = 175 °C
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	60	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	V_{GS} = 10 V; T_{amb} = 25 °C	[1]	-	-	220	mA
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 100 mA; T_j = 25 °C		-	2.2	3	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2.

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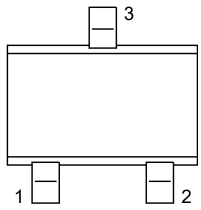
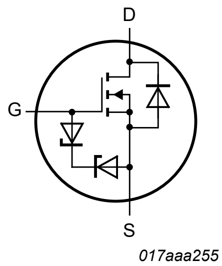
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SC-70 (SOT323)	
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
2N7002AKW-Q	SC-70	plastic, surface-mounted package; 3 leads; 1.3 mm pitch; 2 mm x 1.25 mm x 0.95 mm body	SOT323

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
2N7002AKW-Q	6M%

[1] % = placeholder for manufacturing site code

8. Limiting values

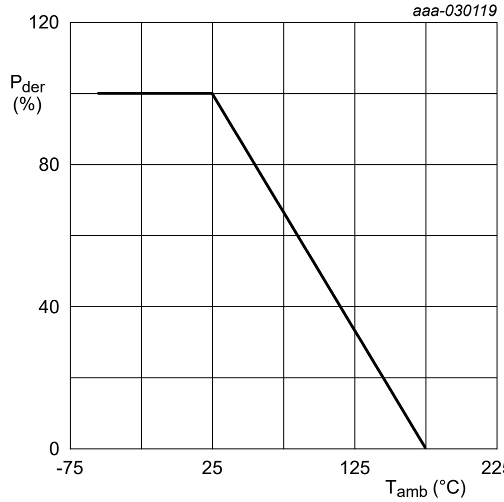
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	60	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{amb} = 25 °C	[1]	-	220	mA
		V_{GS} = 10 V; T_{amb} = 100 °C	[1]	-	160	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \leq$ 10 µs		-	1.8	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	270	mW
			[1]	-	310	mW
		T_{sp} = 25 °C		-	1.3	W
T_j	junction temperature			-55	175	°C
T_{amb}	ambient temperature			-55	175	°C
T_{stg}	storage temperature			-65	175	°C
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	210	mA
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM		-	500	V
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(init)}$ = 25 °C; I_D = 20 mA; DUT in avalanche (unclamped)		-	6.6	mJ

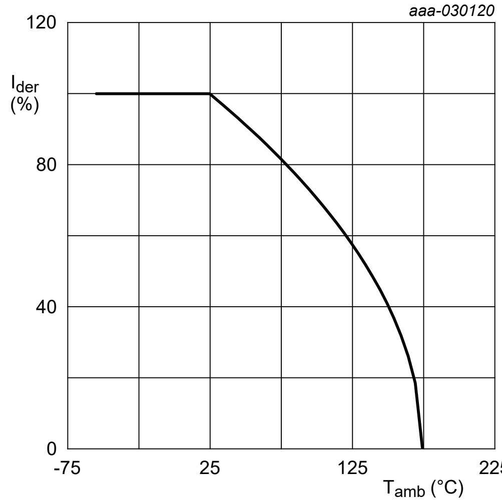
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig. 1. Normalized total power dissipation as a function of ambient temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig. 2. Normalized continuous drain current as a function of ambient temperature

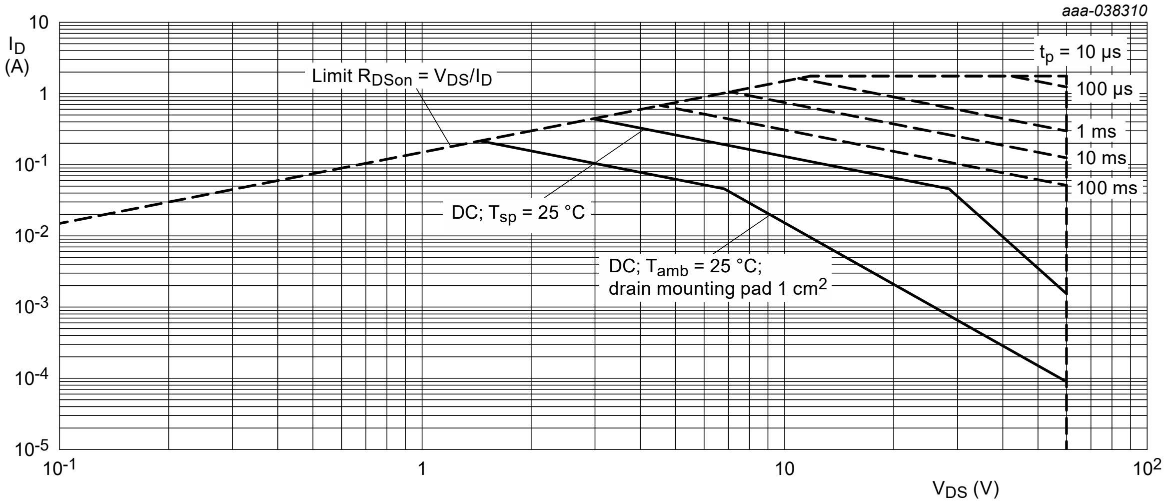


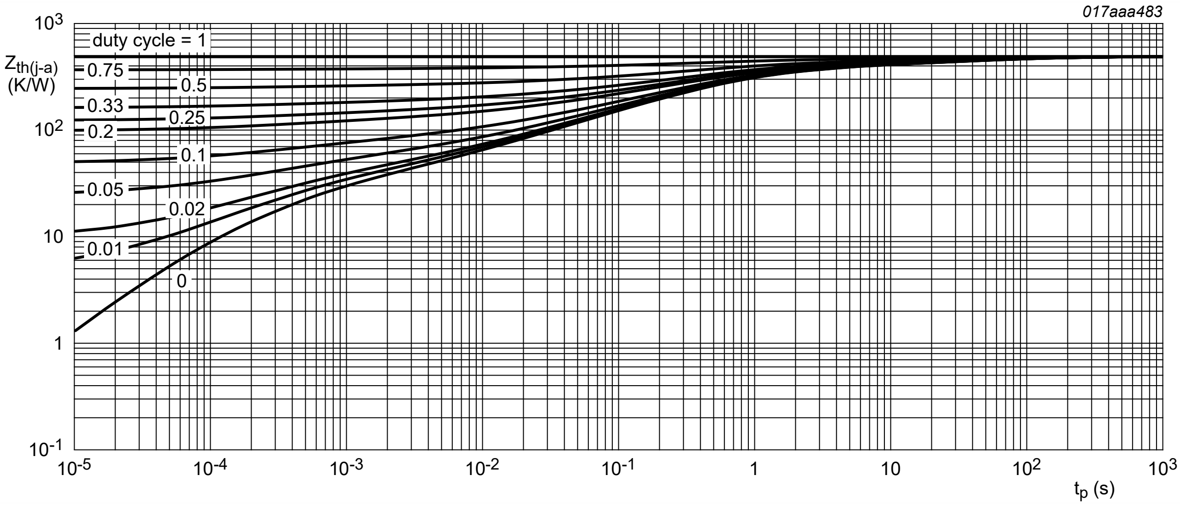
Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

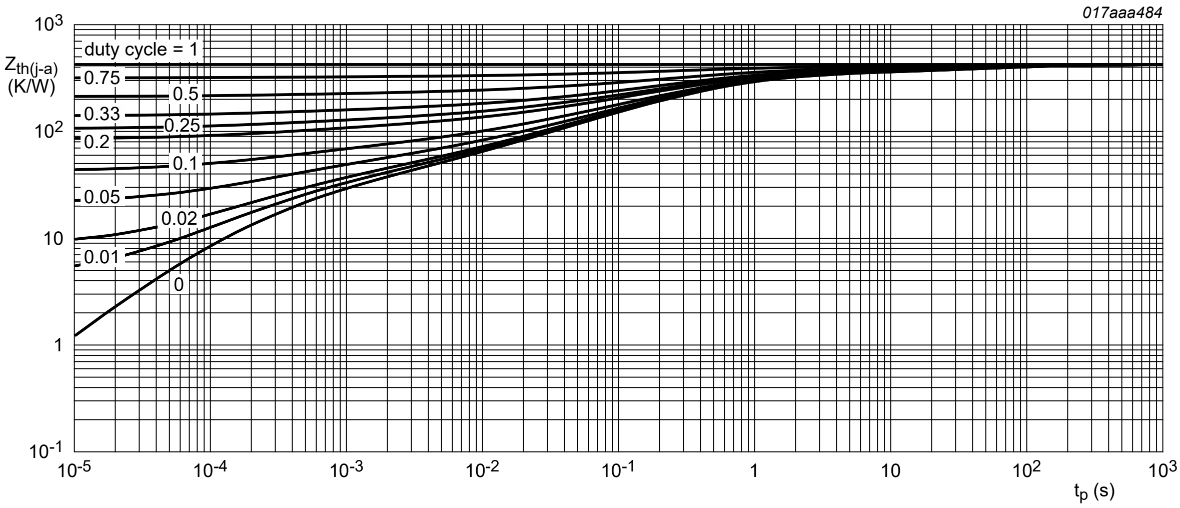
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	485	560	K/W
			[2]	-	420	480	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	98	115	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2.



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



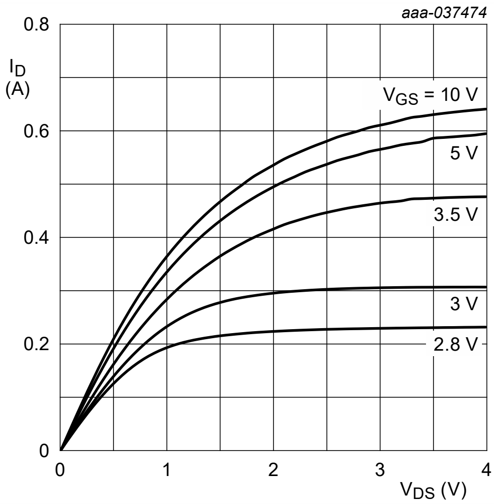
FR4 PCB, mounting pad for drain 1 cm^2

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

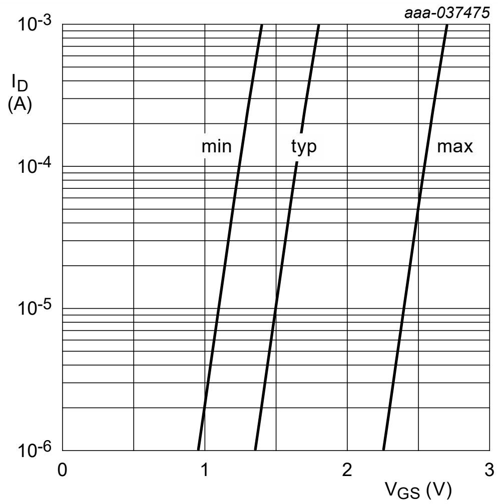
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		60	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 250 µA; V_{DS} = V_{GS}; T_j = 25 °C		1.3	1.7	2.6	V
I_{DSS}	drain leakage current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C		-	-	500	nA
		V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 °C		-	-	5	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	10	µA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-10	µA
		V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-1	µA
		V_{GS} = 5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	500	nA
		V_{GS} = -5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-500	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 100 mA; T_j = 25 °C		-	2.2	3	Ω
		V_{GS} = 10 V; I_D = 100 mA; T_j = 175 °C		-	4.7	6.7	Ω
		V_{GS} = 5 V; I_D = 50 mA; T_j = 25 °C		-	2.5	3.6	Ω
g_{fs}	forward transconductance	V_{DS} = 5 V; I_D = 100 mA; T_j = 25 °C		-	0.3	-	S
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = 30 V; I_D = 100 mA; V_{GS} = 10 V; T_j = 25 °C		-	0.21	0.315	nC
Q_{GS}	gate-source charge			-	0.022	-	nC
Q_{GD}	gate-drain charge			-	0.051	-	nC
C_{iss}	input capacitance	V_{DS} = 30 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	9.2	-	pF
C_{oss}	output capacitance			-	1.6	-	pF
C_{rss}	reverse transfer capacitance			-	0.9	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; I_D = 100 mA; V_{GS} = 10 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	1	-	ns
t_r	rise time			-	1	-	ns
$t_{d(off)}$	turn-off delay time			-	2	-	ns
t_f	fall time			-	6	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 210 mA; V_{GS} = 0 V; T_j = 25 °C		-	1	1.6	V
t_{rr}	reverse recovery time	I_S = 210 mA; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C		-	7	-	ns
Q_r	recovered charge			-	1	-	nC



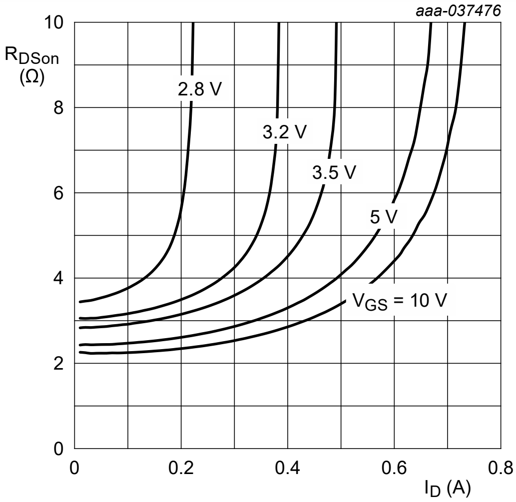
T_j = 25 °C

Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values



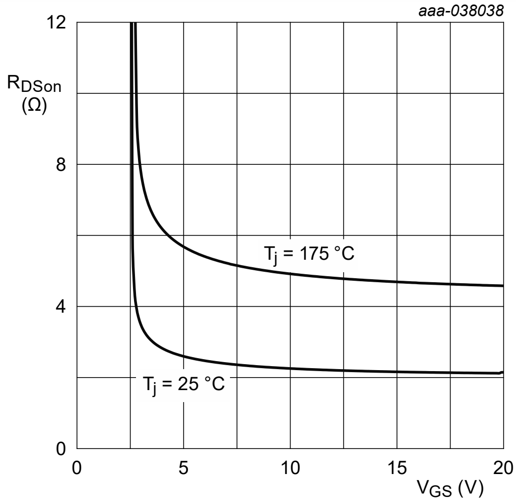
V_{DS} = 5 V; T_j = 25 °C

Fig. 7. Sub-threshold drain current as a function of gate-source voltage



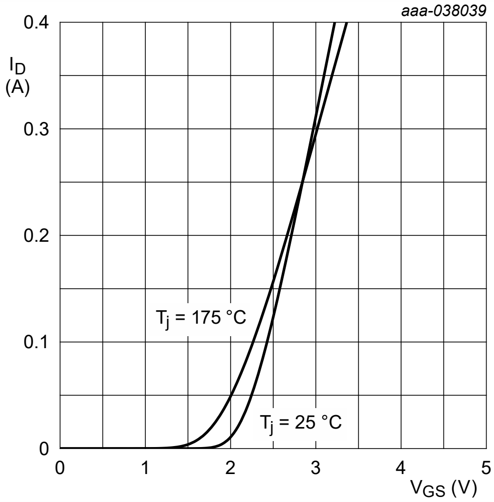
T_j = 25 °C

Fig. 8. Drain-source on-state resistance as a function of drain current; typical values



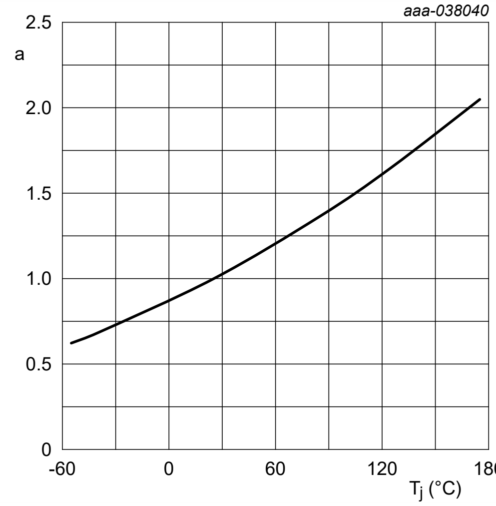
I_D = 200 mA

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



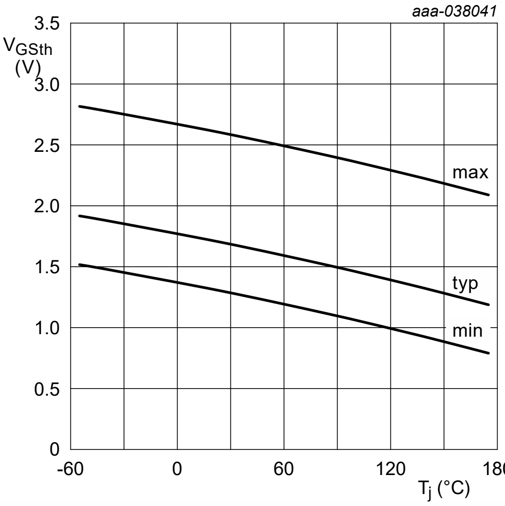
V_{DS} = 9 V

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



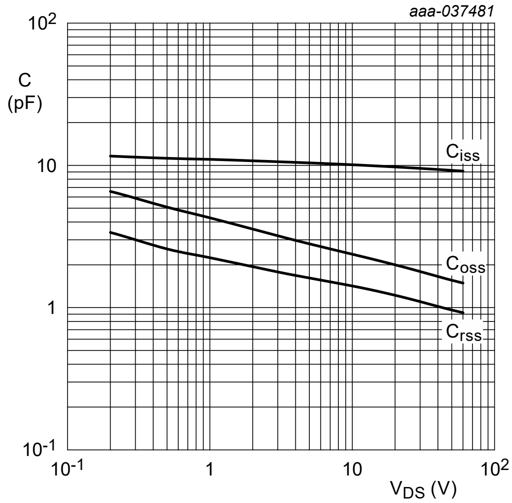
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



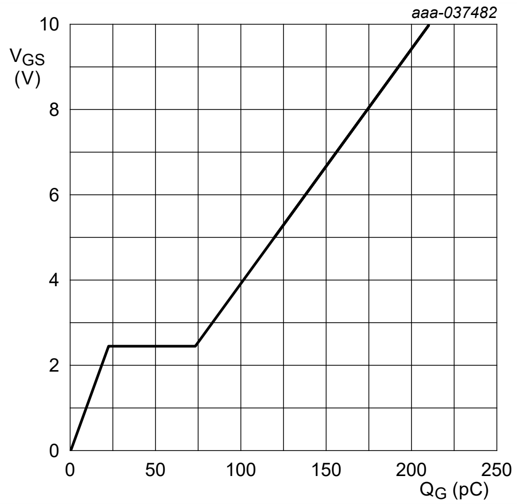
I_D = 250 µA; V_{DS} = V_{GS}

Fig. 12. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = 0.1 A; V_{DS} = 30 V; T_j = 25 °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

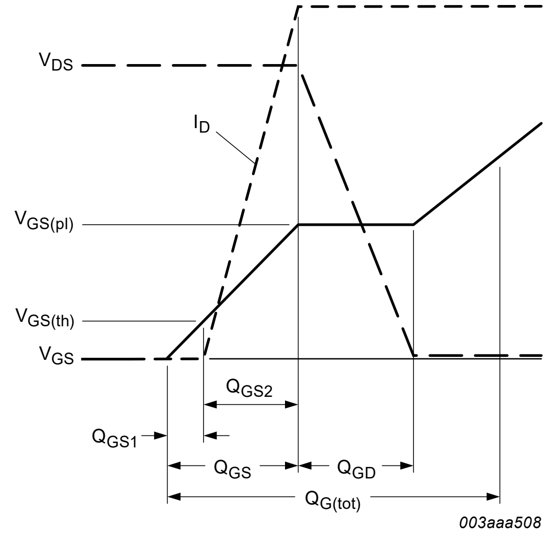
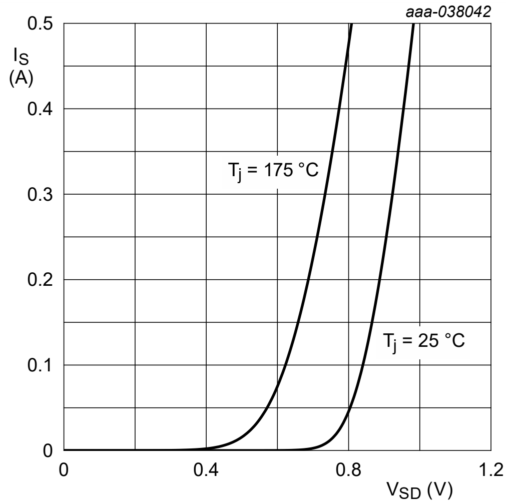


Fig. 15. Gate charge waveform definitions



V_{GS} = 0 V

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

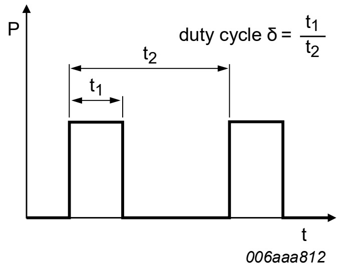


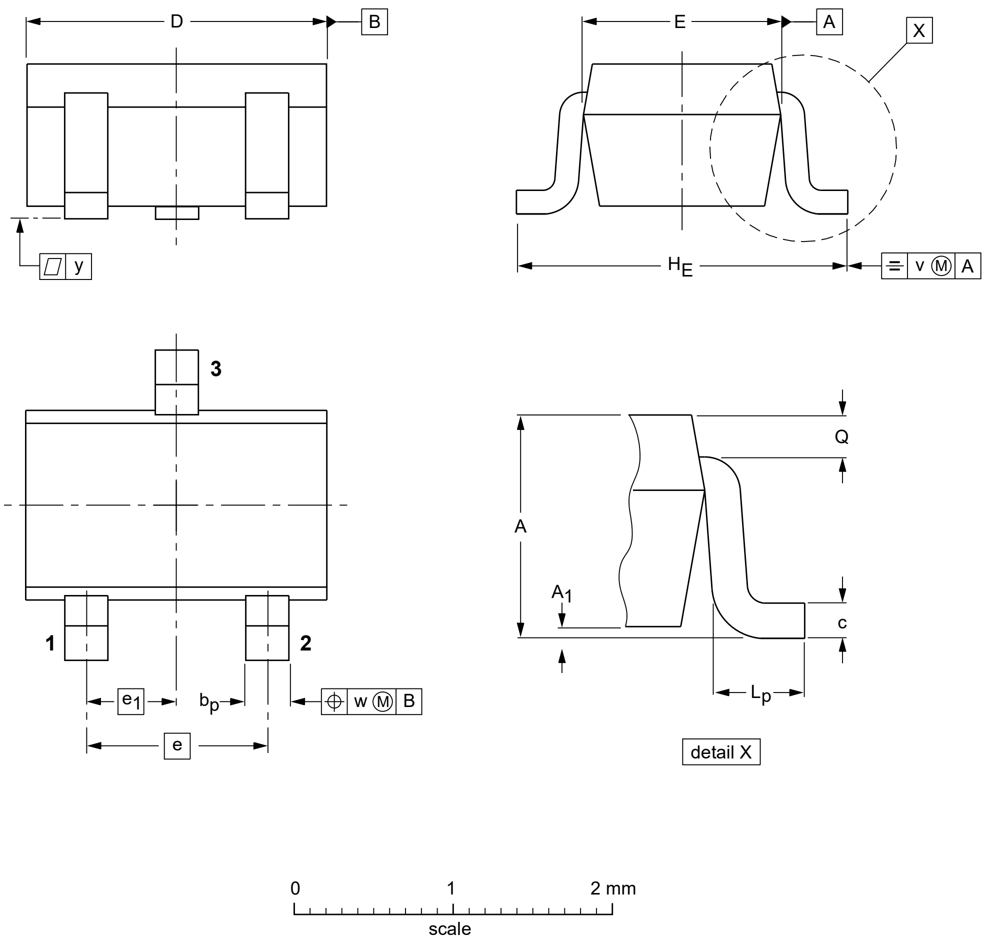
Fig. 17. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

Plastic surface-mounted package; 3 leads **SOT323**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT323			SC-70			~~04-11-04~~ 06-03-16

Fig. 18. Package outline SC-70 (SOT323)

13. Soldering

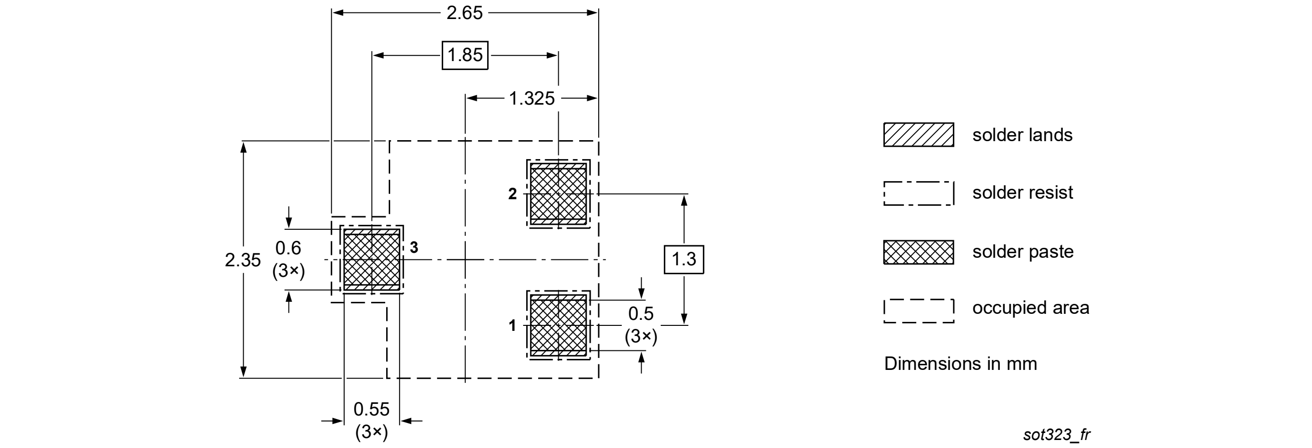


Fig. 19. Reflow soldering footprint for SC-70 (SOT323)

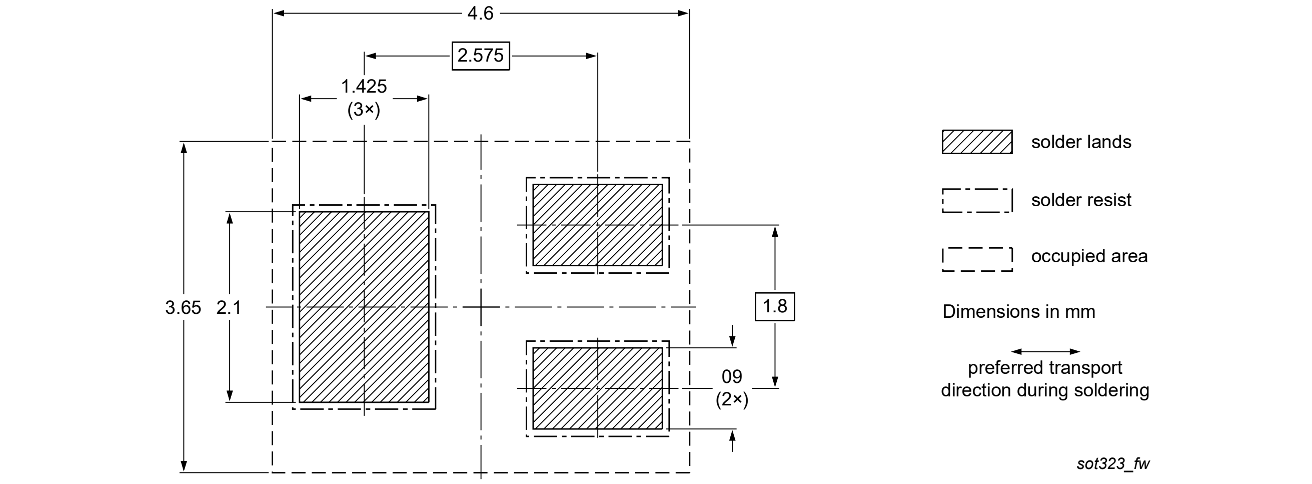


Fig. 20. Wave soldering footprint for SC-70 (SOT323)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
2N7002AKW-Q v.1	20240111	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 11 January 2024