



2N7002AKS-Q

60 V, dual N-channel Trench MOSFET

16 February 2024

Product data sheet

1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Extended temperature range $T_j = 175\text{ °C}$
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

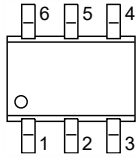
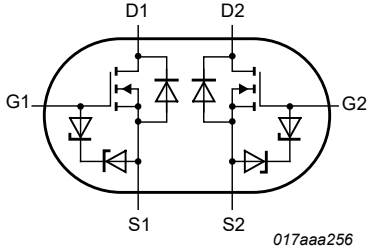
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	220	mA
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 100\text{ mA}; T_j = 25\text{ °C}$	-	2.2	3	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2 .

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source 1	 <p>TSSOP6 (SOT363)</p>	 <p>017aaa256</p>
2	G1	gate 1		
3	D2	drain 2		
4	S2	source 2		
5	G2	gate 2		
6	D1	drain 1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
2N7002AKS-Q	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
2N7002AKS-Q	J2%

[1] % = placeholder for manufacturing site code

8. Limiting values

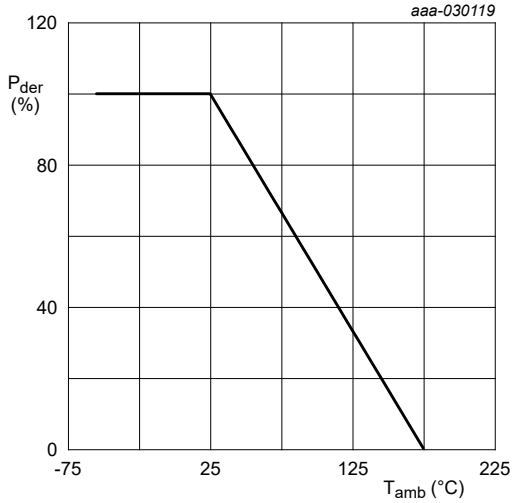
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	60	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	220	mA
		$V_{GS} = 10\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	160	mA
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$		-	1.8	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	270	mW
			[1]	-	310	mW
		$T_{sp} = 25\text{ °C}$		-	1.3	W
Per device						
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	405	mW
T_j	junction temperature			-55	175	°C
T_{amb}	ambient temperature			-55	175	°C
T_{stg}	storage temperature			-65	175	°C
Source Drain Diode (per transistor)						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	210	mA
ESD maximum rating (per transistor)						
V_{ESD}	electrostatic discharge voltage	HBM		-	500	V
Avalanche ruggedness (per transistor)						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(\text{init})} = 25\text{ °C}; I_D = 20\text{ mA};$ DUT in avalanche (unclamped)		-	6.6	mJ

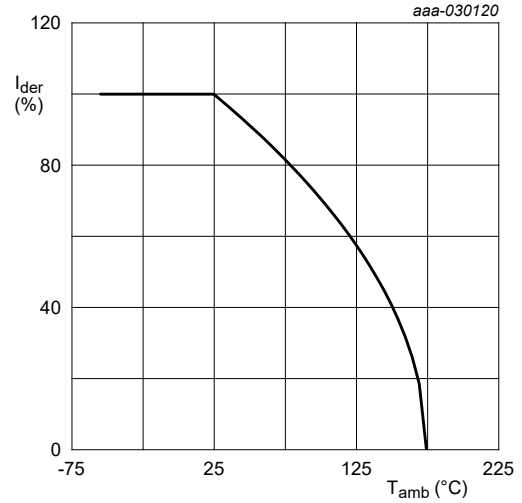
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2 .

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$

Fig. 1. Normalized total power dissipation as a function of ambient temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

Fig. 2. Normalized continuous drain current as a function of ambient temperature

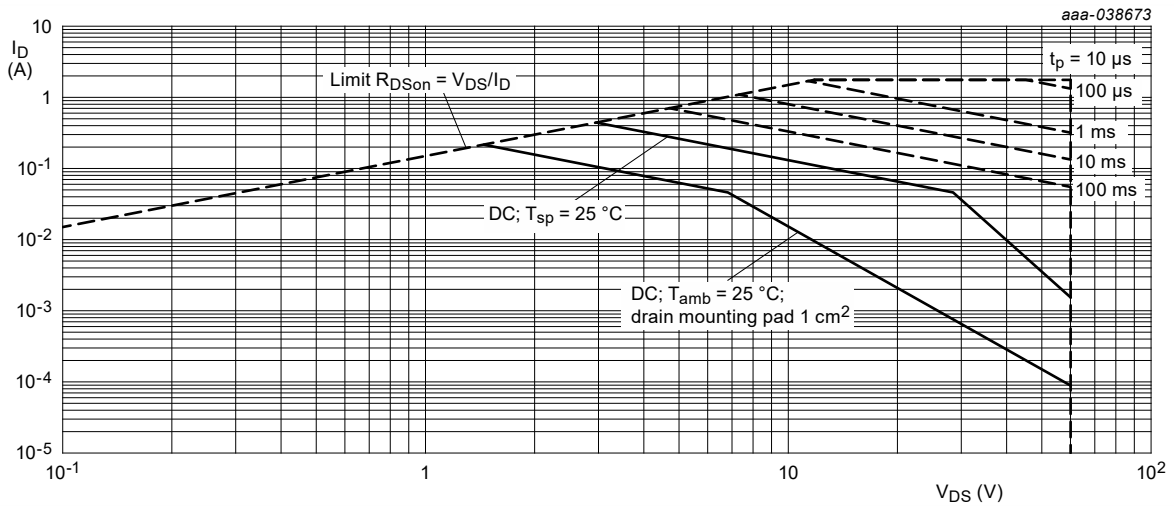


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	375	K/W
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	500	560	K/W
			[2]	-	450	480	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	98	115	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

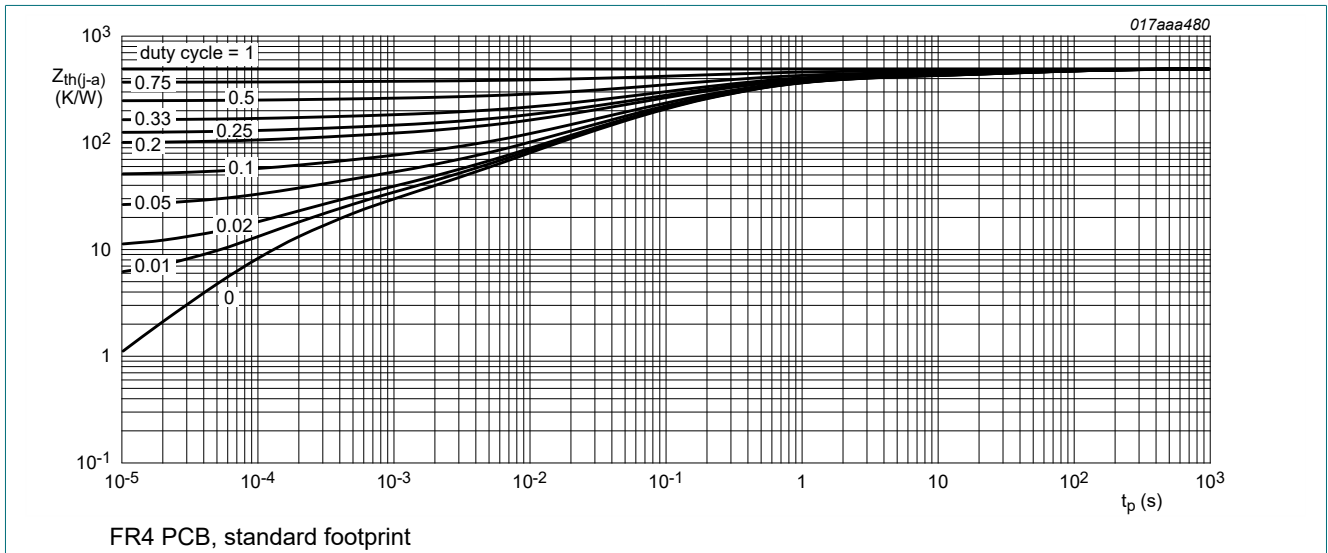


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

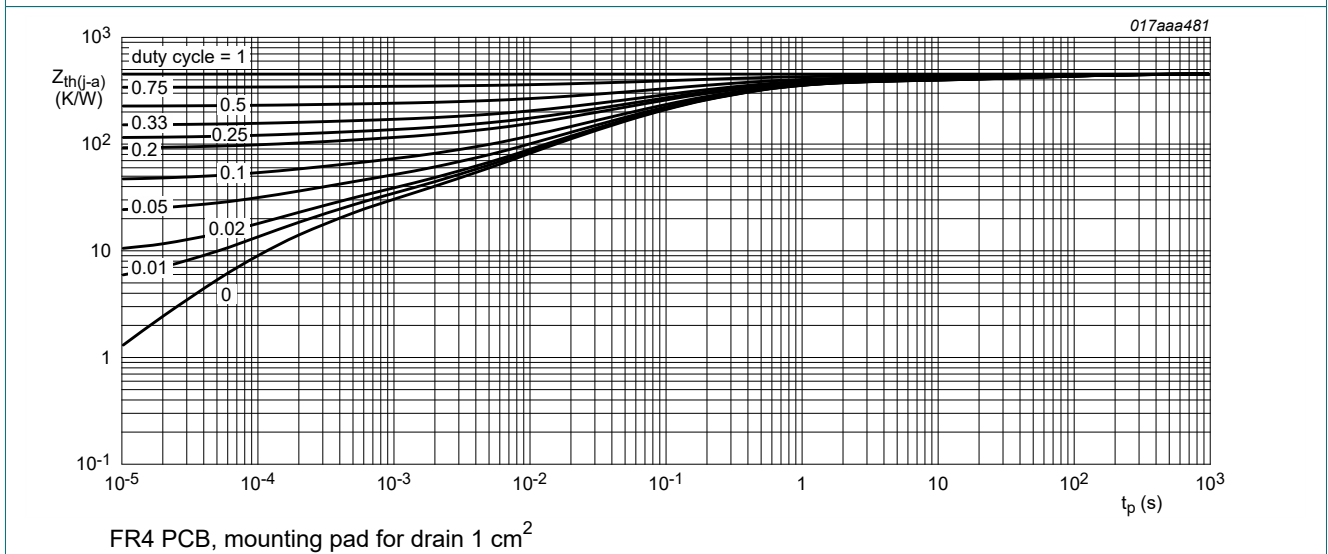


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.3	1.7	2.6	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	500	nA
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$	-	-	5	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-10	μA
		$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{GS} = 5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	500	nA
		$V_{GS} = -5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-500	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 100 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	2.2	3	Ω
		$V_{GS} = 10 V; I_D = 100 \text{ mA}; T_j = 175 \text{ }^\circ C$	-	4.7	6.7	Ω
		$V_{GS} = 5 V; I_D = 50 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	2.5	3.6	Ω
g_{fs}	forward transconductance	$V_{DS} = 5 V; I_D = 100 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	0.3	-	S
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 V; I_D = 100 \text{ mA}; V_{GS} = 10 V; T_j = 25 \text{ }^\circ C$	-	0.21	0.315	nC
Q_{GS}	gate-source charge		-	0.022	-	nC
Q_{GD}	gate-drain charge		-	0.051	-	nC
C_{iss}	input capacitance	$V_{DS} = 30 V; f = 1 \text{ MHz}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	9.2	-	pF
C_{oss}	output capacitance		-	1.6	-	pF
C_{rss}	reverse transfer capacitance		-	0.9	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V; I_D = 100 \text{ mA}; V_{GS} = 10 V; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	1	-	ns
t_r	rise time		-	1	-	ns
$t_{d(off)}$	turn-off delay time		-	2	-	ns
t_f	fall time		-	6	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 210 \text{ mA}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	1	1.6	V
t_{rr}	reverse recovery time	$I_S = 210 \text{ mA}; dI_S/dt = -100 \text{ A}/\mu s; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 \text{ }^\circ C$	-	7	-	ns
Q_r	recovered charge		-	1	-	nC

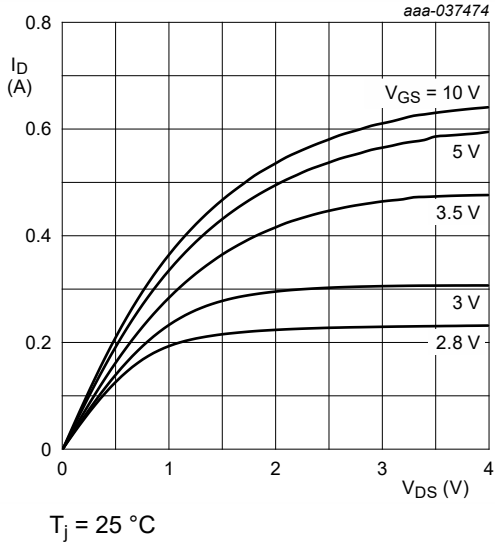


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

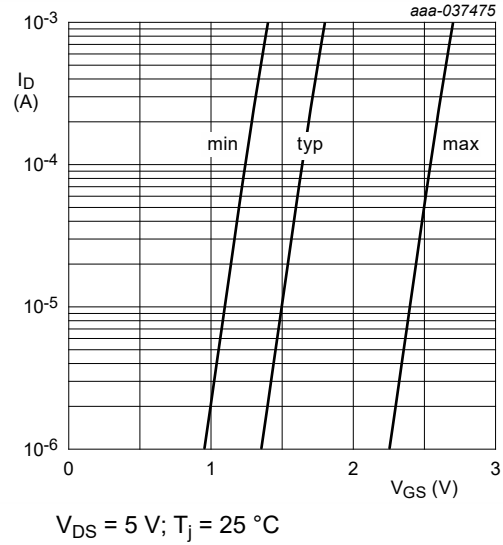


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

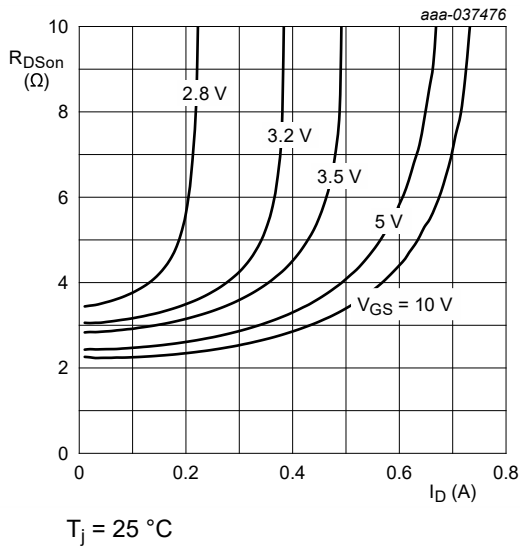


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

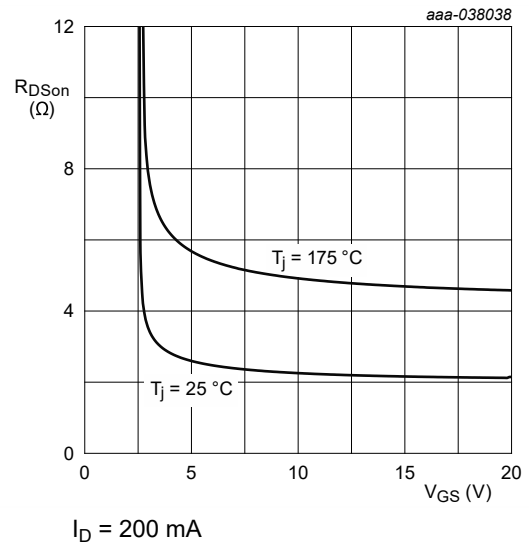


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

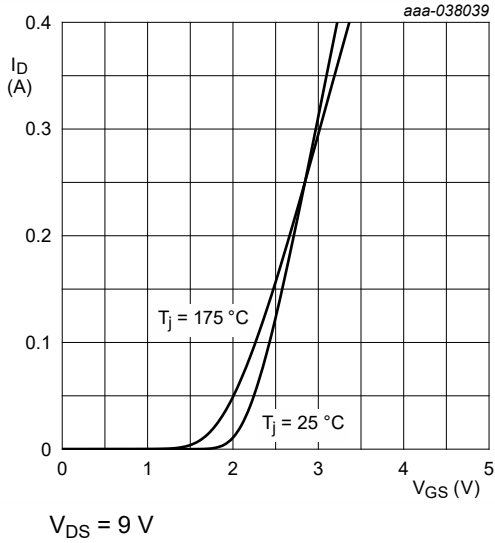
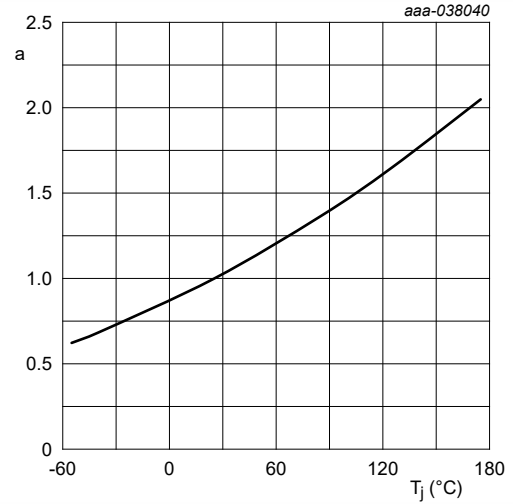


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

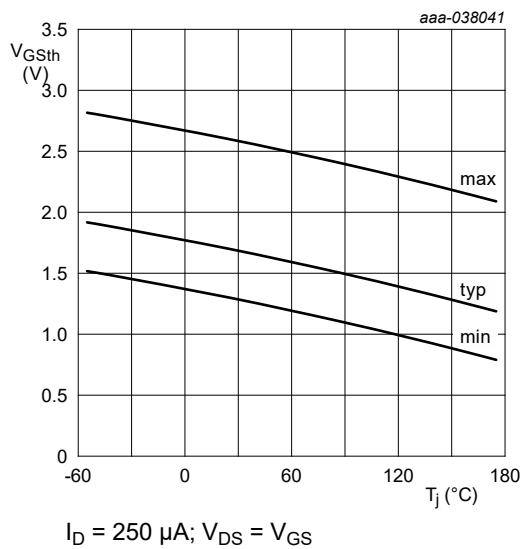


Fig. 12. Gate-source threshold voltage as a function of junction temperature

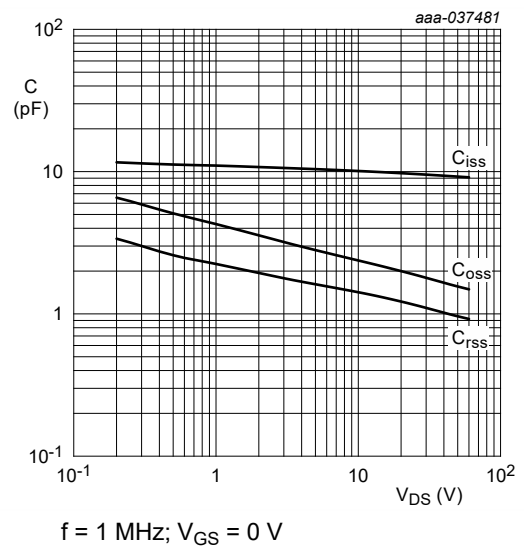
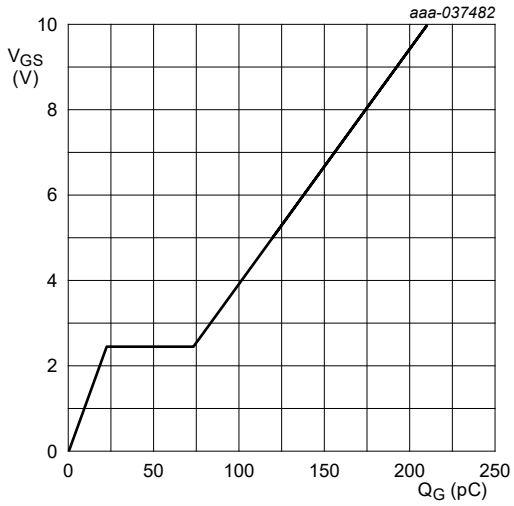


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 0.1 \text{ A}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

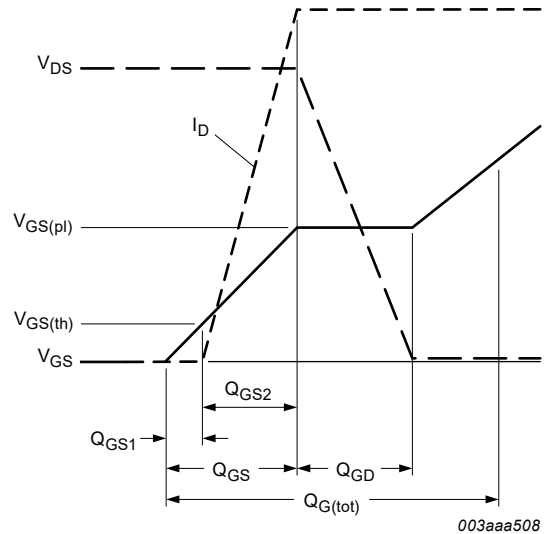
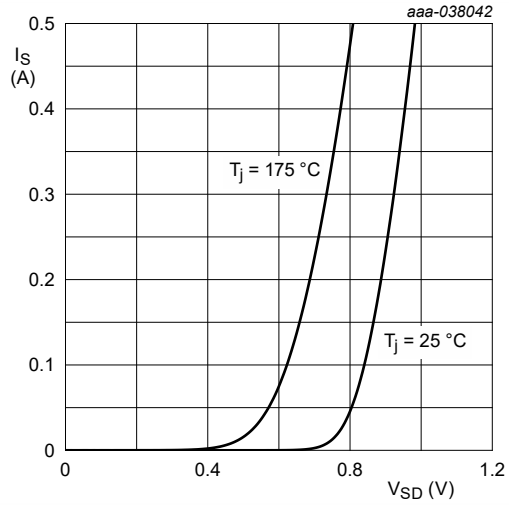


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information



Fig. 17. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

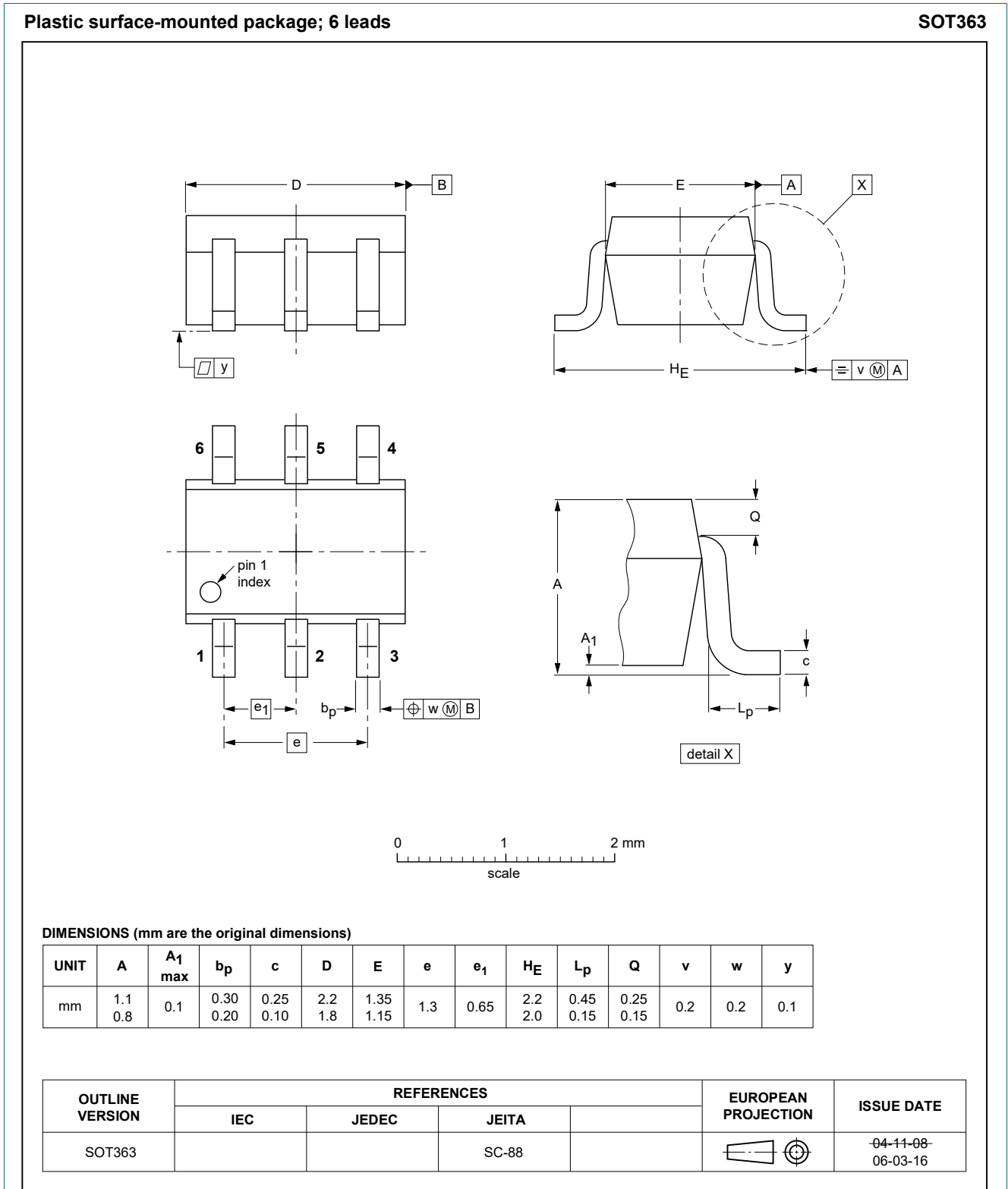


Fig. 18. Package outline TSSOP6 (SOT363)

13. Soldering

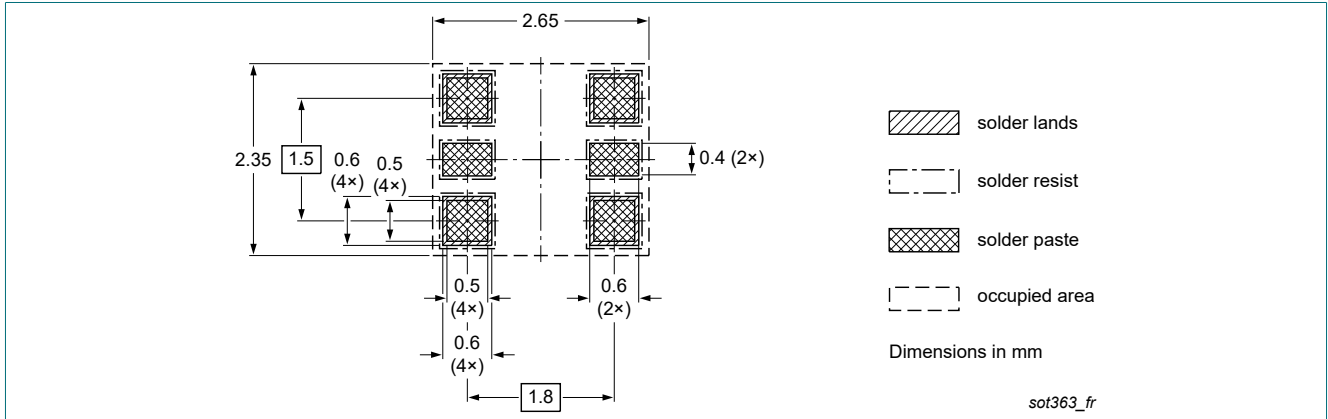


Fig. 19. Reflow soldering footprint for TSSOP6 (SOT363)

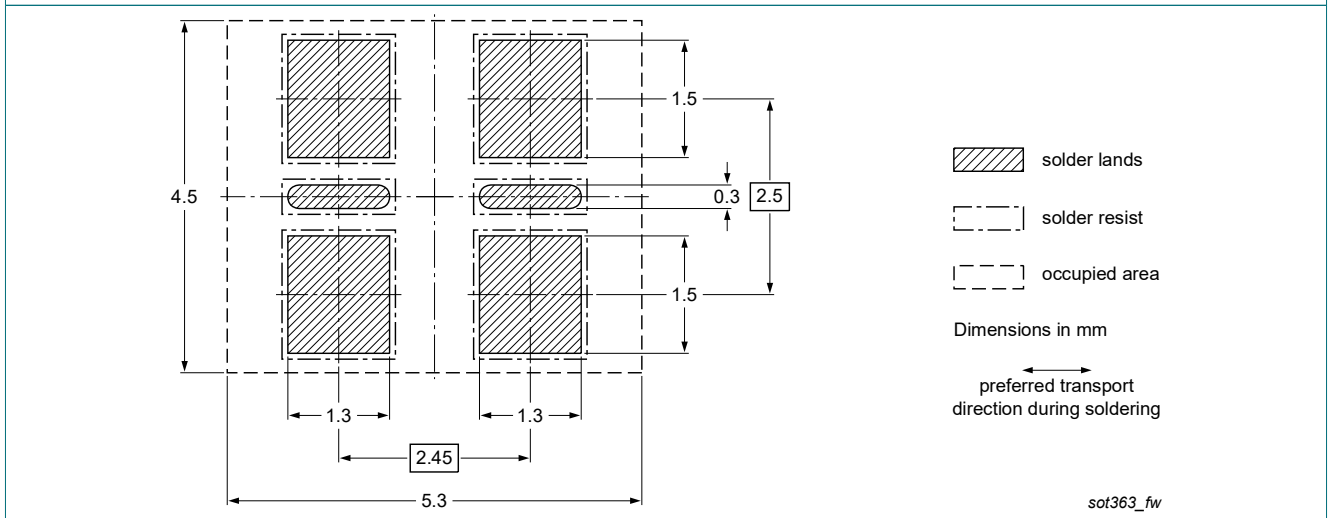


Fig. 20. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
2N7002AKS-Q v.1	20240216	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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