BJT

BIPOLAR JUNCTION TRANSISTOR

APPLICATION HANDBOOK

Design Engineer's Guide

nexperia

Bipolar Junction Transistor Application Handbook

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Preface

Welcome to this handbook, which, like Nexperia's other engineering guides is intended to be a practical, comprehensive, and up-to-date reference work written by engineers for engineers, sharing expertise, application insights and best practices so that application designers can further optimize their electronic circuits.

Nexperia is proud to provide you with this latest reference work which captures yet more its encyclopedic knowledge and expertise in semiconductors. The classical bipolar junction transistor, whose physical principles are around 100 years old and date back to pioneering research performed by Julius E Lilienfeld, forms the basis of modern microelectronics and could be considered to represent the "original cell" on which most modern processors are based.

Today, billions of NPN and PNP bipolar junction transistors are used in a diverse range of applications. The microelectronics industry has experienced massive innovation, which has resulted in minute device structures, nonetheless, discrete BJTs still maintain their relevance. These humble devices have themselves continue to evolve, with newer materials like silicon carbide now enabling environmentally sensitive electric vehicles that meet the performance and range requirements customers expect.

Apart from BJTs, Nexperia's extensive device portfolio features over 15,000 products including diodes, ESD protection devices, MOSFETs, GaN FETs, SiC Diodes, SiC MOSFETs, IGBTs as well as analog and logic ICs. Virtually every electronic design in the world uses Nexperia components, and these products are now recognized as industry benchmarks for efficiency in terms of size, power, and performance.

Nexperia hopes that this handbook will serve readers as a technical dictionary for BJTs and proudly invites you to read, learn and enjoy this outstanding resource which has been designed for ease of navigation.

Finally, I would like to acknowledge the efforts of Burkhard Laue and Eleonora Acerbi, who made significant contributions to this edition.

Olaf Vogt
Director Product Application Engineering
Nexperia

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Chapter 1

Introduction

While CMOS and more recently, wide-bandgap semiconductor technologies generate the most publicity in the technology press, it should never be forgotten that the term 'transistor' (a term derived from the words transfer-resistor) was first associated with a device borne of research performed by William Shockley at Bell Labs in 1948 – the Bipolar Junction Transistor (BJT).

Even though nowadays the humble BJT attracts little attention, billions of these devices are produced by semiconductor manufacturers every year for installation in myriad types of electrical and electronic equipment. Whereas low power consumption is the most attractive feature of CMOS technology, BJTs have advantages in other areas including:

Better power handling capacity:
BJTs are sometimes preferable to use in high-power applications like power amplifiers and motor drivers because of their ability to conduct higher amounts of current than MOSFETs.

Low saturation voltage:
BJTs typically have a lower saturation voltage, a characteristic that enables BJTs to operate more efficiently in some applications like power management and amplification circuits, where minimizing the amount of voltage dropped across the transistor is a key requirement.

Excellent amplification:
BJTs have better gain characteristics, making them especially effective in analog amplifier circuits where minimal signal distortion is essential e.g. audio amplifiers.

Temperature stability:
Compared to MOSFETs, BJTs generally have superior temperature stability. This feature makes them more reliable in environments with widely varying operating temperatures because they can offer more consistent performance.

Low Input capacitance:
BJTs typically have lower input capacitance than MOSFETs. This is beneficial in high-frequency applications where minimizing capacitance is crucial for maintaining signal integrity and reducing distortion.

High-speed operation:
Lower input capacitance enables BJTs to offer superior high-speed operation than MOSFETs. This is an important feature for analog circuits and applications where high-frequency operation is essential like radio-frequency (RF) amplifiers and high-speed switching circuits. Their faster response time makes them the preferred choice for these applications.

Suitability for analog applications:
Many designers prefer to use BJTs s because of their straightforward operation in analog circuit circuits like linear amplifiers. This is because when they are operating in the active region, they provide a more linear relationship between their input and output signals, making them better suited for a range of analog applications like audio circuits and operational amplifiers (opamps).

Rich legacy and ecosystem:
BJTs have been around much longer than MOSFETs and therefore have a more established history in the electronics industry. As a result, designers have collectively developed a vast wealth of knowledge and trusted design methodologies and topologies for using BJTs effectively in a huge range of applications.

The origins of Nexperia's involvement with BJTs can be traced back to its predecessor companies. Nexperia was created in 2017 as a spinoff from NXP Semiconductors, which itself had a rich heritage in semiconductor technology. NXP Semiconductors was formerly part of Philips Semiconductors which had a rich legacy that included manufacturing a variety of electronic components, including BJTs. BJTs remain an integral part of Nexperia's portfolio, catering to specific market demands and applications that require the unique characteristics and advantages offered by Bipolar Junction Transistors. Nexperia now offers a wide range of surface mount device (SMD) packages for BJTs, ranging from the legacy SOT23 package to the most modern in the industry including leadless and clip flat power (CFP) packages. Through ongoing research, development, and manufacturing expertise, Nexperia continues to provide BJTs along with other semiconductor solutions, addressing the needs of customers across different sectors like automotive, industrial, consumer electronics, and more.

In developing this BJT applications handbook, Nexperia has captured the thousands of man years of knowledge and experience that its highly-skilled engineering staff have accumulated while engaging with customers using BJTs in their end applications. Student engineers, hobbyists and seasoned industry experts alike may discover facts about BJTs and their applications that they were previously unaware of when reading this informative and well-researched handbook, which many professional engineers will find very useful in their work.

Chapter 1 addresses the fundamentals of BJTs, describes device structures, physical principles of operation and provides an overview of the main process steps in device fabrication. Chapter 2 reviews various types of BJTs including general-purpose, high-power and matched-pairs, and also discusses the features of resistor-equipped transistors (RETs) and their benefits in switching applications. This chapter also considers types of LED drivers. Interpreting data sheet

parameters for BJTs is explained in Chapter 3 before device behavior from a thermal perspective is explored in Chapter 4. Nexperia's diverse range of SMD package options for BJTs are discussed in Chapter 5, before key quality and reliability considerations are examined in Chapter 6. A wide range of BJT application circuits are presented in Chapter 7, including various amplifier topologies, current sensing, voltage regulation and power as well as audio, discrete digital gate circuits and signal generation applications. Finally, an explanation of modelling and software simulation of BJT devices is provided in Chapter 9.

Chapter 2

The Bipolar Junction Transistor

2.1 Introduction to semiconductor physics

2.1.1 Introduction to semiconductor physics

Electrical conduction in a solid is determined by the concentration of free electrons; i.e., electrons that are shared by atoms forming a bond, and that can freely move. This creates an electron flow called electrical current, and the particles themselves are referred to as charge carriers.

A semiconductor is a material that contains a number (n) of free electrons that is intermediate between that of conductors and that of insulating materials. The number n can be controlled, and increased, through a process called doping.

In the absence of an applied electric field $\vec{E}$, the average electron velocity is zero (all electrons have random speed and direction that balance each other out); if an electric field is applied, the average electron velocity becomes:

$$< \vec{v} >= -\mu_n \vec{E}$$

where μ_n is a coefficient named mobility [$m^2/(V \cdot s)$]. The current density that originates from this velocity is:

$$< \vec{j} >= q\mu_n n\vec{E}$$

where q is the electron's charge, and n is the electron concentration.

Within a solid, electrons arrange themselves in quantized energy levels (i.e., energy can only be equal to certain discrete values), and there is a finite number of states for each energy level.

The Fermi level, E_F, is the highest energy level that electrons can occupy. Electrons however "prefer" to sit in a level with the lowest possible energy.

If the solid body is heated, some electrons can move up to a level with $E > E_F$. This is represented by the well-known Fermi-Dirac distribution (Figure 1), which indicates the probability (between 0 and 1) to find an electron at an energy level E (eV) and temperature T (K). The value of E_F changes based on the solid's material.

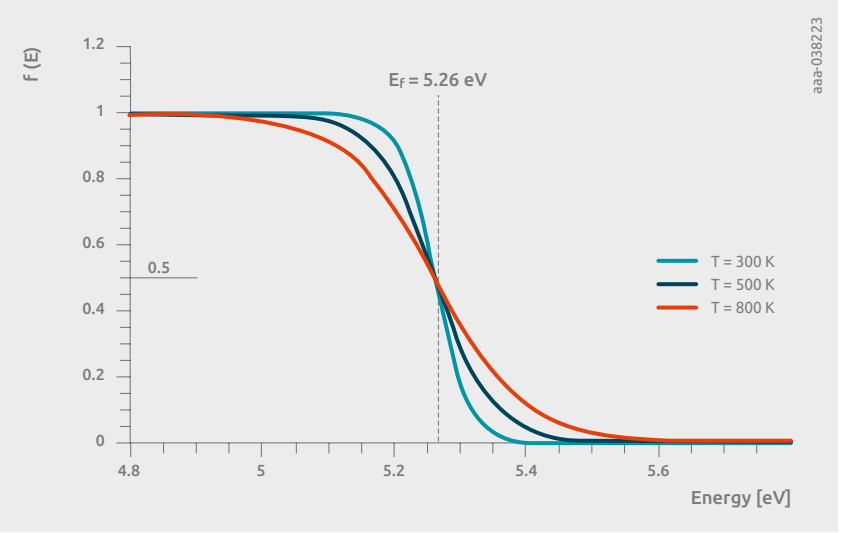


Figure 1 | The Fermi-Dirac distribution

The difference between the Fermi level and the so-called vacuum level is the minimum energy that must be applied to extract an electron from the material (see Figure 2).

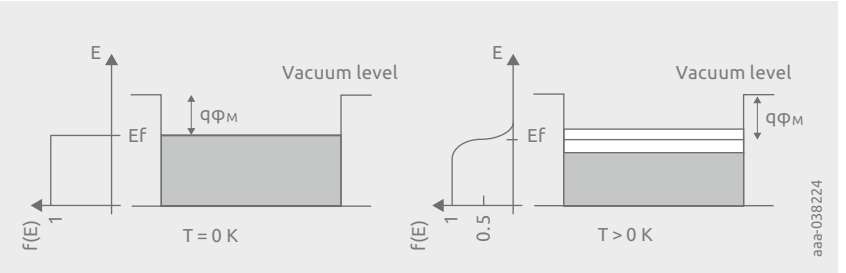


Figure 2 | Fermi-Dirac distribution and representation of the vacuum level at different temperatures

Schrödinger's equation for potential can be solved only for certain energy values and has no solution for others. The permitted energy levels are called bands, and the forbidden ones gaps. In a crystalline material such as silicon, whose energy bands are shown in Figure 3, only the penultimate band (the valence band) and the last band (the conduction band) contribute to conduction. The forbidden gap for silicon is also shown in Figure 3, and measures 1.12 eV.

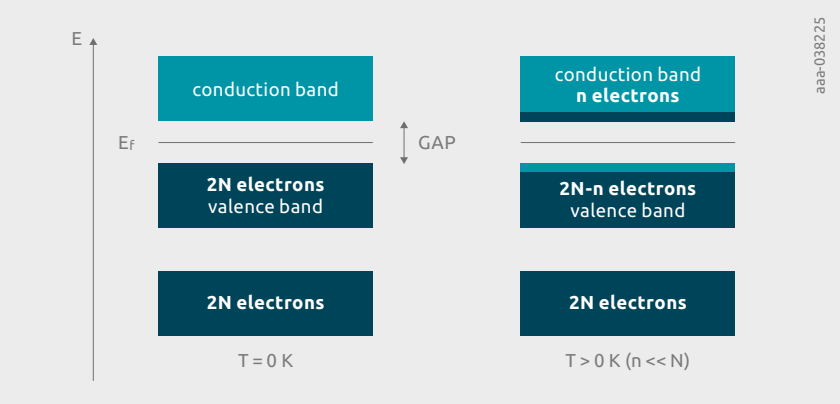


Figure 3 | Occupation of bands in a group IV element such as silicon

If energy is supplied to the material (for example by heating), an electron in the valence band can skip the gap and position itself in the conduction band (this is called generation), leaving a hole (with positive |q| charge) in the valence band. It can also go back down to the valence band, in a process called recombination.

In this chapter we will use the simple band diagram shown in Figure 4, considering electrons with a negative charge in the conduction band, and holes with a positive charge in the valence band, while the x-axis indicates the position within the material.

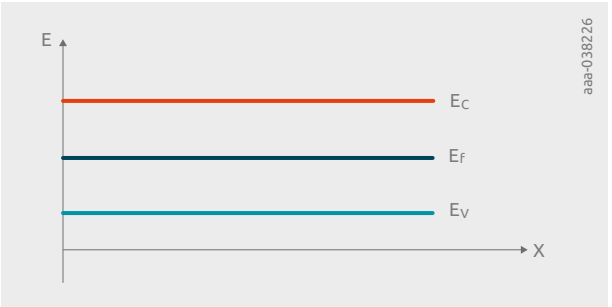


Figure 4 | Band diagram of a semiconductor; E_F is the Fermi level, E_C is the energy of the bottom of the conduction band, E_V the energy of the top of the valence band

The concentration of holes in the valence band and electrons in the conduction band can be altered through a doping process.

In a non-doped (intrinsic) semiconductor, the Fermi level (see E_i in Figure 5) is positioned in the middle of the forbidden gap, indicating the energy where the probability of finding a free electron is ½. In a doped semiconductor, the Fermi level (see E_F in Figure 5) moves up or down because the probability of finding an electron in the conductance band or a hole in the valence band has changed.

With n-doping, free electrons are introduced by adding donor atoms such as phosphorus (P) or arsenic (As), which release electrons. In p-doping, holes are increased by adding acceptor atoms such as boron (B), which captures electrons from neighboring atoms. The concentration of donors and acceptors is indicated respectively as N_D and N_A.

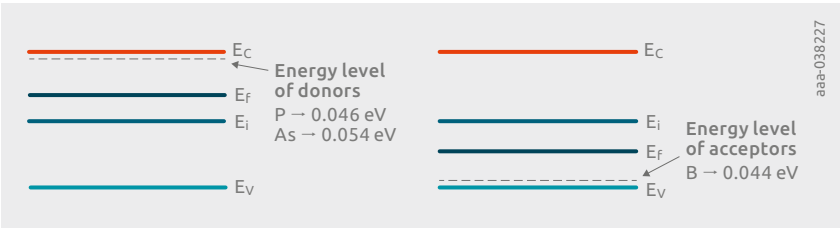


Figure 5 | Band diagram in a doped semiconductor (n on the left, p on the right)

In a semiconductor, two types of electrical current are present.

The drift current is generated by the presence of an electrical field $\vec{E}$, which acts on the carriers (the current flows in the same direction as $\vec{E}$). The drift current densities for electrons (n) and holes (p) take the form:

$$\begin{cases} \vec{J}_n = q\mu_n n\vec{E} \\ \vec{J}_p = q\mu_p p\vec{E} \end{cases}$$

where q is the electron's charge, $\mu_{n/p}$ the mobility constants, n and p the concentrations of electrons and holes, and $\vec{E}$ the electric field vector.

The other type of current is called diffusion current; here, like the molecules of a gas, the charge carriers diffuse from areas with higher concentrations to areas with lower concentrations; the expression is the following:

$$\begin{cases} \vec{J}_n = qD_n \dfrac{dn}{dx} \\ \vec{J}_p = -qD_p \dfrac{dp}{dx} \end{cases}$$

where D_n and D_p are diffusion constants [m²/2] in the form $D_{n/p} = \frac{kT}{q}\mu_{n/p}$ (k is Boltzmann's constant, T is temperature [K]).

The drift and the diffusion components are both present at the same time in a semiconductor.

In the absence of an externally applied voltage, but with a concentration gradient (in this case, of electrons) as shown in Figure 6 ($n_{x1} > n_{x2}$), there will be a diffusion current $J_{n\text{-}diff} \neq 0$.

However, in order for the total current to be 0, the diffusion current needs to be counteracted by a drift component. An opposing electric field, and therefore potential, is present; this potential can be calculated by knowing the concentrations n_{x1} and n_{x2}.

This phenomenon can also be observed in the band diagram in Figure 6: the electrons tend to diffuse toward the right side (lower n concentration), but the bands bend upward to oppose their flow.

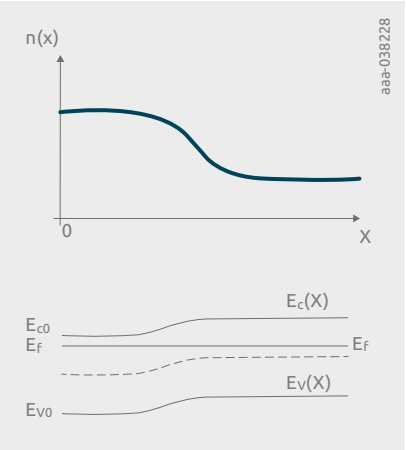


Figure 6 | Bands bending because of a concentration gradient of electrons

Because generation-recombination phenomena can alter the number of each type of carrier, on a microscopic level the current density of electrons (or holes) can vary along the x-axis; nonetheless, the overall current is constant. This is the equivalent of Kirchhoff's law on a microscopic scale:

$$J_p + J_n = Const$$

2.1.2 Diodes

When two pieces of counter-doped (n and p) semiconductor are placed side by side, an electronic device called a diode is formed. The diode is a unidirectional device, meaning that current can only flow in one direction: when a positive voltage is applied between the anode (p side) and the cathode (n side), the diode acts as a short-circuit; when a negative voltage is applied, the diode acts as an open circuit.

The diode is the most basic electronic device, from which all others are derived, in particular the bipolar junction transistor (BJT).

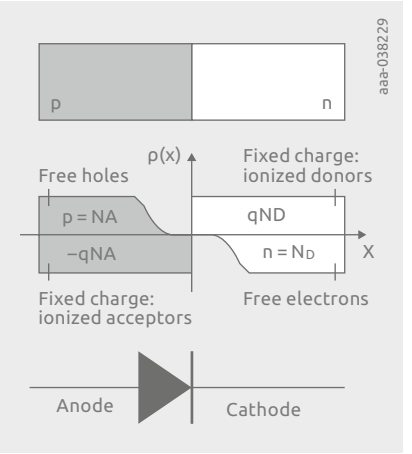


Figure 7 | Top) a p-n junction; middle) fixed charges (ionized acceptors and donors) and free charges (holes and electrons) in a p-n junction, vs. position in the material; bottom) schematic symbol of a diode

As shown in Figure 7, let us consider a junction with p-doping on the left (with acceptor ion concentration N_A), and n-doping on the right (with donor concentration N_D). The derivative of the carrier concentration profiles at the junction (x = 0) must be zero: if the concentrations formed a step, the diffusion currents which depend on these derivatives would paradoxically be infinite.

The free charges (free electrons and holes) rearrange internally as shown in Figure 7, to balance out the diffusion currents, thus generating a so-called built-in voltage between p and n:

$$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

where V_T is a constant that depends on temperature T (K), N_A and N_D are the acceptor and donor concentrations, and n_i the concentration of electrons and holes in intrinsic silicon.

The positive and negative charges can be approximated as shown in Figure 8, and then algebraically added; the result shown in the bottom picture is called full depletion approximation. The approximation assumes that in an area between $-x_p$ and x_n there are no free charges: the only charges present are ionized donors (N_D) or acceptors (N_A). Consequently, all that is left is a positive area on the right and a negative area on the left (Figure 8, bottom).

It should be noted that the net overall charge should be zero (although locally charged areas do exist).

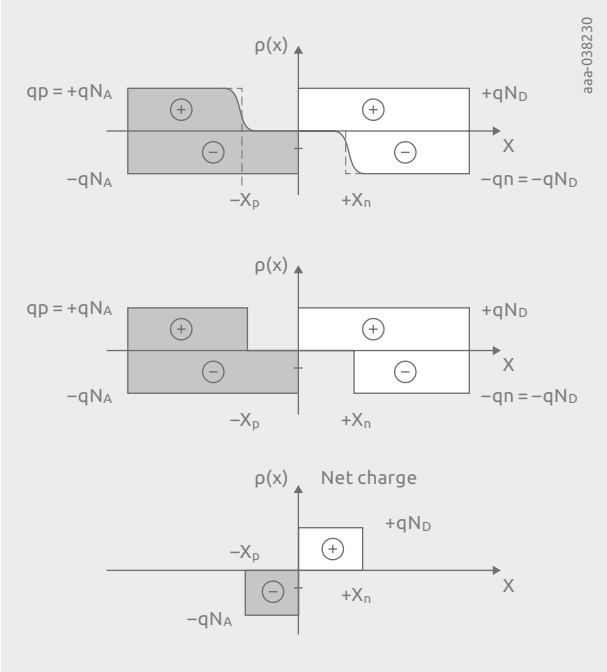


Figure 8 | Charge (top) and net charge approximation (middle and bottom) in a p-n junction

The electric field obtained after solving Poisson's equation has a negative maximum at the junction (see Figure 9) and is equal to zero outside of the depletion region $[-x_p, x_n]$. Its expression is the following:

$$\begin{cases} E(x) = -\dfrac{qN_A}{\varepsilon_s}(x + x_p) & -x_p < x < 0 \\ E(x) = +\dfrac{qN_D}{\varepsilon_s}(x - x_n) & 0 < x < x_n \end{cases}$$

Note that the field goes from n to p. Moreover, the depletion region is W wide and extends further in the less doped side of the junction (see Figure 9, bottom graph).

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_0}$$

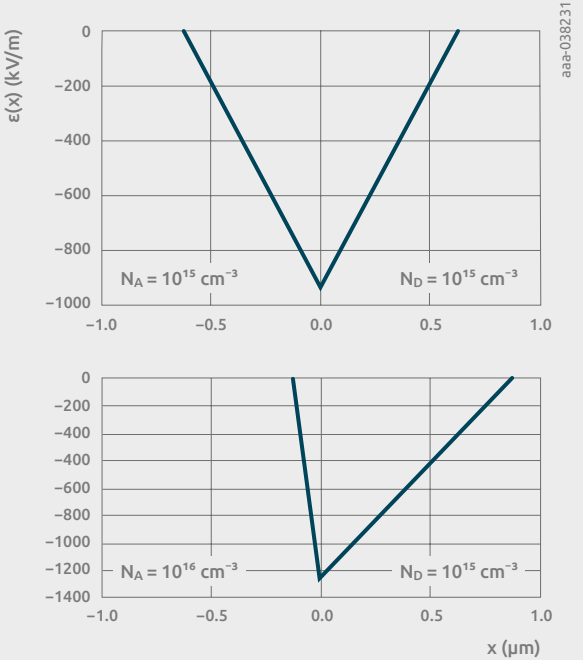


Figure 9 | Electric field in a p-n junction with symmetric doping (top) and asymmetric doping (bottom)

The potential in the p-n junction can be found by integrating the electric field, which can be seen in Figure 10 along with a band diagram. The potential that's established at the sides of the junction is the built-in potential, which serves to balance out the diffusion currents; it can be demonstrated that the Fermi level is constant at equilibrium (no external voltage applied, net current equal to zero).

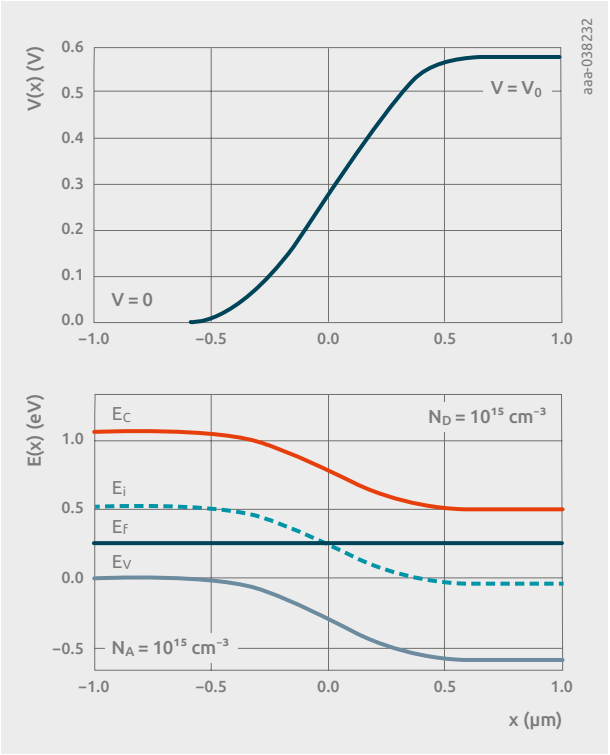


Figure 10 | Variation of the potential along the x-axis (top) and band diagram (bottom) in a p-n junction with no external voltage applied

If an external voltage is applied to the junction between anode and cathode, two outcomes are possible. If V is positive, and therefore opposed to V_0, the barrier between p and n lowers: the diffusion components dominate over the drift currents and more carriers can flow from one side to the other (holes toward n and electrons toward p). This condition defines the direct polarization of the diode.

If V is negative, the barrier becomes higher: this phenomenon inhibits conduction and the only possible current is that of minority carriers (the few electrons in p, and the few holes in n) moving to their "native" side. This small current is called inverse saturation current: the diode is considered in its off-state. It should be noted that when the diode is reverse polarized, its depletion region widens.

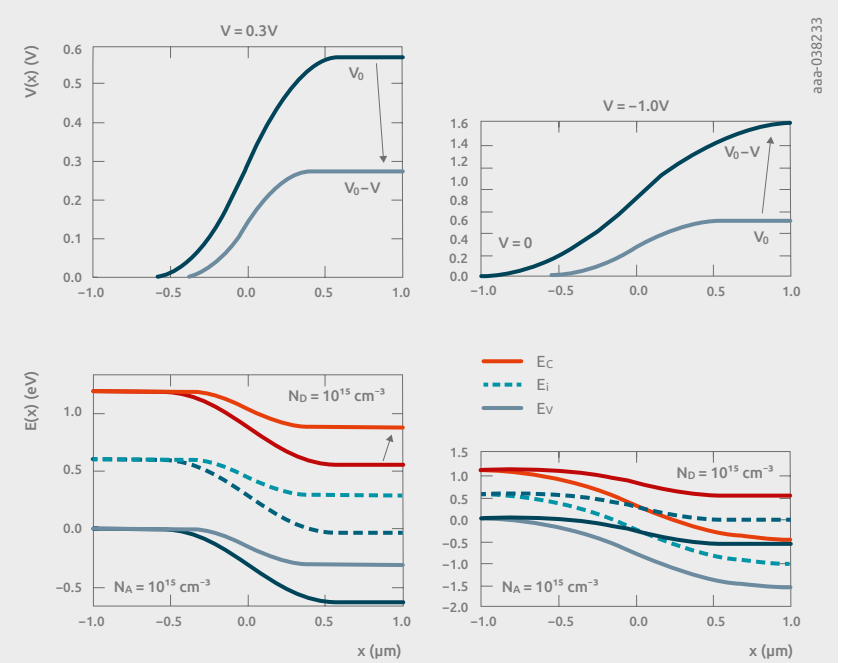


Figure 11 | Potential and band diagrams in the case of direct polarization (left) and reverse polarization (right)

It's important to note that, if a voltage V is applied, the Fermi level ceases to be constant across the material: E_{fp} and E_{fn} are misaligned and depend on V, as shown in Figure 12.

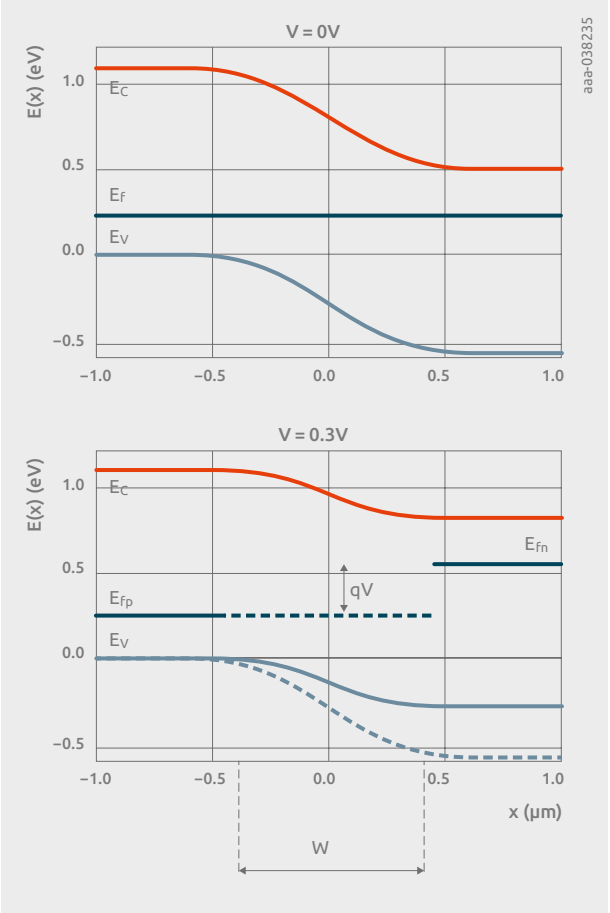


Figure 12 | Unequal values of E_{fp} and E_{fn} following the application of a voltage V

The law of mass action, valid at equilibrium,

$$np = n_i^2$$

now changes to Shockley's equation:

$$np = n_i^2 e^{\frac{qV}{kT}}$$

This equation is useful to calculate the excess minority carriers $p(x_n)$ or $n(-x_p)$, which is found to be inversely proportional to the concentration of majority carriers. If, for example, $N_A \gg N_D$, the injection of holes in x_n is much higher than that of electrons in $-x_p$.

In every diode two currents coexist: a hole current and an electron current. Outside of the depletion region Ë is very low, and on each side the minority carrier concentration is also low; for this reason, the drift components $q\mu_n nE$ and $q\mu_p pE$ are negligible for minority carriers.

For $x > x_n$ we shall consider:

$$\begin{cases} J_p \cong -qD_p \dfrac{dp}{dx} \\ J_n = q\mu_n nE + qD_n \dfrac{dn}{dx} \end{cases}$$

For $x > x_p$:

$$\begin{cases} J_n \cong qD_n \dfrac{dn}{dx} \\ J_p = q\mu_p pE - qD_p \dfrac{dp}{dx} \end{cases}$$

As shown by the previous expressions, the currents depend directly on the profiles of minority carriers, which can be approximated as shown in Figure 13. The profiles can be assumed linear in a short-base diode, so called because the bases (W_n and W_p in the pictures) are short enough that all carriers recombine on the opposite contact. In a long-base diode, on the other hand, carriers recombine in the silicon, and the profiles are assumed to be exponential.

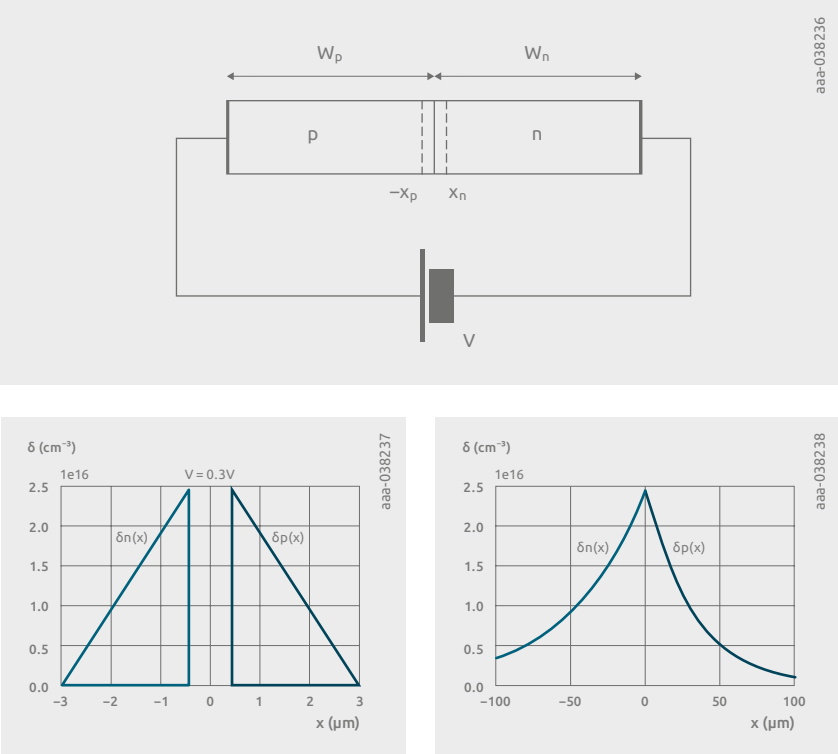


Figure 13 | Bases of a diode (top); profile of minority carriers in a short-base diode (bottom left) and in a long-base diode (bottom right)

In all cases, the profile of majority carriers is not zero and is identical to the profile or minority carriers but is negligible with respect to the dopant concentration N_A, N_D (low injection hypothesis).

After making the necessary calculations, the expression for J in a junction with generic doping is:

$$J = J_n(x) + J_p(x) = \left(q\frac{D_p}{L_p}\frac{n_i^2}{N_D} + q\frac{D_n}{L_n}\frac{n_i^2}{N_A}\right)\left(e^{\frac{V}{V_T}} - 1\right) = J_0\left(e^{\frac{V}{V_T}} - 1\right)$$

Both $J_n(x)$ and $J_p(x)$, shown in Figure 14, consist of a diffusion and a drift component, and they add up to a constant value. To get the current from current density, multiply J by the section of the junction, S. I_0 is called inverse saturation current of the diode and is the small current that flows when the diode is reverse polarized.

$$I = JS = J_0 S\left(e^{\frac{V}{V_T}} - 1\right) = I_0\left(e^{\frac{V}{V_T}} - 1\right)$$

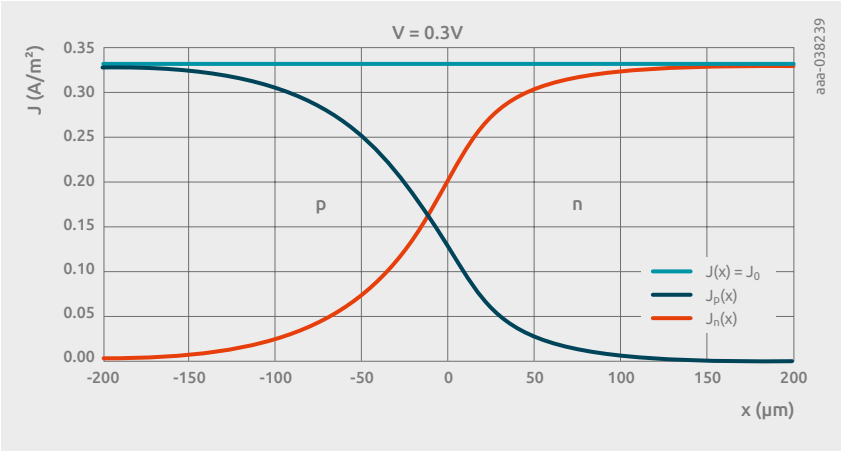


Figure 14 | Current densities in a p-n junction; minority carriers reach a maximum on each side of the depletion region

Referring to Figure 15, which shows the diode's current vs. applied voltage, it can be seen that I increases exponentially starting from 4÷5 V_T, around 100 mV. Below 100 mV, I is equal to the inverse saturation current.

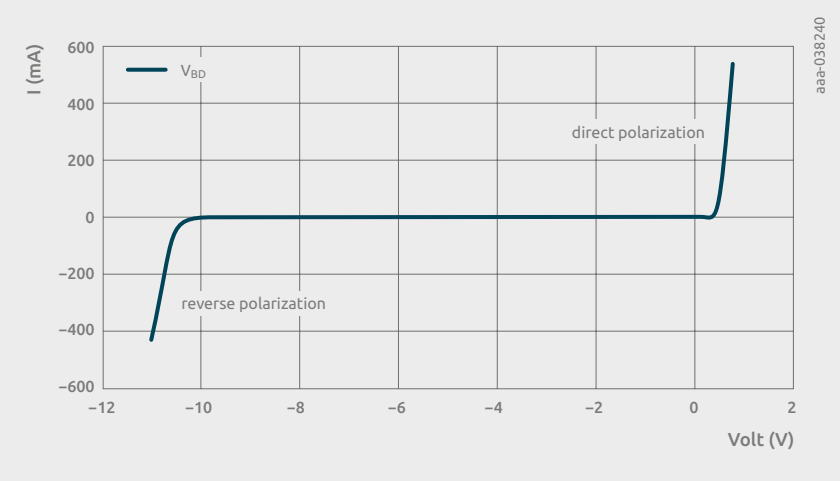


Figure 15 | I-V characteristic of a 10 V Zener diode

In a short-base diode under reverse bias, the depletion region can become so wide that it reaches the end of one or both bases (note that the depletion region extends more in the less doped base). This phenomenon, called punch-through, makes the reverse current suddenly surge as the diode loses its unidirectional feature.

In addition to punch-through, which affects short-base diodes, another important effect is a junction's breakdown. Breakdown happens when high currents and voltages (i.e., high power) are applied to a junction and lead to its failure. Breakdown can happen for multiple reasons, including the Zener effect, where a steep bending of the bands in reverse polarization lets majority carriers flow by means of tunneling, and the avalanche effect, where an enormous number of electron-hole pairs are generated through impact against the reticle, having applied an electric field E > E_{BD} (E_{BD} being a function of doping).

2.1.3 Structure of a BJT

A BJT is composed of a pair of junctions, either PN-NP or NP-PN (respectively forming a PNP or an NPN transistor). Figure 16 shows the structure of two BJTs.

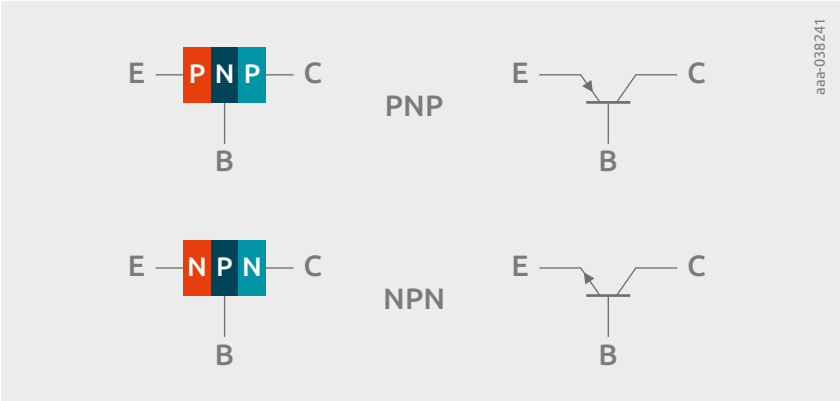


Figure 16 | Structure of PNP and NPN BJTs

Referring to Figure 16, the central part of the BJT is the base, while the right and left sides are called emitter and collector.

Typically, the emitter is more heavily doped than the base, and the collector is less doped than the base, resulting in P^+NP or N^+PN structures; the purpose of this is to boost the injection of minority carriers in the direction of emitter to base (rather than the other way around).

Figure 17 shows the positive direction of currents and the naming of the voltages in a BJT. According to Kirchhoff's laws, the following equations must be true:

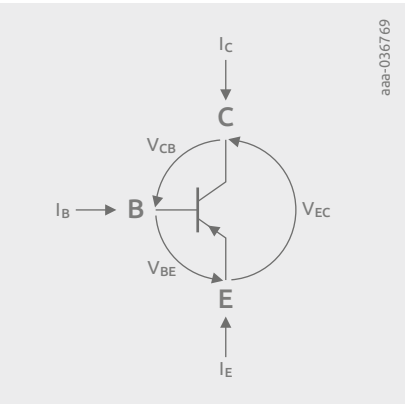


Figure 17 | Naming of the voltages in a BJT

$$I_E + I_B + I_C = 0$$

$$V_{EB} + V_{BC} + V_{CE} = 0$$

Because it is composed of two junctions, a BJT can have radically different behaviors based on how these junctions are polarized. The polarization of the emitter-base and collector-base junctions defines four different working conditions for the device, shown in Figure 18.

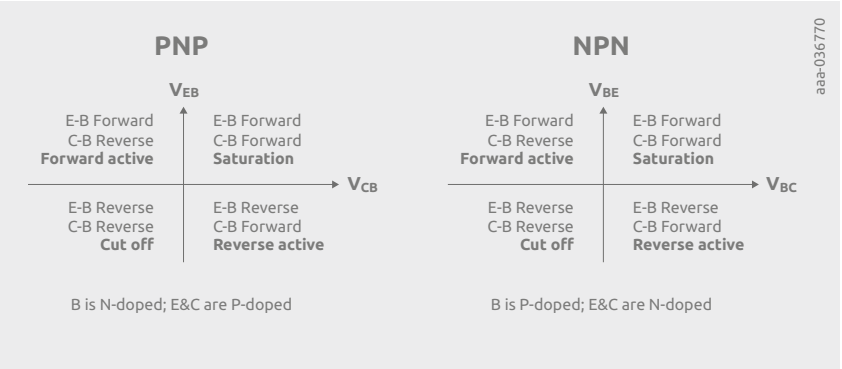


Figure 18 | Voltage values determining the four different regions of operation

The most important region of operation for a BJT is the forward-active region, where the emitter-base junction is forward biased, and the collector-base junction is reverse biased. The emitter-base junction injects carriers into the base, and the collector-base junction "sucks them out" of the base toward the collector. For an NPN transistor, the forward-active region happens when $V_{BE} > 0$ and $V_{BC} < 0$. Conversely, for a PNP transistor it is necessary to apply $V_{BE} < 0$ and $V_{BC} > 0$.

In this region, a BJT outputs a current, I_C, controlled by a much smaller current, I_B: the I_C/I_B ratio is defined as β, the gain of the transistor. A high β in this region of operation suggests using the device to make a power amplifier.

The saturation region and the cutoff region each have comparable I_C and I_B values, so they lack the element of controlling a larger current with a smaller one, making them less appealing than the forward-active region for analog applications. The saturation and cutoff regions are typically only used in digital circuits.

Lastly, the reverse-active region would seem to be identical to the direct-active region, but the higher emitter doping causes β (current gain) to be much higher in the latter.

2.1.4 Carrier flow in a BJT

If $W_0 \gg L_p$, where L_p is the diffusion length of holes (simply put, how far holes travel before recombining with an electron), the BJT is equivalent to two back-to-back diodes. On the contrary, if $W_0 \ll L_p$ the two junctions directly interfere with each other and form a BJT.

We define W_{eff} (or simply W) as the distance between the limits of the two depletion regions ($W_{eff} \leq W_0$); in other words, W_{eff} is the quasi-neutral region of the base where minority carriers coming from the emitter diffuse toward the collector. W_{eff} varies according to how the junctions are polarized (for example, inverse polarization expands a junction's depletion region, thus lowering W_{eff}).

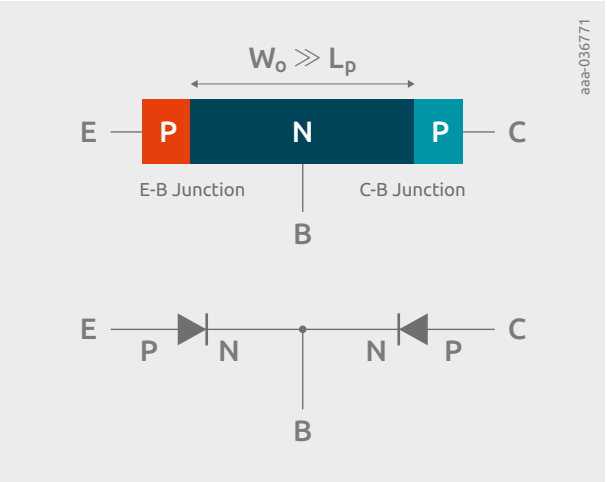


Figure 19 | Representation of a long-base bipolar transistor

From diode theory we know that a depletion region is broader on the less doped side of a junction: for this reason, the depletion region from the EB junction will extend more in the base (highly doped emitter), and on the collector's side of the BC junction (lower collector doping). Moreover, in the forward-active region of operation, the BC junction's depletion region will be broader than that of the EB junction (because the former is inverse biased).

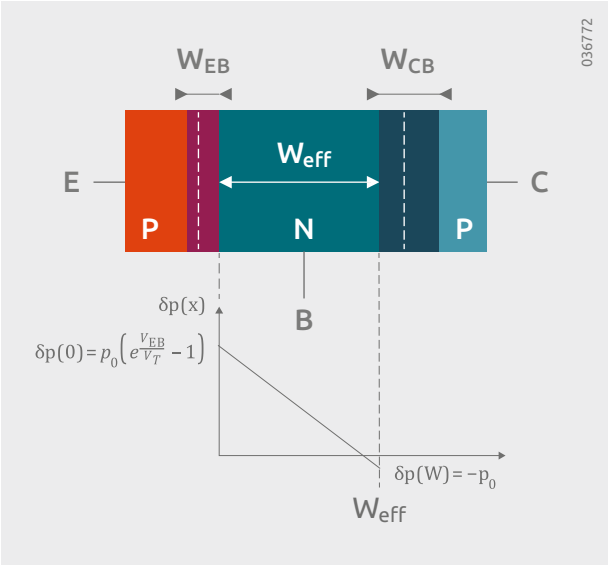


Figure 20 | Sizes of the two depletion regions and excess carrier (hole) concentration in the base

2.1.5 Definition of β_F

In a short-base P^+N diode, most holes injected by the P^+ side reach the opposite electrode and immediately recombine upon contact. Transit time is called τ_t. Nonetheless, even in short-base diodes, some of the carriers recombine before reaching the electrodes, every τ_p (carrier lifetime, in this case: holes). The diode's total current is then:

$$I = \frac{Q}{\tau_t} + \frac{Q}{\tau_p}$$

where Q is the total charge given by the carriers, mostly holes in a P^+N diode, which are moving through the device (found by integrating the carrier excess concentration in Figure 20).

Similarly, in a PNP transistor, holes are injected into the EB junction by the emitter and reach the right border of the depletion region; once they arrive at the transistor's base, most of them reach the CB junction with a transit time τ_t: here they are swept away toward the collector by the strong electric field of the inversely biased collector-base junction. The collector current (negative because it flows out of the device) will then be:

$$I_C = -\frac{Q}{\tau_t}$$

The base provides the few electrons that allow a small number of holes to recombine in the quasi- neutral region, therefore:

$$I_B = -\frac{Q}{\tau_p}$$

Lastly, the emitter provides all the minority carriers (holes) that flow into the base:

$$I_E = \frac{Q}{\tau_t} + \frac{Q}{\tau_p}$$

A key element in the physics of the BJT is this: if W_{eff} is short enough compared to the carriers' diffusion lengths, in this case $W_{eff} \ll L_p$, most carriers reach the opposite side of the base without recombining with electrons. This also means that $\tau_t \ll \tau_p$, and given the formulas above for I_C and I_B, $I_B \ll I_C$.

Figure 21 shows a possible polarization for a PNP transistor: I_B is given by a current source, so that $|Q| = I_B\tau_p$; a voltage V_{EC} is applied. The current source can change the voltage at its terminals so a specific amount of charge Q can flow through it, thus forcing a fixed I_B: I_C is dependent on Q, and is therefore controlled by I_B. This dependency is expressed by the parameter β_F (current gain in the forward-active region):

$$\beta_F = \frac{I_C}{I_B}$$

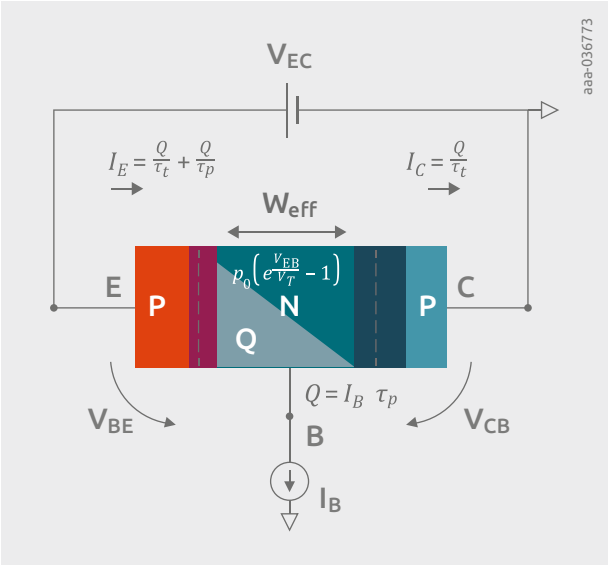


Figure 21 | Polarization of a BJT with current supply I_B and voltage supply V_{EC}

It should be noted that β_F is higher the shorter the base width is:

$$\beta_F = \frac{I_C}{I_B} = \frac{\tau_p}{\tau_t} = 2\frac{L_p^2}{W_{eff}}$$

2.1.6 Input–output characteristics

A fundamental piece of information about BJTs is given by their input or output characteristics. By characteristics we mean a group of parametric curves showing a device's current as a function of its voltage and a third parameter; for example, in the case of a BJT in the common emitter configuration (with the emitter terminal chosen as ground) we usually consider:

- Output characteristics (Figure 22):
  I_C as a function of V_{CE} using I_B as a parameter
- Input characteristics (Figure 23):
  I_B as a function of V_{BE}, with V_{CE} as a parameter

It is important to note that the input and output characteristics of an NPN transistor have an odd symmetry with respect to those of a PNP transistor, because currents and voltages have opposite signs.

Output characteristics in the common emitter configuration show I_C with a fixed value of I_B (so they implicitly display the gain β_F). The equation of output characteristics in the common emitter configuration is:

$$I_C = \beta_F I_B - I_{CE0}\left(e^{-\frac{V_{CE}-V_{BE}}{V_T}} - 1\right)$$

but in practical terms, if the device can be considered in the forward-active region, $I_C \sim \beta_F I_B$.

Generally speaking, the forward-active region is located in the output characteristics where $V_{CE} > 0.3$ to 0.4 V (see Figure 22 on the right of V_{CEsat}). On the other hand, for $V_{CE} < V_{BE}$, the BJT is in the saturation region (see Figure 22, left side of V_{CEsat}).

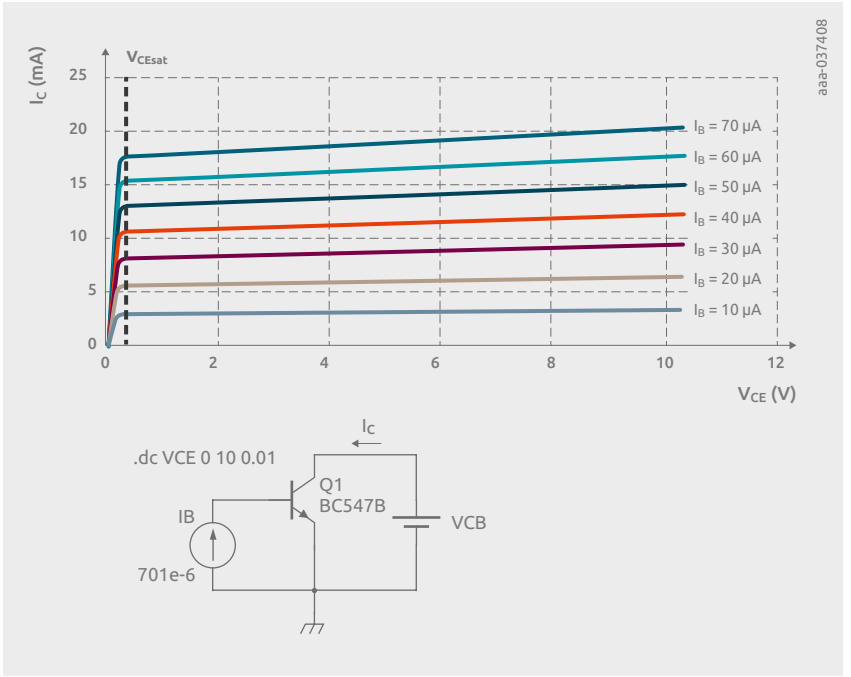


Figure 22 | Output characteristics for an NPN transistor

In truth, although in the forward-active region $I_C \sim \beta_F I_B$, β_F actually grows for higher values of V_{CE}, which accounts for the slanted characteristics in Figure 22. This happens because $\beta_F = \alpha_F / (1 - \alpha_F)$, and α_F is:

$$\alpha_F = \frac{1}{1 + \frac{W_{eff}^2}{2L_n^2}}$$

If the value of V_{CE} rises, so does the reverse polarization of the CE junction, which in turn expands the CE depletion region, and W_{eff} shrinks (this is called base-width modulation). Consequently, higher V_{CE} values correspond to higher β_F values.

Regarding input characteristics (Figure 23), I_B depends almost exclusively on V_{BE}, much less on V_{CE}, and therefore the graph looks like a diode's current (the N^+P/P^+N emitter-base junction):

$$I_B = f(V_{BE}, V_{CE})$$

As Figure 23 shows, for $V_{CE} > 1$ (in the forward-active region) the curves are nearly coinciding; for $V_{CE} = 0$ though (or generally in the saturation region, where $V_{CE} < V_{BE}$ and $V_{BC} > 0$), the base is flooded with charges coming both from the emitter and the collector which are forward biased, so even small changes in V_{CE} influence I_B. All things considered, in the forward-active region of operation, V_{BE} is considered a diode, with a 0.6 to 0.7 V voltage drop.

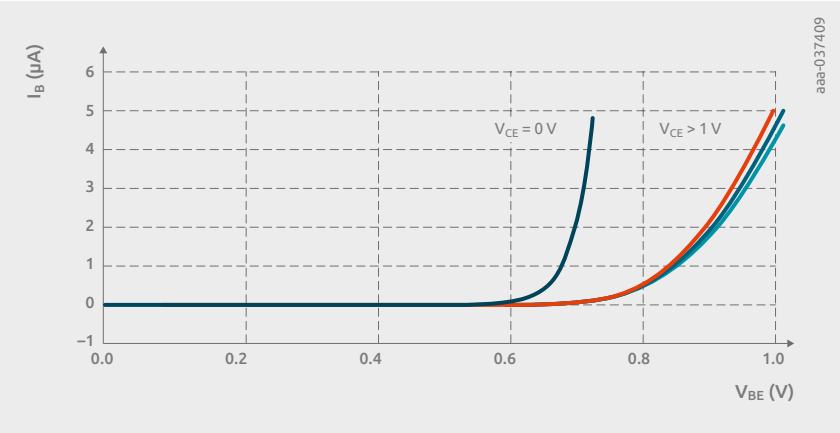


Figure 23 | Input characteristics of an NPN transistor (for multiple values of V_{CE})

2.2 Bipolar transistor fundamentals

2.2.1 Production process

In common integrated circuit (IC) processes, all connections to the outside world are located on the front side of the die. The advantage of this is that, through use of isolation, many electrical components with different functions can be combined on one chip, as in an IC. For example, if several NPN transistors were manufactured on one IC chip without isolation, they would all have a common collector.

For bipolar ICs containing an NPN as well as a PNP transistor, the so-called planar process is used. In this process the NPNs are fabricated vertically (left side of Figure 1) and the PNPs laterally (right side of Figure 1). A low-doped N-epi is grown on a low-doped P-substrate. By diffusion of P-type isolation between the components, N-type isolated pockets are formed in which the components can be formed. If the P-type substrate is put at the most negative voltage of the circuit, each pocket is isolated by a reverse-biased P-N junction.

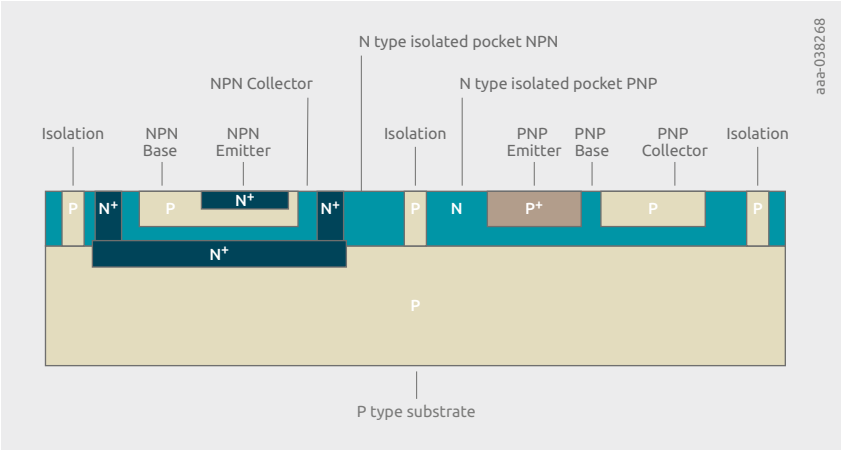
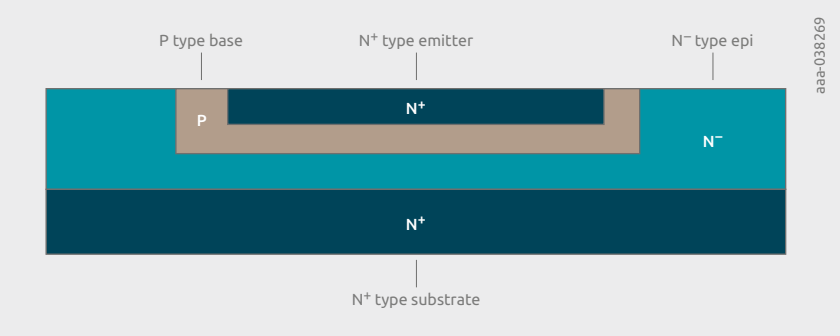


Figure 1 | NPN and PNP BJTs in a monolithic IC manufactured using the planar process

To minimize the resistance of the current path from the NPN collector under the NPN base back to the top of the die surface, a high-doped N+ layer is added below the NPN transistor and beside it. Still, the NPN transistor is vertical and can be quite effective, alongside the resistive path of the collector contact to the surface. In the planar NPN transistor the width of the base, which is important for defining the current gain, is defined by the diffusion of the emitter into the base.

To manufacture the PNP transistor using the same process, this transistor must be lateral (right side of Figure 1). Here the width of the base is instead defined by the lateral distance between the emitter and collector diffusions, and cannot also be defined as for the NPN planar transistor, because it is dependent on lithography and etching processes as well as the lateral diffusion of emitter and collector. Therefore, the performance of the PNP transistor is normally much worse than the NPN transistor in the planar IC process.



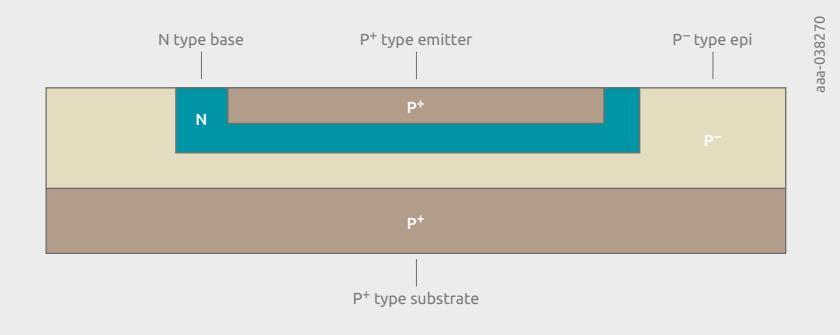


Figure 2 | a) NPN vertical discrete BJTs; b) PNP vertical discrete BJTs

On the other hand, for a discrete bipolar junction transistor (BJT), it is not necessary to have isolation or one polarity being lateral. In contrast to the IC process, the substrate is chosen as low ohmic, and the collector contact can be made on the back of the die instead of the front. In this way the transistor can be made much more efficient.

1. No die area has to be used for isolation.
2. No die area has to be used for routing a low-ohmic collector contact to the die front.
3. The collector resistance will be much lower because the whole die area can be used as the collector contact.
4. PNP and NPN transistors can be located vertically, resulting in much more efficient PNP transistors.
5. The blocking voltage will be better, because the area under the base in a vertical transistor is not restricted by the increased field of the three-dimensional curvatures of the emitter and collector areas in a lateral transistor.

General description of the fabrication process (vertical)

Here the basic manufacturing process of an NPN BJT is described. (For a PNP-BJT, simply replace all N-doping with P-doping and all P-doping with N-doping.) Note that the images are not to scale, for clarity.

The process starts with a low-ohmic N+ substrate. On this substrate a low-doped epi is grown.

In the next step an oxide is grown on the epi surface, and a photoresist is spun onto the wafer surface (see Figure 3).

The pattern for the base is transferred by photolithography and the photoresist is exposed to light. The properties of the exposed areas change and the resist is developed.

The photoresist that was not exposed protects the oxide from the etching chemical. The oxide under the exposed areas is etched. In this way an opening is made in the oxide.

The photoresist is stripped, because it is organic and cannot withstand the following furnace steps.

Dopant is implanted into the silicon for the base. The areas where oxide is not opened are protected by the oxide.

After the base is implanted, it is driven in by the base diffusion. The base diffusion grows a thermal oxide in the opening to structure the emitter.

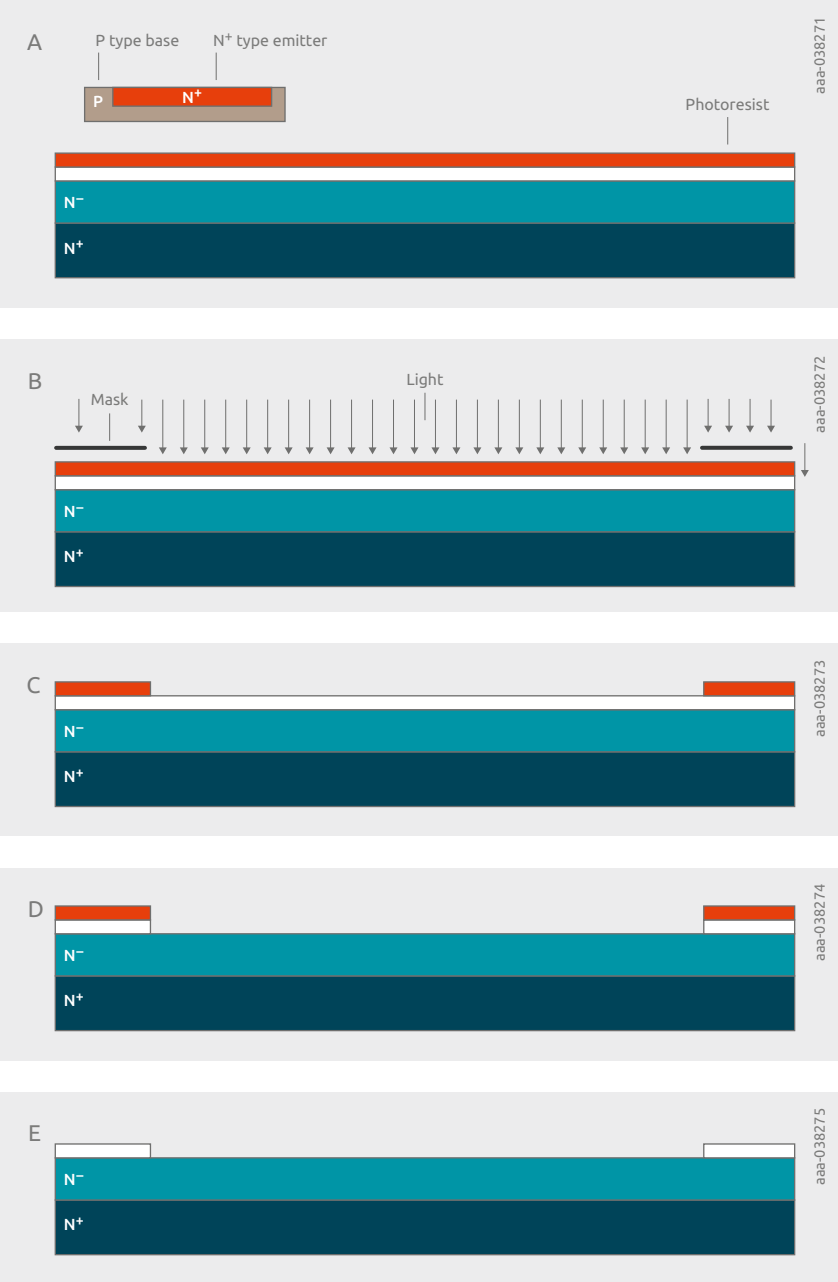


Figure 3 | A) Photoresist on oxide; B) photoresist exposure with mask; C) exposed photoresist on oxide; D) etched oxide; E) etched oxide after resist strip

An opening for the emitter is made in the oxide by photolithography and etching.

The emitter is made with an N+-type implant and driven to the desired depth so that a base remains under the emitter, and an emitter oxide is grown.

The emitter and base contacts are opened in the oxides and metal is sputtered onto the die surface and shaped by lithography and etching to form base and emitter contacts.

A passivation layer is deposited on the chip. This is to keep charges away from the die surface and to provide scratch protection.

Openings are etched in the passivation layer for the bond pads, where the bond wires will connect the die to the package during assembly.

Now the wafers are ground back to give the wafer the desired final thickness.

To attach the die during assembly, so that the back of the die is connected to the package, metal is spattered onto the wafer back. This metal should provide:

- a good contact to the silicon substrate
- a diffusion barrier to prevent unwanted metals diffusing into the die
- a metal toward the die that can either be glued, eutectically attached or soft-soldered.

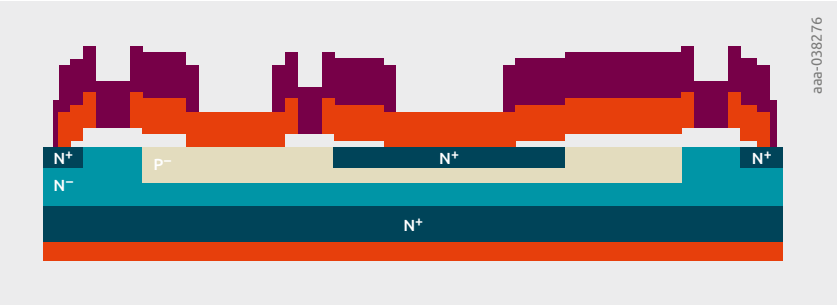


Figure 4 | Thinned wafer with metal back

2.2.2 Types of discrete bipolar transistors

While all of Nexperia's bipolar junction transistors (BJTs) follow the same scheme of a vertical device with a collector as the die backside and a base and emitter on top, there are several classes of BJTs which target different applications. All of the different types are designed for best performance, however, as in daily life, everything is a tradeoff.

General-purpose transistors

The name "general-purpose transistor" is self-explanatory. It is a transistor that suits all conditions. All parameters are in the middle, fitting most applications. If your application has no specific demands relating to certain parameters, this category of transistor will be good for you, offering the best balance between performance and cost. The parameters listed in the data sheet will usually have a certain tolerance in terms of specifications.

Some examples of general-purpose transistors are the BC series, such as the BC847/BC857 family (100 mA, 45 V, SOT23), the BC807/BC817 family (500 mA, 45 V, SOT23) or the BCP5x family (1 A, 45 to 80 V, SOT223).

As well as the common SMD packages (e.g., SOT23), general-purpose transistors are also available in more advanced or power-oriented packages. For example, the BC5xPAS series (1 A, 45 to 80 V) in DFN2020D-3 package with visible and solderable side pads, or in the power segment the MJD series in DPAK (e.g., MJD31CA – 3 A, 100 V, NPN).

Low V_{CEsat} transistors/high-power transistors

This class of BJTs is designed to have a low voltage drop during operation. A typical tradeoff is the breakdown voltage of the transistor. Specifications in the data sheet target the V_{CEsat}/R_{CEsat} performance of the device and are more detailed for this parameter.

Minimizing the typical values of V_{CEsat} can incur extra cost, for example when using more wires or a larger silicon area. It is quite common that types with high collector current ratings have the lowest typical V_{CEsat} values. These types of devices are made for applications requiring low power consumption, such as LDOs.

Low-V_{CEsat} transistors are available in a wide range of packages, such as standard SMD packages, more advanced DFN packages or even more power-oriented packages.

Most of the low-V_{CEsat} BJTs include "PBSS" in the name. Prominent examples are PBSS5240T (2 A, 40 V, PNP, SOT23) or PBSS4350T (3 A, 50 V, NPN, SOT23). These two come in SOT23 SMD package, but are also available in SOT457, SOT89 or SOT223.

A more power-oriented series of the low-V_{CEsat} transistors is the PHPT series in LFPAK56, for example with PHPT61003NY (3 A, 100 V, NPN) or PHPT60415PY (15 A, 40 V, PNP). Moreover, the PHPT series is also available as double transistors in LFPAK56D, such as PHPT610030NPK (3 A, 100 V, NPN/PNP).

High-voltage transistors

The family of high-voltage transistors starts at Nexperia with more than 100 V breakdown voltage for the emitter-collector range.

This family of transistors features special techniques to guarantee capability of withstanding high reverse voltages on the emitter-collector range and base-collector range. The emitter-collector range typically withstands 6 to 9 V in reverse. A typical tradeoff for these kinds of transistors is the V_{CEsat} performance or the current gain.

At Nexperia, high-voltage transistors are available as general-purpose high-voltage transistors, such as PMBTA42 (100 mA, 300 V, NPN) or as a low-V_{CEsat} high-voltage transistor, such as PBHV8540T (500 mA, 400 V, NPN, SOT23), PBHV8560Z (500 mA, 600 V, NPN, SOT223) or PBHV9040X (250 mA, 500 V, PNP, SOT89).

Switching transistors

For applications that require a fast-switching transistor, Nexperia offers several transistors with optimized switching times. The provision of fast switching usually comes at the expense of V_{CEsat} performance. Moreover, the current gain at low collector currents can be reduced.

At Nexperia the switching transistors have "PMBT" or "BSR" in the name, but there are also some types of the PBSS family that include features to improve the switching. Common examples are PMBT3904 (200 mA, 40 V, NPN, ton = 70 ns, toff = 250 ns) and PMBT3906 (200 mA, 40 V, PNP, ton = 70 ns, toff = 300 ns) or PMBT2222A (600 mA, 40 V, NPN, ton = 35 ns, toff = 250 ns) and PMBT2907A (600 mA, 60 V, PNP, ton = 40 ns, toff = 365 ns). From the PBSS family the PBSS4032NZ (4.9 A, 30 V, NPN, ton = 65 ns, toff = 215 ns) and PBSS4032PZ (4.4 A, 30 V, PNP, ton = 90 ns, toff = 220 ns) are examples of low-V_{CEsat} transistors with optimized switching times.

Matched pair BJTs

Nexperia's bipolar product portfolio offers many dual BJTs - two transistors assembled in one package. This comes with the advantage of saving mounting space on a PCB as well as providing two transistors which are closely coupled thermally, ideal for applications with a symmetrical design. For a precise operation of these applications, closely matched current gains (h_{FE}) are beneficial. The same is true for the V_{BE} characteristics of the two BJTs. During production, BJTs can exhibit a wide range of current gains. To guarantee almost identical current gains, Nexperia provides matched pair transistors. The dies used for these products are picked from a single wafer at an adjacent location in the assembly process, making it very likely that the two BJTs are matched very well. The last phase of testing involves verifying that the values of the following parameters fall within a narrow target window:

- h_{FE} matching: $h_{FE}1/h_{FE}2$ 2 % -10 % accuracy, depending on the type
- V_{BE} matching: V_{BE1}-V_{BE2} <= 2 mV

Designs that benefit from the symmetry of matched pair BJTs, like current mirrors, differential amplifiers, comparators, and current sensing circuits, are discussed in detail in the application section of this handbook (chapter 7). Thermal shift is significantly reduced and compensated thanks to the thermal coupling of the BJT pair assembled into a single package such as SOT363 or SOT467. If needed, a designer can easily decide to improve the performance of a circuit by replacing two standard BJTs with a matched pair type with identical pinning.

2.2.3 Types of complex bipolar transistors

Resistor-equipped BJTs

Bipolar junction transistors (BJTs) are generally applied with one or more resistors for biasing and to work with voltage input instead of current input.

The most basic configuration is a resistor in front of the base. In addition to biasing, this also limits the input current and protects the device.

Adding a second resistor between base and emitter provides a voltage divider to set the bias. This R2 also stabilizes the current gain of the internal transistor and thus keeps the operating point more stable.

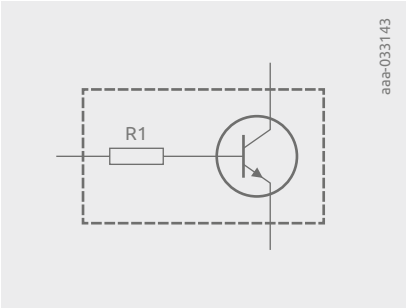


Figure 1 | Bipolar transistor with base resistor only

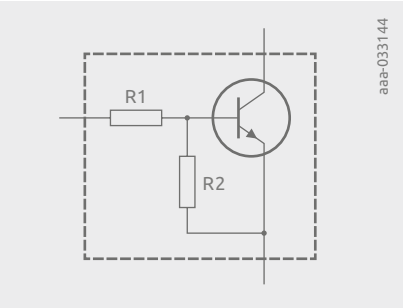


Figure 2 | Bipolar transistor with base and base-emitter resistor

Nexperia's resistor-equipped transistor (RET) family integrates one or two resistors with general-purpose BJTs to reduce component count, keep pick-and-place time down and reduce the PCB area used.

Nexperia RETs are available in single and double configuration in SMD leaded and DFN leadless packages.

The RETs are available with either 100 mA or 500 mA output current and in NPN or PNP polarities.

The internal transistors of the 100 mA RETs is equivalent to the BC847B (NPN) or BC857B (PNP).

The 100 mA family has standard parts, with 50 V emitter-collector breakdown voltage and higher specified parts with 80 V V(BR)CEO. The 80 V devices are intended for the 48 V automotive board net and also offer some extended specifications.

The 500 mA RET family uses internal transistors similar in performance to the BC807-25 (PNP) or BC817-25 (NPN).

Nexperia offers a 600 mA RET family with increased specifications. These performance-based RETs are a close relations of the 500 mA RETs, but have a much higher current gain and an increased output current of 600 mA with a lower minimum breakdown voltage V(BR)CEO of 40 V.

The poly-Si resistors have much higher tolerances than metal film resistors. For that reason, the RETs are most commonly used for switching applications where they operate in the on- or off-state. This is why RETs are often referred to as digital transistors.

Construction of internal resistors

Polysilicon is used for the internal resistors of RETs. The resistor process is integrated in the BJT fabrication after the emitter processing is finished. At first, an oxide is deposited to insulate the resistors from the BJT. Then, 0.55 µm poly-Si is deposited, doped and annealed. Finally, the normal BJT process flow is followed again.

The doping materials are phosphorus for 150 mm and boron for 200 mm. The following sections describe the properties of the poly-Si resistors.

Nexperia and most competitors use a polysilicon sheet resistance of 1 kΩ per square. That means you have to add 10 poly-Si squares for a resistance of 10 kΩ. Or in other words, the length-to-width ratio of this resistor would be 10:1.

The following graph shows the layout and the cross-section of a 100 mA PNP RET:

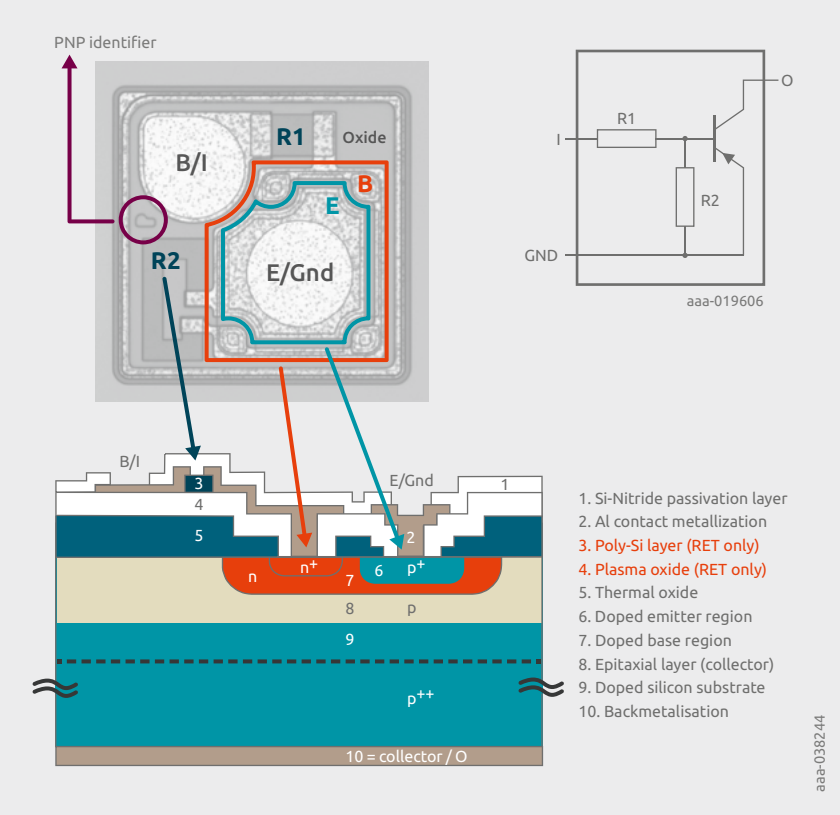


Figure 3 | RET construction, top view and cross-section

Resistor linearity

The resistor linearity for R1 over the allowed input voltage range depends on different factors such as doping material, sheet resistance and poly-Si cross-section area. This will be described below in more detail.

Doping material: The standard doping for n-type is phosphorus, and for p-type boron is most commonly used for poly-Si resistors. Boron (blue) doped resistors are more linear over input voltage than phosphorus (red) doped ones.

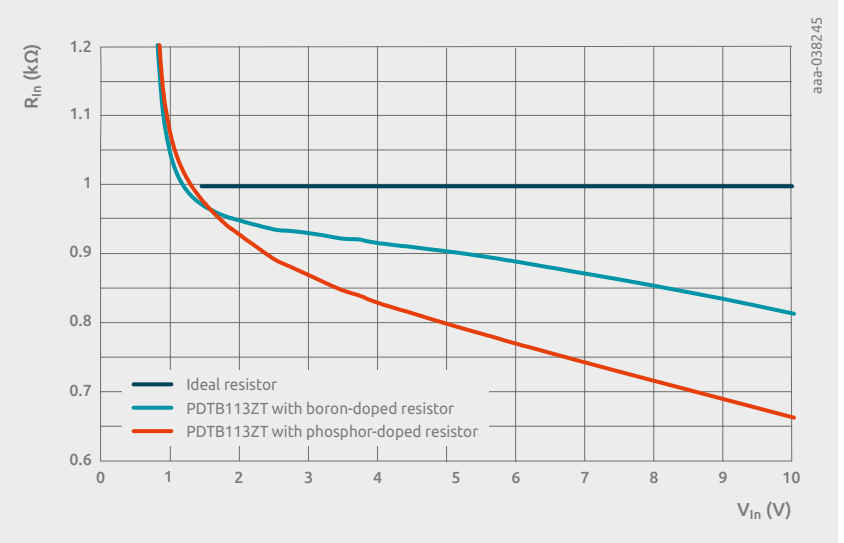


Figure 4 | Resistor linearity over input voltage range

The variation of resistance over input voltage for different sheet resistances is shown in the following table. The resistances are shown normalized, as the same resistor layout was used for all trial parts and the absolute resistance varied according to sheet resistance.

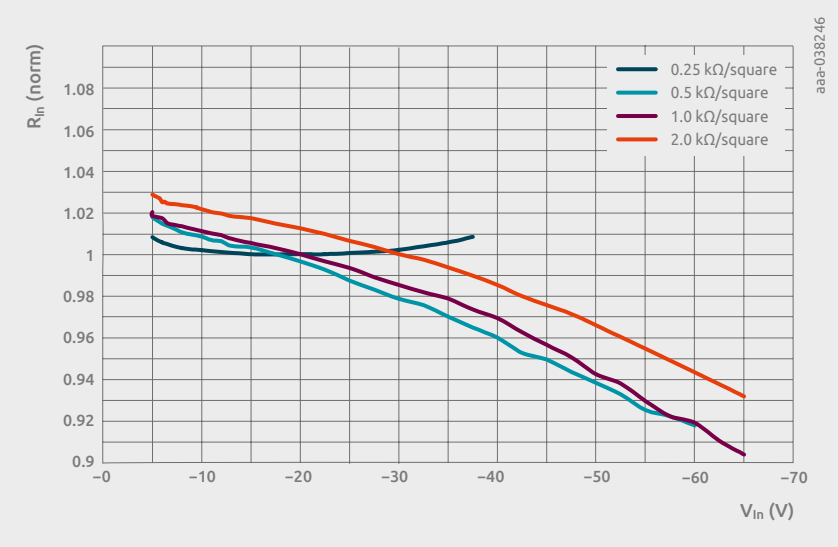


Figure 5 | Polysilicon sheet resistance as a function of input voltage

The next parameter affecting the linearity is the resistor cross-section. But as thickness is constant within the RET portfolio, the width is the relevant design factor here.

The graph below compares the standard 100 mA/50 V RET with R1 = 22 kΩ (PDTC124ET) to the 100 mA/80 V RET with the same R1 (NHDTC124ET). The poly-Si width of the resistor in the 80 V RET is 2.3 times that of the standard 50 V RET.

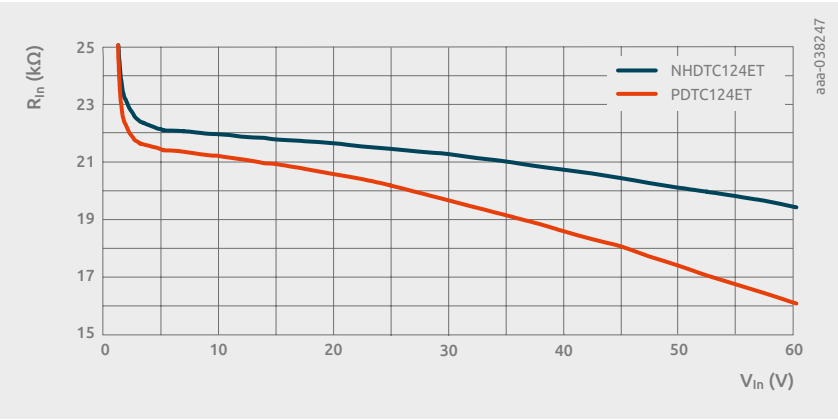


Figure 6 | R1 plotted as function of input voltage for NHDTC124ET and PDTC124ET

Thermal dependence of resistance

In addition to the non-linearities over the input current, the poly-Si resistance is also influenced by the operating temperature.

At fixed resistor test conditions, the temperature dependence can be described with a second-order Taylor series:

$$R(T) = R(T_0) \times (1 + \alpha \times (T - T_0) + \beta \times (T - T_0)^2)$$

For Nexperia RETs, the constants are as follows for 150 mm RETs with phosphorus doping and the 200 mm RETs with boron doping:

Table 1. Constants for Nexperia's 150 mm RETs with phosphorus doping and 200 mm RETs with boron doping

	α	β
Phosphorus-doped Poly-Si	−0.00229	7.26 × 10E-6
Boron-doped Poly-Si	−0.00161	3.7275 × 10E-6

The following graph plots the two Taylor series of resistance vs. temperature for boron- and phosphorus-doped poly-Si resistors. The y-axis shows the resistance normalized to the room-temperature resistance.

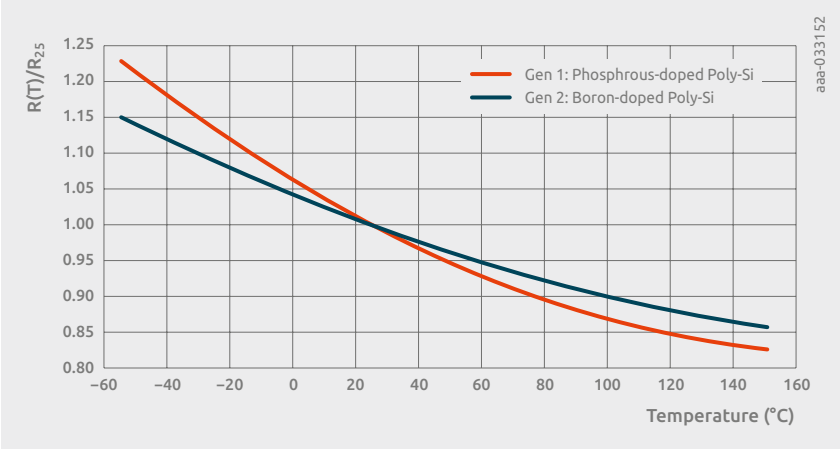


Figure 7 | Poly-Si resistance as function of operating temperature for boron- and phosphorous-doped poly-Si.

ESD/EOS influence of poly-Si resistors

Poly-Si has a lower maximum current rating than external resistors. Nexperia qualified a continuous current density of 0.8 mA/µm² for its poly-Si with a 1000 h operating life test for Gen 1 and Gen 2 RETs.

The resistors in Nexperia's RETs are designed to keep the current density below 0.8 mA/µm² at the maximum allowed input voltage.

Electrical overstress (EOS) or electrostatic discharge (ESD) greater than 0.8 mA/µm² causes damage to the poly-Si of the base resistor. The extent of the damage is proportional to the strength of the ESD/EOS. An analysis of the fails shows a discolored, low-ohmic path within the poly-Si that is causing the resistance to fall below the specifications. Even higher discharge voltages cause more damage to the R1 resistor and lead at some stages to total destruction of the resistor.

The following pictures of RETs after 1 kV and 2 kV ESD pulses according to Human Body Model (HBM) specifications show the increased damage at increased stress.

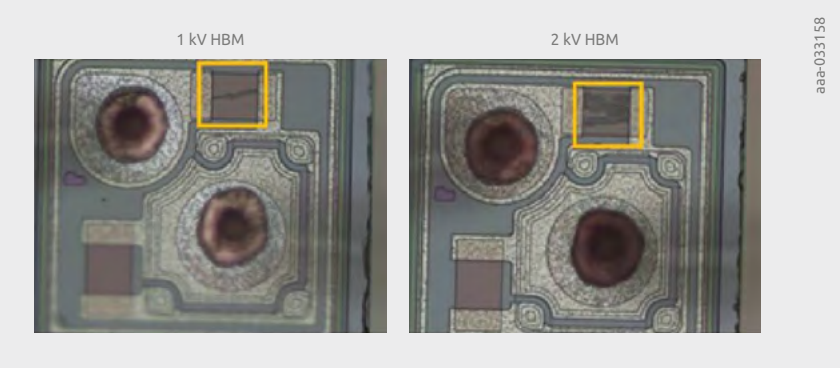


Figure 8 | PDTA113ET after 1 kV and 2 kV ESD pulses according to HBM specifications

All Nexperia RETs are qualified for ESD (HBM) class H1B (≥500 V, <1000 V).

Tolerance of poly-Si resistors

The tolerance of base resistor R1 is ±30% at the testing conditions (see section "Testing of R1 and R2/R1 ratio") and not over the full temperature and input voltage range due to the poly-Si non-linearities.

The ±30% tolerance is based on the poly-Si module process spreads: poly-Si sheet resistance, poly-Si etching, metal contact etching.

Influence of resistors on device characteristics

The following section describes in detail the characteristics of the complete RET, derived from the characteristics of the resistors and the base-emitter and base-collector diodes.

RET with R1 only

The first case is a RET with an R1 only. The example shown is an NPN device. Looking at the circuit between input I and ground GND, we have the resistor R1 in series with the base-emitter diode.

The input current is constant and the input voltage is divided into V1 across R1 and V_{BE} across the B-E diode, as shown below:

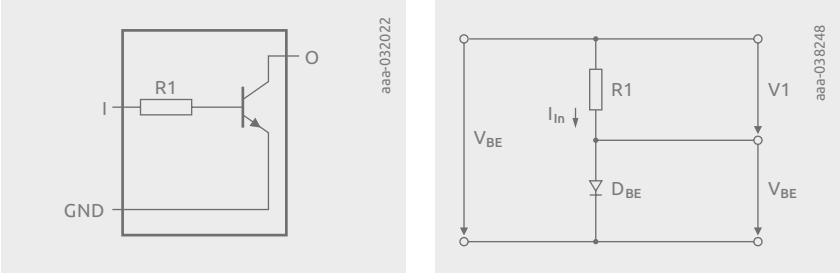


Figure 9 | RET with R1 only: equivalent circuit for input to gound

The characteristics of the equivalent circuit can now be derived from the characteristics of the two devices. As the current is the same in both devices, the voltages V1 and V_{BE} at a given current can be added up to obtain VIN.

$$V_{IN}\,(\times mA) = V_1\,(\times mA) + V_{BE}\,(\times mA)$$

The characteristics of R1 and of the B-E diode of the built-in transistor are shown below for an R1 of 4.7 kΩ:

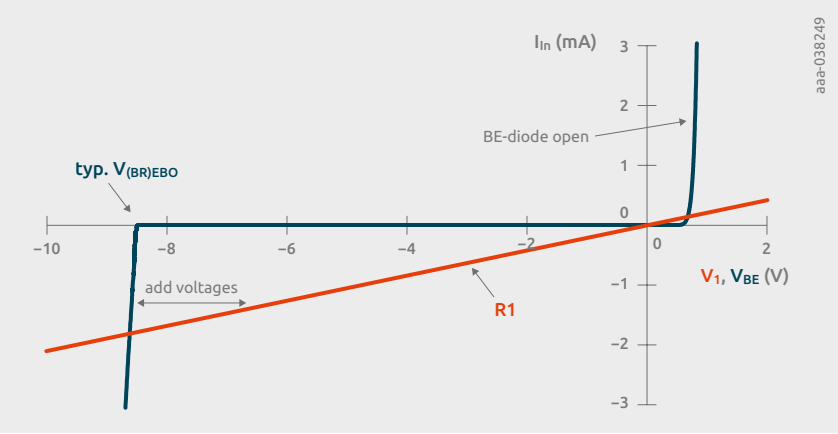


Figure 10 | Characteristics of R1=4.7kΩ and the B-E diode of the built-in transistor

The characteristics of the input voltage vs. the input current to ground then look like this:

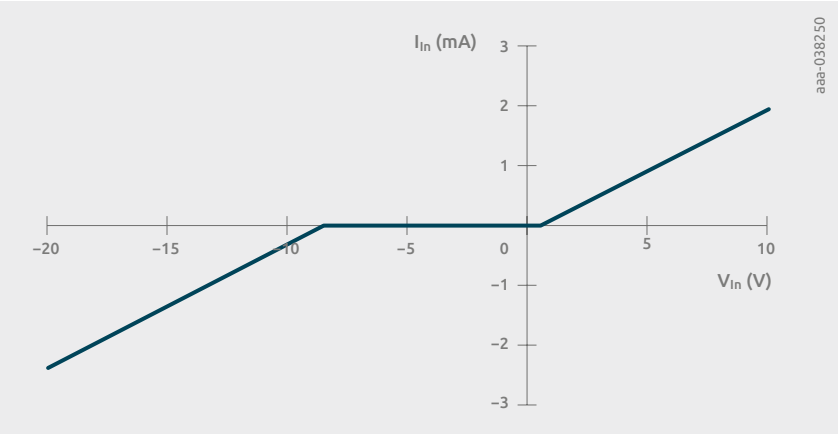


Figure 11 | Input voltage vs. input current to ground

It is basically the B-E diode characteristic with R1 acting as current limiter, when the diode opens or is in breakdown mode.

The circuit between input and output behaves identically, now with R1 in series with the base-collector diode as shown in Figure 12.

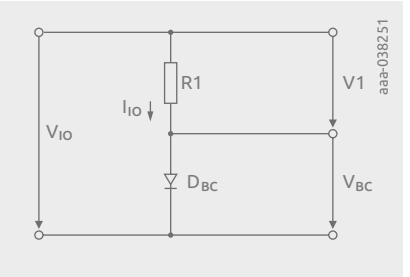


Figure 12 | RET with R1 only: equivalent circuit for input to output

RET with R1 and R2

Calculating the characteristics of the input circuit of a RET with two resistors involves a step more than in the case of a device with R1 only.

The input circuit now consists of a parallel circuit of R2 and the B-E diode, which is in series with R1 as shown in Figure 13.

For the derivation of the device characteristics, we will have to start with the parallel circuit of R2 and the B-E diode. The voltage drop V2 across both devices is the same and the input current for a fixed V2 can be calculated by adding the currents I2 and IB at that voltage as shown in Figure 14.

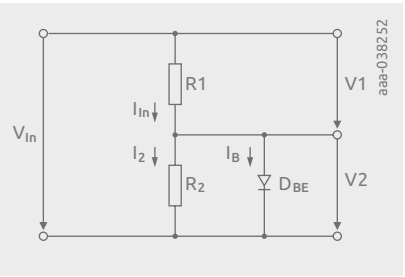


Figure 13 | Equivalent circuit from input to ground of RET with two resistors

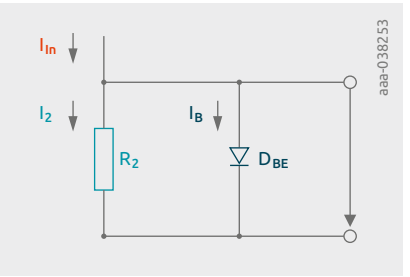


Figure 14 | Schematic for base-emitter diode with parallel Resistor R2

$$I_{In}(\times V) = I_2(\times V) + I_B(\times V)$$

The following example calculations are now shown for an NPN RET with an R1 of 4.7 kΩ and an R2 of 10 kΩ. The following graph shows the characteristics of the B-E diode and the R2:

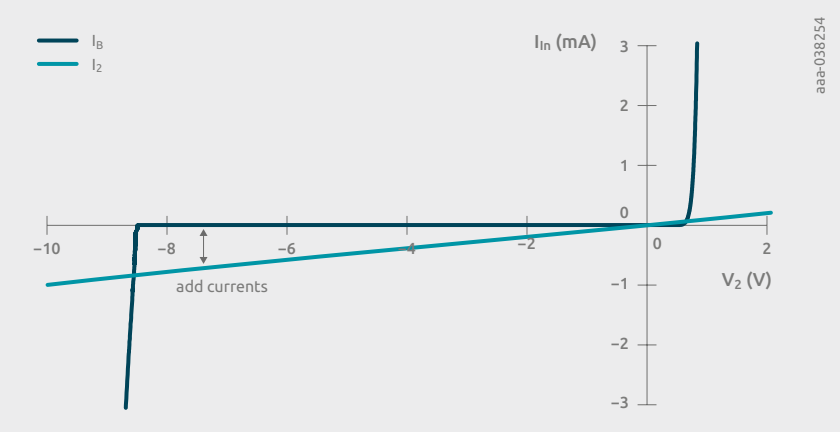


Figure 15 | Characteristics of the B-E diode and R2=10kΩ

Adding the currents of the devices for each voltage yields the following characteristics of the equivalent circuit of the paralleled devices:

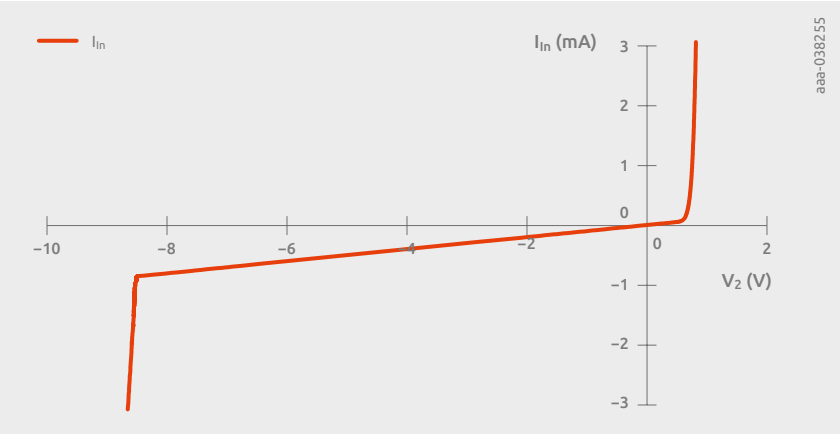


Figure 16 | Characteristics of the equivalent circuit of the paralleled devices

The combination of R2 and DBE shows the diode characteristics, when the diode opens or is in breakdown. Here, the diode has a much lower resistance than R2, and R2 can basically be neglected.

At voltages between the typical breakdown voltage $V_{(BR)EBO}$ and the forward voltage of approximately 0.7 V, the diode is blocking and has a much higher resistance than R2. Here, the diode resistance can be neglected and the current/voltage slope is proportional to R2.

Now, the equivalent circuit for R2 // DBE will be combined with the input resistor R1 to obtain the RET input characteristics.

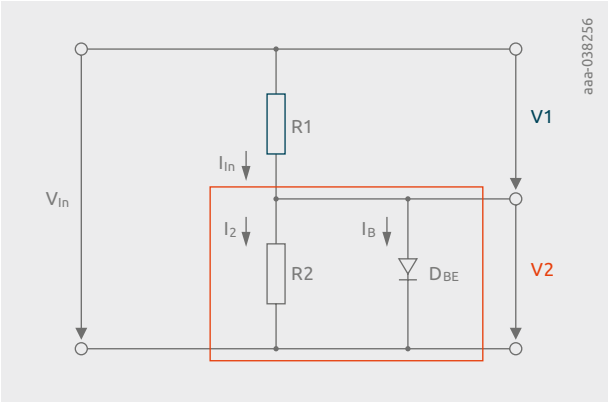


Figure 17 | Equivalent circuit for R2 // DBE combined with the input resistor R1

As this is a series circuit with a constant input current, the voltage drops over R1 and the equivalent circuit for R2 and DBE can be added at a given current:

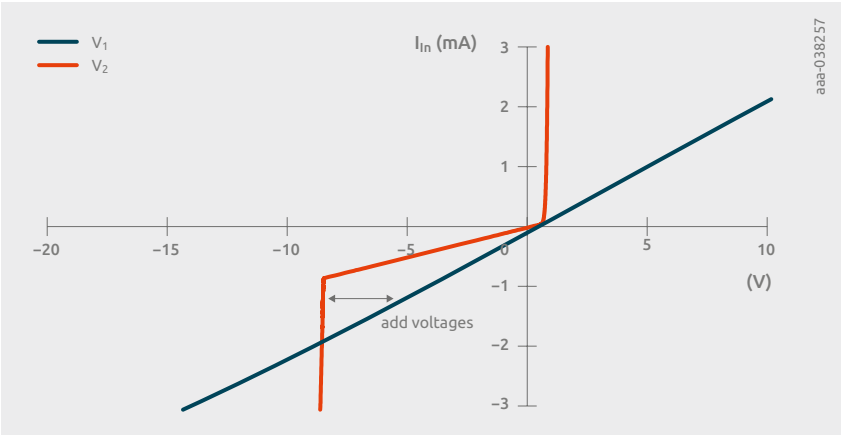


Figure 18 | Current-Voltage characteristics of R1=4.7kΩ and equivalent circuit for R2=10kΩ and DBE added at a given current

The complete input characteristics now show again the current limiting of R1, when the B-E diode is in breakdown or open.The breakdown of the device occurs at a higher voltage than the typical breakdown voltage $V_{(BR)EBO}$ of the diode because of the voltage divider formed by R1 and R2.

When the diode is in blocking mode, its resistance can be neglected, as it is much higher than R2. Now, there are only the two resistors in series and the slope of the IIN to VIN curve is proportional to R1 + R2.

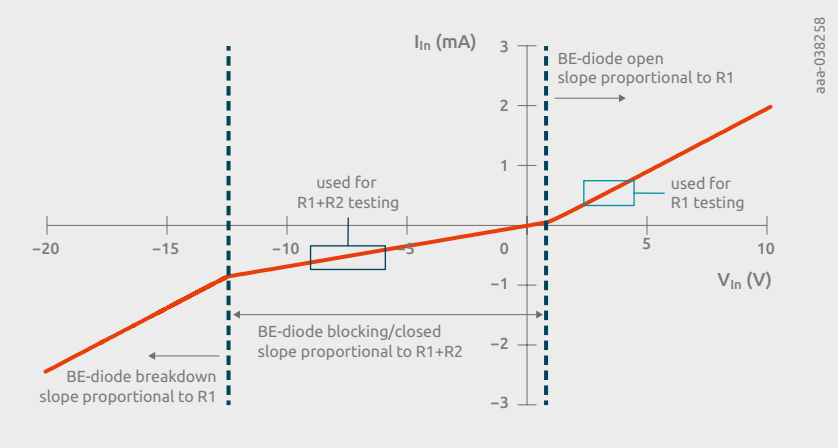


Figure 19 | Input characteristics of PDTC143XT

Resistor testing is described in more detail in Section "Testing of R1 and R2/R1 ratio", but the areas used are marked in the Figure above. R1 has to be tested by the voltage delta divided by the current delta, as the slope is offset by the 0.7 V forward voltage of the B-E diode. In reverse blocking mode, two points are also tested for the resistor ratio calculation.

A plot of the calculated input resistance of the device (ΔV_{In} / ΔI_{In}) for the RET shows this more clearly. In blocking mode, the input resistance equals R1 + R2. In breakdown or open mode, the input resistance is equivalent to R1.

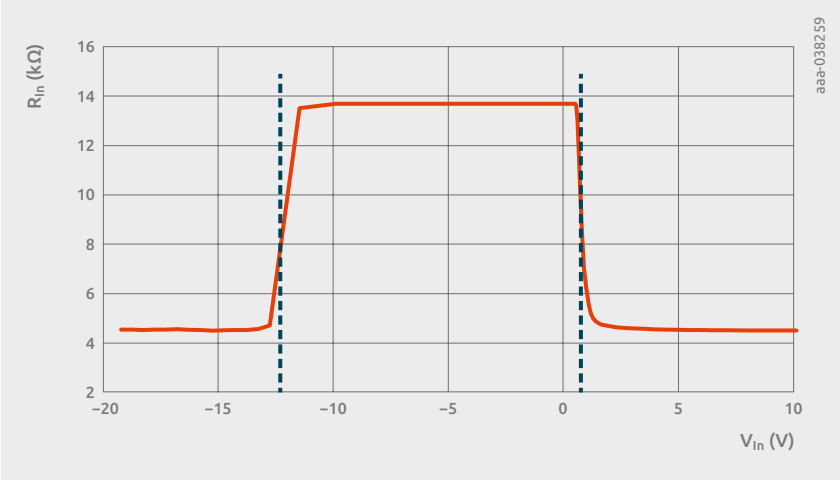


Figure 20 | Calculated input resistance as a function of input voltage

Data sheet parameters

The following sections describe the naming and most important data sheet parameters of the RETs.

Type naming and resistor portfolio

The resistor portfolio starts at 1 kΩ and has a maximum value of 100 kΩ. The resistor values in between are chosen according to the E3 series (IEC 60063) because the tolerance is in the range >20% to ≤40%.

The following table shows the resistor combinations offered by Nexperia; the meaning of the two numbers and the letter is explained in Tables 3 and 4:

Table 2. Resistor combination overview

R2 (kΩ) \ R1 (kΩ)	1	2.2	4.7	10	22	47	100
open		23T	43T	14T	24T	44T	15T
1	13E						
2.2		23E					
4.7			43E				
10	12Z	23Y	43X	14E		44V	
22					24E	44W	
47		23J	43Z	14Y	24X	44E	
100							15E

500 mA family | **100 mA family**

The naming of the single RETs follows the quasi industry standard for the resistor combinations, so it is easy to derive the resistor combinations, polarity and collector currents from the type names. The last letter(s) always indicate the package used.

Table 3 explains the type naming in detail.

Table 3. Nomenclature of single RETs

1st letter Company Indicator	2nd letter Voltage Indicator	2nd/3rd letter	5th letter Polarity and Current	1st number	Base number for R1	Multiplier for R1	Resistor ratio R2/R1	Package Indicator
N= Nexperia	H= high voltage	DT= digital transistor	A=PNP <500 mA	1= no meaning	1=1	3=x 10E3	T=R1 only	T=SOT23
P= Philips (legacy)		R=RET	B=PNP ≥500 mA		2=2.2	4=x 10E4	E=1 R1=R2	U=SOT323
PB= performance based			C=NPN <500 mA		4=4.7	5=x 10E5	V=0.213	M=SOT883
			D=NPN ≥500 mA		Comp. only:	Comp. only:	W=0.46	MB=SOT883B
			N=NPN ≥500 mA		3=3.3	2=x 10E2	X=2.13	QA=SOT1215
			P=PNP ≥500 mA		5=5.6		Y=4.55	QB=SOT8015
							Z=10	QC=SOT8009

Table 4. Nomenclature of double RETs

1st letter Company Indicator	2nd letter Voltage Indicator	3rd letter Package Indicator	4th letter	5th letter Polarity and Current	Number(s)	Trailing letters
N= Nexperia	H= high voltage	I=SOT457	M= no meaning	B=2 x PNP <500 mA	Consecutive numbering	—
P= Philips (legacy)		I+trailing letters		C=NPN/PNP ≥500 mA		PA=SOT1118 PAS-Q=SOT1118D
		U=SOT363		D=NPN/PNP <500 mA		—
		E=SOT666		H=2 x NPN <500 mA		—
		Q=SOT1216		N=2 x NPN ≥500 mA		—
		R=SOT1268		P=2 x PNP ≥500 mA		—

For double RETs, it is not possible to derive the resistor combination from the name. Here, a consecutive numbering of the types is used.

However, polarity, current and package are represented in the naming, as can be seen in the Table 4.

Testing of R1 and R2/R1 ratio

All RET data sheets published after 2015 contain the resistor test conditions in the chapter "Test Information" right after the typical curves. Figure 19 shows the input IIn vs. VIn characteristics, and indicates in which area/operating state the resistor measurements are done. The following section shows the data sheet test information for the PIMN32PAS-Q (R1 = 2.2 kΩ, R2 = 10 kΩ) double 500 mA/50 V RET in DFN2020D-6 (SOT1118D).

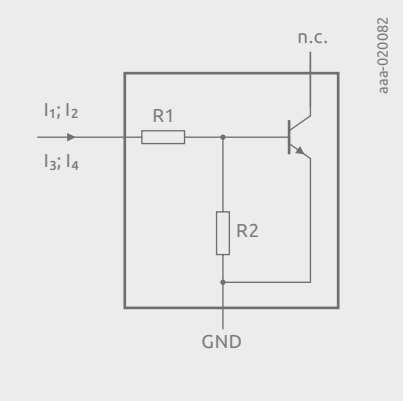


Figure 21 | NPN RET: Resistor test circuit

The following Figure shows the device under test:

I_1 and I_2 are always measured in forward bias conditions and are used to calculate R1:

$$R1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

The resistor R2 cannot be measured directly, so the data sheet includes the resistor ratio R2/R1 instead. Please note that some competitors specify the inverse ratio R1/R2.

I_3 and I_4 are always measured in reverse bias conditions and are used to calculate the bias resistor ratio R2/R1 together with the R1 result:

$$\frac{R2}{R1} = \frac{V(I_4) - V(I_3)}{R1 \cdot (I_4 - I_3)} - 1$$

Here is an example table with the test conditions from the PIMN32PAS-Q data sheet:

Table 5. Test conditions for PIMN32PAS-Q

PIMN32PAS-Q	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I1	I2	I3	I4
TR1/TR2 (NPN)	2.2	10	0.7 mA	0.8 mA	−0.45 mA	−0.55 mA

R1 Resistor value and tolerance

The minimum and maximum resistor ratings are at the test conditions stated in the data sheet and at room temperature. For R1, the tolerance is ±30% and the minimum and maximum resistance can be calculated as follows:

$$R1_{min} = (1 - tolerance_{R1}) \cdot R1_{typ} = (1 - 30\%) \cdot R1_{typ}$$

$$R1_{max} = (1 + tolerance_{R1}) \cdot R1_{typ} = (1 + 30\%) \cdot R1_{typ}$$

Resistor ratio R2/R1 and tolerance

For the resistor ratio, the tolerance is either ±20% (for 100 mA RETs) or ±10% (for ≥ 500 mA RETs). The tolerance for R2 can be calculated from the tolerances of R1 and R2/R1:

$$R2_{min} = R1_{min} \cdot \frac{R2}{R1_{min}} = (1 - tolerance_{R1}) \cdot R1_{typ} \cdot (1 - tolerance_{R2/R1}) \cdot \frac{R2}{R1_{typ}}$$

$$R2_{min} = (1 - tolerance_{R1}) \cdot (1 - tolerance_{R2/R1}) \cdot R2_{typ}$$

$$R2_{max} = (1 + tolerance_{R1}) \cdot (1 + tolerance_{R2/R1}) \cdot R2_{typ}$$

With an R1 tolerance of 30% and an R2/R1 tolerance of 20%, the minimum and maximum values of R2 are $0.56 / 1.56 \times R2_{typ}$.

For an R2/R1 tolerance of 10%, the minimum and maximum values of R2 are $0.63 / 1.43 \times R2_{typ}$.

Power dissipation

The power dissipation of a BJT is the sum of the input power dissipation between base and emitter and the output power dissipation between collector and emitter. For RETs, the power loss in the two resistors has to be added to the input power.

$$P_{tot} = P_{R1} + P_{R2} + P_{BE} + P_{CE} =$$

$$\frac{(V_{In} - V_{BE(fwd)})^2}{R1} + \frac{V_{BE(fwd)}{}^2}{R2} + I_B \cdot V_{BE(fwd)} + I_C \cdot V_{CE}$$

PR2 can be neglected, as it is only 0.5 mW in the worst case for R2 = 1 kΩ.

PBE is also comparatively small; with an R2 of 1 kΩ it is 6.5 mW.

PCE is strongly dependent on the collector current. With the transistor in saturation at a V_{CE} = 0.3 V, the power dissipation would be between 1.5 mW at I_C = 5 mA and 150 mW at an I_C of 500 mA.

P_{R1} is in a similar range to PCE. At the maximum input voltage per type, it ranges from 15 mW (R1 = 100 kΩ, V_{IN} = 40 V) to 183 mW (R1 = 4.7 kΩ, V_{IN} = 30 V). Due to the poly-Si nonlinearities described in sections "Resistor linearity" and "Thermal dependence of resistance", the typical resistance at the highest input voltage is lower than the nominal resistance of each type. That means the real power dissipation P_{R1} is higher than the examples mentioned here.

So, the simplified equation below gives a good enough approximation of the RET P_{tot} at higher collector currents (and the necessary higher input voltages to drive these currents):

$$P_{tot} \approx P_{R1} + P_{CE} = \frac{(V_{In} - V_{BE(fwd)})^2}{R1} + I_C \cdot V_{CE}$$

Breakdown voltages

Two of the three breakdown voltages of the RET are influenced by the resistors.

The breakdown voltage $V_{(BR)CEO}$ between output and ground is the same as that of the built-in transistor and is not affected by the resistors.

The test current is usually 2 mA for transistors with an I_C (DC) of 100 mA or less and 10 mA for all other types.

Please note that the "O" in $V_{(BR)CEO}$ stands for "open" and refers to the third pin not mentioned in the name, in this case the base. So $V_{(BR)CEO}$ reads as breakdown voltage beween collector and emitter, base open. The "S" in $V_{(BR)CES}$ stands for a short between the last named pin and the not-named pin, so between emitter and base. And the "R" at the end of $V_{(BR)CER}$ stands for "resistor", so there is a resistor between emitter and base.

The breakdown voltage $V_{(BR)CBO}$ between input and output is slightly higher than the $V_{(BR)CBO}$ of the built-in transistor because of the voltage-drop over R1:

$$V_{(BR)CBO\ RET} = V_{(BR)CBO\ Built-in\ transistor} + I_C \cdot R1$$

The test current is always 100 µA for all Nexperia BJTs.

The emitter-base breakdown voltage $V_{(BR)EBO}$ between input and ground is influenced by the resistors as well. If the RET has only an R1, it behaves similarly to $V_{(BR)CBO}$, as can be seen in Figure 12:

$$V_{(BR)EBO\ RET} = V_{(BR)EBO\ Built-in\ transistor} + I_B \cdot R1$$

If the RET has two resistors, the breakdown voltage $V_{(BR)EBO}$ is influenced by the resistor ratio. In the reverse direction, the resistance of the blocking base-emitter diode is so much higher than the parallel resistor R2 that it can be neglected and only R2 is considered:

$$\frac{V_{(BR)EBO\ RET}}{V_{(BR)EBO\ Built-in\ transistor}} = \frac{R1+R2}{R2} = \frac{R1}{R2} + 1 = \frac{1}{\frac{R2}{R1}} + 1$$

$$V_{(BR)EBO\ RET} = V_{(BR)EBO\ Built-in\ transistor} \cdot \left(\frac{1}{\frac{R2}{R1}} + 1\right)$$

The absolute value of $V_{(BR)EBO}$ is also the maximum allowed input voltage in reverse operation. Only the sign changes, because V_{Input} is defined as voltage drop between input and ground, therefore reversing the two pins compared to the $V_{(BR)EBO}$ measurement.

The emitter-base (open) breakdown voltage of the built-in transistor is 5 V maximum for the standard RETs and 7 V maximum for the 80 V/100 mA RETs.

Leakage currents

Collector-base and collector-emitter leakage currents I_{CBO} and I_{CEO} are not affected by the resistors and are typically in the single digit nA range at room temperature and have a maximum limit of 100 nA.

The emitter-base leakage current between input and ground pins depends on the resistor configuration. If the RET has no R2, the leakage current is that of the blocking base-emitter diode and is in the nano-ampere range. If an R2 is present, the high-ohmic reverse biased base-emitter diode is bypassed by this base-emitter resistor and can be neglected. So, here we have a current defined by the voltage drop over the two resistors i.s.o. a leakage current:

$$I_{EBO} = \frac{V_{EB}}{R1+R2}$$

V_{EB} is the reverse input voltage in this case.

The maximum limit of this current can be calculated with the V_{EB} test condition and the minimum allowed resistor values:

$$I_{EBO(max)} = \frac{V_{EB}}{R1_{min} + R2_{min}}$$

$$I_{EBO(max)} = \frac{V_{EB}}{(1 - tolerance_{R1}) \cdot R1_{typ} \cdot \left(1 + (1 - tolerance_{R2/R1}) \cdot \frac{R2}{R1_{typ}}\right)}$$

This current is in the range of micro- to milliamperes depending on the resistor values.

Current gain

The current gain of a RET is influenced by the size of the R2. The R2 in parallel with the base-emitter diode acts as a leakage path and reduces the part of the input current that is available for driving the transistor:

$$I_B = I_{In} - I_{R2} = I_{In} - \frac{V_{BE(forward)}}{R2} \approx I_{In} - \frac{0.7V}{R2}$$

So, the minimum input current needed to turn the transistor on is:

$$I_{In} > \frac{V_{BE(forward)}}{R2} \approx \frac{0.7V}{R2} = I_{B(min)}$$

IB(min) ranges from 7 µA (R2 = 100 kΩ) to 700 µA (R2 = 1 kΩ).

Therefore, a RET with a small R2 with high leakage current has lower current gain than a RET with a higher R2. This is visualized in the following graph. It compares types with an R1 of 4.7 kΩ and different R2s to the built-in transistor and a RET with R1 only.

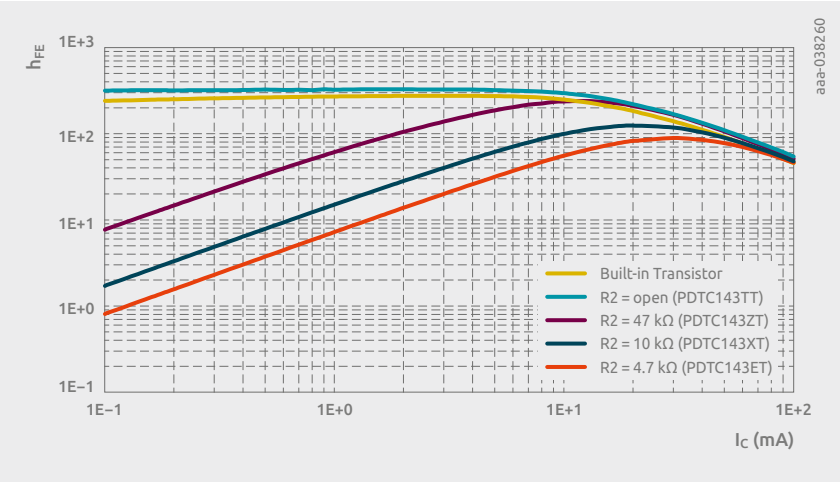


Figure 22 | h_{FE} as a function of I_C, V_{CE} = 0.3 V for different R2 values (R1 = 4.7 kΩ)

As can be seen, the size of the R2 determines the current gain at low collector currents. The current gain at high collector currents approaches that of the built-in transistor, because I_B is now much larger than IR2 and the latter can be neglected. R1 has no influence on the current gain, as can already be seen in the graph above for the PDTC143TT without an R2. That device has the same current gain as the built-in transistor. Only the input voltage is higher, of course.

A comparison of types with different R1 values 2.2 kΩ from to 47 kΩ but all with an R2 of 47 kΩ shows the same current gain for all.

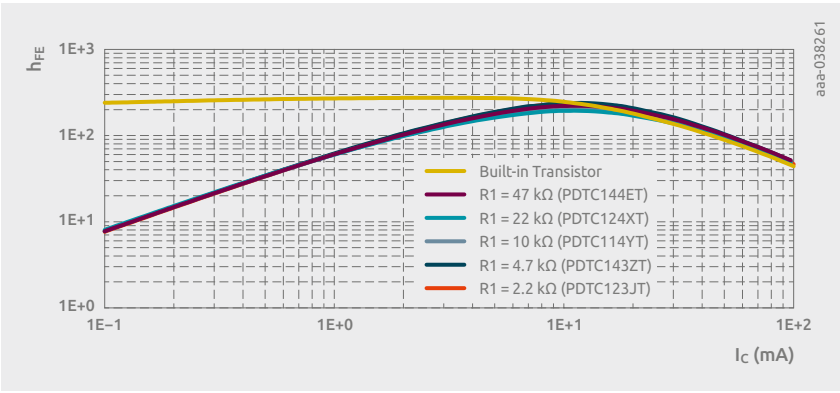


Figure 23 | h_{FE} as function of IC, V_{CE} = 0.3 V for different R1 values (R2 = 47 kΩ)

Figure 23 also shows the stabilizing effect on the current gain at lower collector currents. Between 10 and 20 mA, the batch-to-batch variation of the transistor current gain can be seen; at lower currents, the R2 is pulling the current gain down and stabilizes it.

h_{FE} in the data sheets is always specified at a V_{CE} of 5 V.

The 50 V/100 mA RET test conditions have type-dependent collector currents, which make comparisons difficult. This is for historical reasons.

For the 80 V/100 mA RETs with an R2 between 4.7 kΩ and 47 kΩ, standardized h_{FE} test conditions of I_C = 10 mA are used.

For the families with a maximum $I_C \geq 500$ mA, h_{FE} is specified at I_C = 50 mA.

Collector-Emitter saturation voltage

The R2 resistor also affects the saturation voltage of the RET. The leakage current reduces the base current and the device only turns on when the input current exceeds IB(min). The minimum collector current at a given I_C/I_B ratio can be calculated with the following equation:

$$I_{C(min)} = \frac{I_C}{I_B}\, ratio \cdot I_{B(min)} \approx 20 \cdot \frac{0.7V}{R2}$$

As with the current gain, the larger the R2, the earlier/at lower collector currents the V_{CEsat} curve returns to that of the built-in transistor. This can be seen in the following graph with RETs with an R1 of 4.7 kΩ and different R2 values:

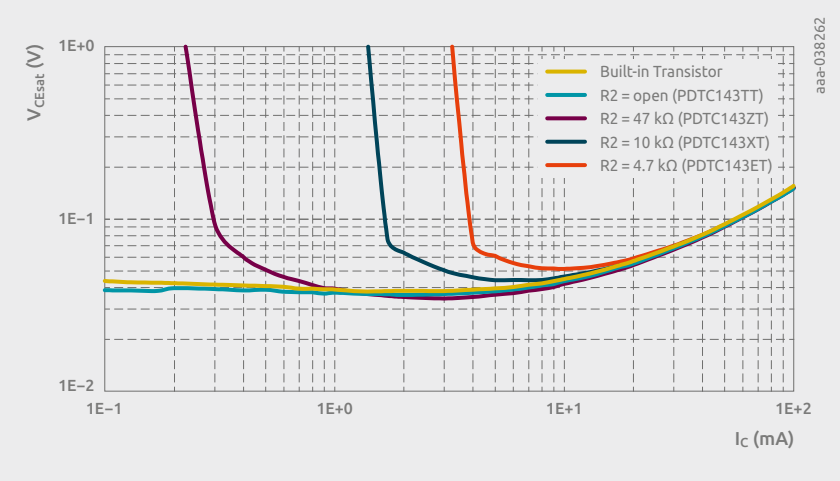


Figure 24 | V_{CEsat} as a function of I_C, $I_C/I_B = 20$ for different R2 values (R1 = 4.7 kΩ)

The R1 value has no influence on the V_{CEsat} characteristics as the base current is fixed in this graph:

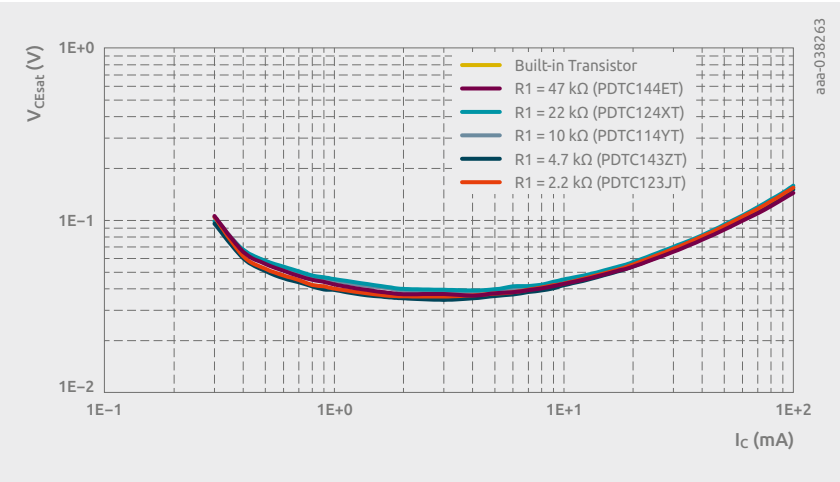


Figure 25 | V_{CEsat} as a function of I_C, $I_C/I_B = 20$ for different R1 values (R2 = 47 kΩ)

Only the input voltage has to be increased to achieve the same input current with a larger R1. The following graph shows the input voltages necessary to achive the saturation voltages in Figure 25:

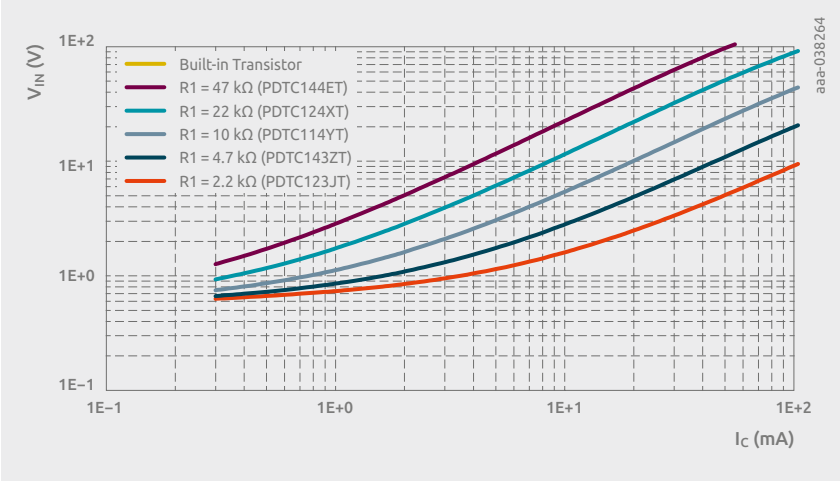


Figure 26 | V_{In} as a function of I_C, $I_C/I_B = 20$ for different R1 values (R2 = 47 kΩ)

V_{CEsat} in the data sheets is always specified at an I_C/I_B ratio of 20. The performance-based RET (PBR) family also have additional V_{CEsat} parameters specified at other I_C/I_B ratios.

The 50 V/100 mA RETs use type-dependent collector currents for the V_{CEsat} specification, which make comparisons difficult. Again, this is for historical reasons.

For the 80 V/100 mA RETs with an R2 between 4.7 kΩ and 47 kΩ, standardized V_{CEsat} test conditions of $I_C = 10$ mA are used.

For the families with a maximum $I_C \geq 500$ mA, V_{CEsat} is specified at $I_C = 50$ mA.

Switch-on/switch-off voltages

The digital transistors are primarily used for switching loads, and to help customers choose the right resistor combination for their application, the data sheets contain the $V_{I(off)}$ and $V_{I(on)}$ parameters and typical curves.

The $V_{I(off)}$ and $V_{I(on)}$ parameters specify the switching voltages to switch the digital transistor from off-/blocking state to on-/saturation state. In the off-state, the output is pulled up to an assumed supply voltage of 5 V and a leakage current of 100 µA. In the on-state, the RET is in saturation, V_{CEsat} is commonly specified as 0.3 V, and the specified output current is type-dependent. The following graph shows

the output voltage V_{CE} vs. the input voltage V_{IN}. The typical voltages $V_{I(off)}$ and $V_{I(on)}$ in the data sheets, where the RET switches, are the production averages. For a Gaussian distribution of the production process spread, this means that 50% of all devices are switching on at this specific voltage and the other half switch above or below this voltage. To always guarantee switching at the specified conditions, the minimum/maximum values have to be higher or lower than the typical voltages.

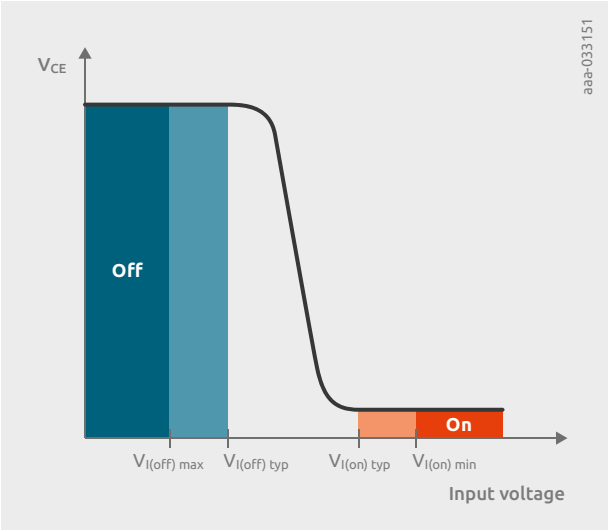


Figure 27 | RET V_{CE} voltage vs. input voltage

The above graph shows that to switch into the off-state, the maximum input voltage allowed has to be below the typical $V_{I(off)}$ voltage to ensure that the device is always off.

To switch to the on-state, the minimum $V_{I(on)}$ voltage has to be higher than the typical voltage to safely turn the device on.

The data sheet test conditions for the collector/output currents in the on-state differ by type.

For the families with a maximum $I_C \geq 500$ mA, $V_{I(on)}$ is specified at $V_{CE} = 0.3$ V and $I_C = 20$ mA.

The 50 V/100 mA RETs have type-dependent collector currents, at which $V_{I(on)}$ is specified. This is for historical reasons and makes comparing the on-voltages difficult.

For the 80 V/100 mA RETs with an R2 between 4.7 kΩ and 47 kΩ, standardized $V_{I(on)}$ test conditions of $V_{CE} = 0.3$ V and $I_C = 10$ mA are used.

To select the right resistor combination for a specific application, it is recommended to refer to the typical graphs of $V_{I(on)}$ vs. I_C and $V_{I(off)}$ vs. I_C. First, the output voltages of the logic circuit driving the RET for high- and low-state have to be specified. The resistor combination should then be chosen, so that the output voltage of the driver at high state switches the RET safely on and ensures the desired output current. The following graph shows the input voltage vs. the output current at room temperature for RETs with an R2 of 47 kΩ and different R1 from 2.2 kΩ to 47 kΩ. The built-in transistor without resistors is shown as a reference.

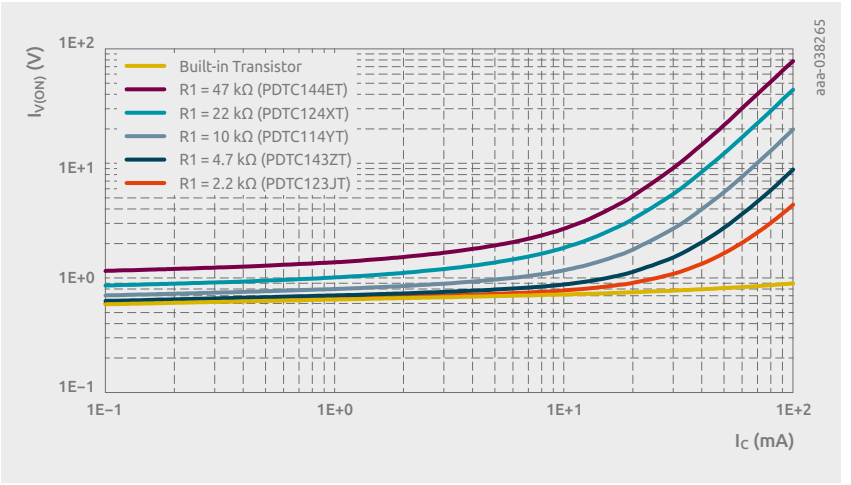


Figure 28 | $V_{I(on)}$ as a function of I_C for different R1 (R2 always 47 kΩ)

It is necessary to look at the worst-case operating conditions to make sure that the circuit works over the whole desired operating temperature range. For low temperatures, the input voltage must be higher than at room temperature. The following graph shows the different operating temperatures for the PDTC143ZT:

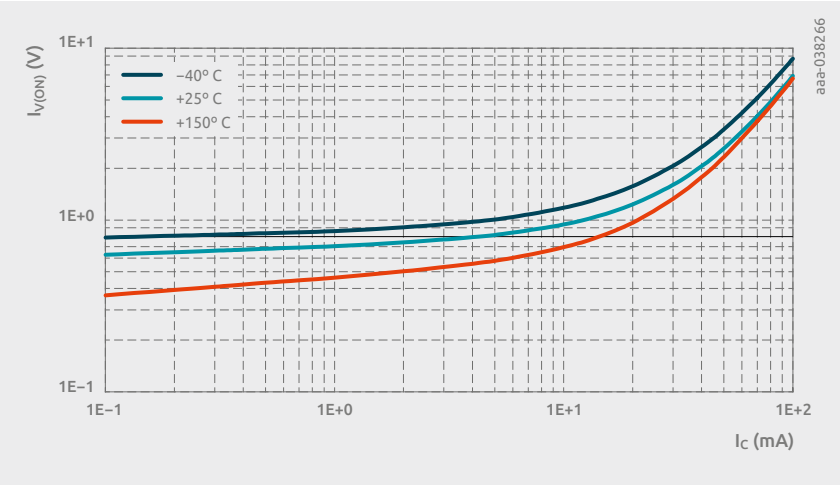


Figure 29 | $V_{I(on)}$ as a function of I_C at different operating temperatures (PDTC143ZT)

In addition to the temperature, the R1 tolerance also has to be included in a safety margin for the minimum input voltage.

For the $V_{I(off)}$ voltage, the same principle applies. Looking at a graph with different R2 values, using the same R1 of 4.7 kΩ from the previous figure, it shows that the types with large R2 values need the lowest switch-off voltage.

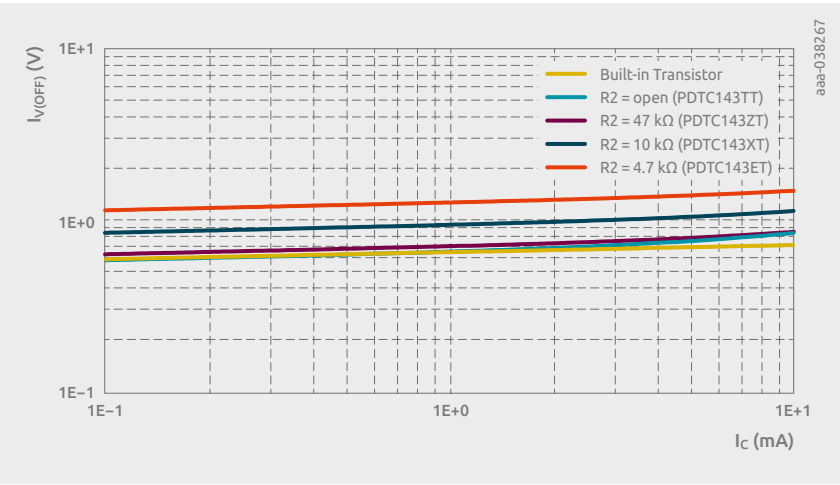


Figure 30 | $V_{I(off)}$ as a function of I_C for different R2 (R1 always 4.7 kΩ)

The operating temperature range also has to be considered for the turn-off voltage. At higher temperatures, the typical $V_{I(off)}$ voltage is lowered compared to room temperature.

The switching speed can also be influenced by the resistor choice. For BJTs, the turn-off time is much longer than the turn-on time. To increase switching speed, the turn-off time has to be addressed. When a BJT is turned on, base and emitter are flooded with carriers and the device is in saturation. To turn the device off, these excess carriers have to be removed. There are two ways to speed up this process: reducing the excess charge at turn-on by avoiding the device going into deep saturation (I_C/I_B of 5 to 10), and helping to remove the charge more quickly at turn-off.

The resistor R2 between base and emitter speeds up the removal of the excess charges. A smaller resistor is more efficient and leads to faster turn-off. The drawback is a higher leakage current I_{EBO}.

Helping to avoid exess charge in the transistor at turn-on can be done by selecting an R1 that is as large as possible to lower the base current and increase the I_C/I_B ratio. A further way to reduce excess charges during turn-on is to use a RET with a higher current gain. A reduced input voltage/current can then be used to drive the desired output current compared to a standard RET. The typical current gain of standard RETs is around 300 and is equivalent to the "B" selection of the BC848/BC858 (I_C (DC) = 100 mA) or the BC807-25/BC817-25 (I_C (DC) = 500 mA). Nexperia currently only offers high current-gain RETs for the 500 mA family: the PBR series with a $V_{(BR)CEO}$ of 40 V and maximum output current of 600 mA.

LED drivers

LEDs and LED applications are widely used across all market segments, and have a significant impact on everyday life. Although high-power LEDs need complex driver schemes and dedicated thermal concepts, most applications use LEDs with currents far below 500 mA and can be driven by a very simple and robust driver solution using constant-current LED drivers, which operate as simple linear regulators. Nexperia offers this type of LED driver family. The drivers are easy to use, reliable and cost-efficient, do not affect electromagnetic compatibility (EMC) and can be used in automotive applications such as interior and exterior lighting (e.g., door handles, dashboard, number plate lights, indicators and rear lights).

Nexperia offers a bipolar-based LED driver family. It consists of one transistor, two diodes and two resistors built on one chip. This one-chip solution reduces component count and board space. An LED driver works as a constant current source and ensures constant LED brightness. Figures 1 and 2 show the output current characteristic of LED driver NCR401U over supply voltage V_S. This driver provides initial output current I_{OUT} of 10 mA. The output current can be adjusted by connecting an external resistor.

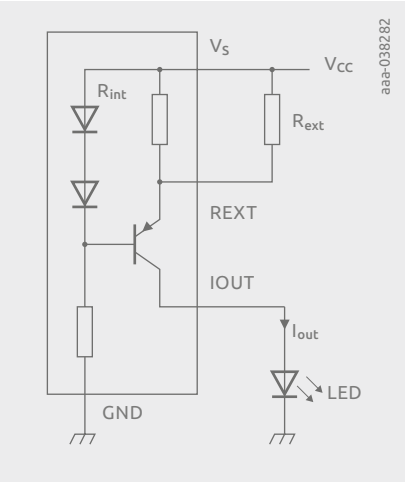


Figure 1 | LED driver dependent on R_{ext}

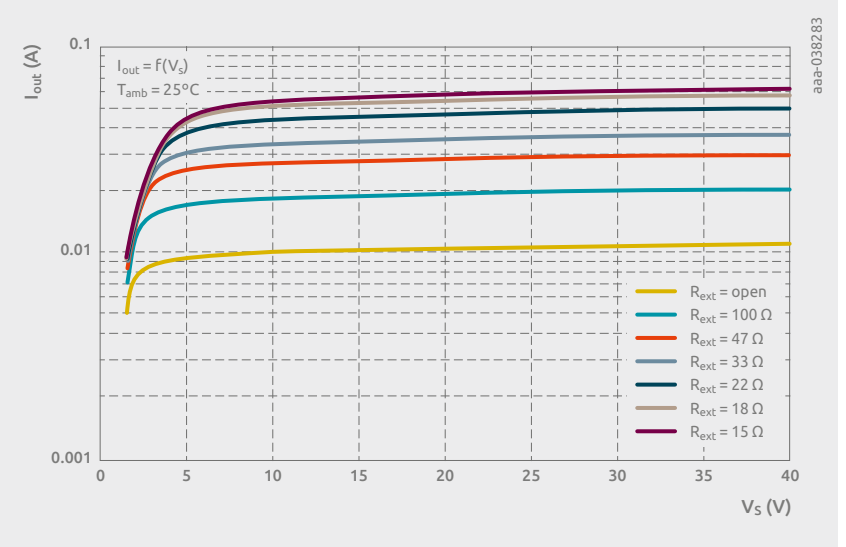


Figure 2 | Output current of NCR401U

The characteristic of the constant current source is explained in Figure 3.

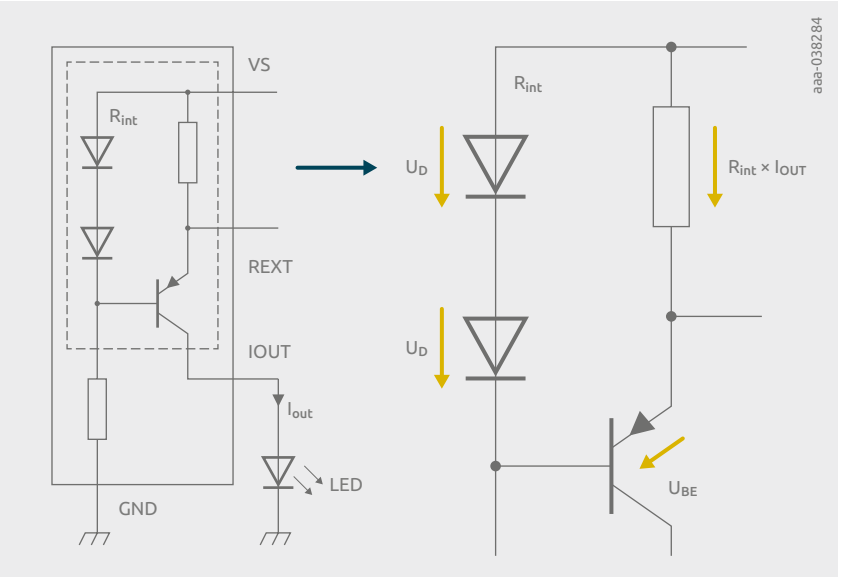


Figure 3 | Voltage drops in operation mode

In LED driver operation mode, the following equation is valid:

$$U_D + U_D = (R_{int} \times I_{OUT}) + U_{BE}$$

The resulting output current I_{OUT} is:

$$I_{OUT} = \frac{U_D + U_D - U_{BE}}{R_{int}}$$

In practice the forward voltage of diodes U_D and of transistor U_{BE} changes slightly over V_S. For a simplified I_{OUT} characteristic, this small change has been neglected here and all mentioned forward voltage regarded as constant. As the equation shows, the output current I_{OUT} is independent of supply voltage V_S. The output current can be determined only by internal resistor R_{int}.

For increasing output current an external resistance R_{ext} can be connected parallel to R_{int}. The estimated output current can be given by:

$$I_{OUT} = \frac{U_D + U_D - U_{BE}}{R_{int} /\!/ R_{ext}}$$

Product portfolio and applications

LED drivers can be divided into two groups with regard to applications. The first group is the LED driver family based on PNP bipolar junction transistors (BJTs), and the second is based on NPN BJTs. A PNP LED driver operates as a high-side driver, as shown in Figure 4. An NPN LED driver is used as a low-side driver.

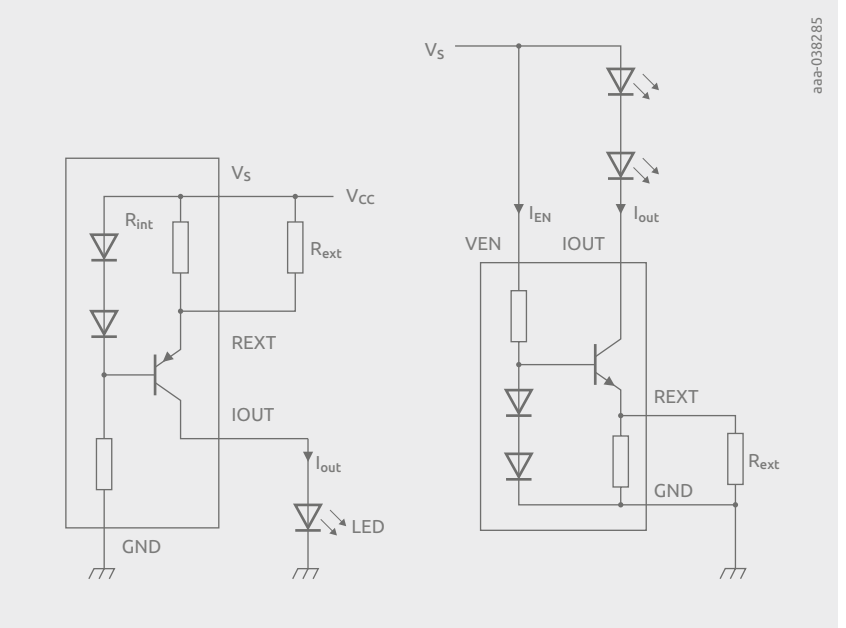


Figure 4 | LED driver topologies – high-side using a PNP and low-side using an NPN

Nexperia's product portfolio of PNP LED drivers is summarized in the table below.

Table 1. PNP LED driver family

Product	Internal resistor R_{int}	Output current I_{OUT}	Adjustable I_{OUT} range	Max. supply voltage V_S	Package
NCR401U	88 Ω	10 mA	10 to 65 mA	40 V	SOT457
NCR402U	42 Ω	20 mA	20 to 65 mA	40 V	SOT457
NCR405U	16 Ω	50 mA	50 to 65 mA	40 V	SOT457
NCR401T	88 Ω	10 mA	Not adjustable	40 V	SOT23
NCR402T	42 Ω	20 mA	Not adjustable	40 V	SOT23
PSSI2021SAY	48 kΩ	15 µA	15 µA to 40 mA	75 V	SOT353

The following operating conditions must be considered and ensured to work properly as a constant current source.

Minimum required supply voltage V_S: Figure 5 shows the output current characteristics of NCR401U over supply voltage. NCR401U initially provides 10 mA output current in case no R_{ext} is connected. The minimum overhead voltage drop (V_S–V_{LED}) across a constant-current driver is approximately 1.4 V. Below this overhead voltage, the LED driver does not work properly. The required supply voltage is given:

$$V_S > 1.4\ V + V_{LED} \quad or \quad V_{LED} < V_S - 1.4\ V$$

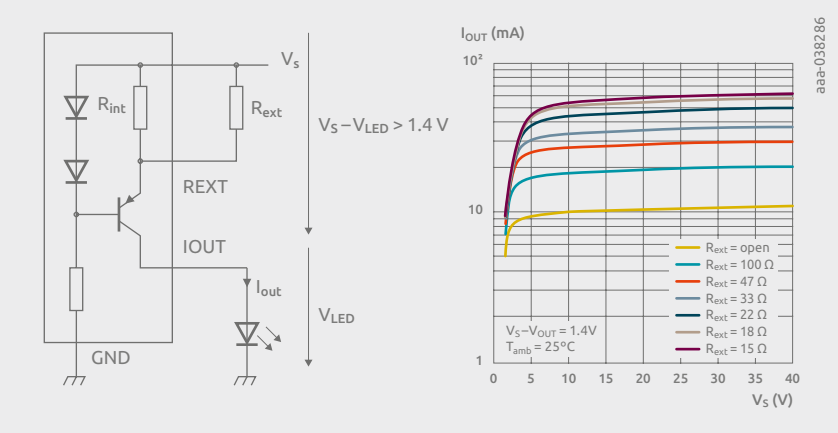


Figure 5 | Output current dependent on external resistance R_{ext}

LED drivers are used when the brightness of an LED should be independent of the supply voltage to some degree. The 12 V power supply in a car fluctuates between 11 V and 15 V during regular operation. V_{LED} determines how many LEDs can be connected in series. For example, if one LED requires 2 V then up to four LEDs can be connected in series for 11 V supply voltage, as checked below:

$$V_{LED} < V_S - 1.4\ V = 9.6\ V$$

Maximum power dissipation: The power dissipation at an LED driver can be roughly estimated below. This maximum power dissipation at the LED driver is limited by package power dissipation P_{tot}. The NCR401U is in the package SOT457 with a P_{tot} of 0.75 W, which determines the allowed operating range.

$$P_{LED\ driver} \approx (V_S - V_{LED}) \times I_{OUT} < P_{tot}$$

The following examples show easy estimation of the allowed operation conditions.

The device NCR401U is supplied with V_S = 20 V. The output current I_{OUT} is adjusted to 50 mA by an external resistor. Different numbers of LEDs are connected. Each LED needs 2 V supply.

With one LED connected, the power dissipation at the LED driver exceeds the allowed package power dissipation. This operation condition will damage the LED driver.

$$P_{LED\ driver} \approx (V_S - V_{LED}) \times I_{OUT} = (20\ V - 2\ V) \times 50\ mA = 900\ mW$$

If there are five LEDs connected in series, the power dissipation at the LED driver is still within the allowed package power dissipation. It is close to the limit, and the output current will slightly decrease due to the high power load at the LED driver. This effect is due to the self-heating of the device and the negative thermal coefficient of the output current.

$$P_{LED\ driver} \approx (V_S - V_{LED}) \times I_{OUT} = (20\ V - 10\ V) \times 50\ mA = 500\ mW$$

If there are nine LEDs connected in series, the power dissipation at the LED driver is clearly below the allowed package power dissipation.

$$P_{LED\ driver} \approx (V_S - V_{LED}) \times I_{OUT} = (20\ V - 18\ V) \times 50\ mA = 100\ mW$$

The output can be switched on and off by connecting a resistor-equipped transistor (RET) such as PDTC124XU.

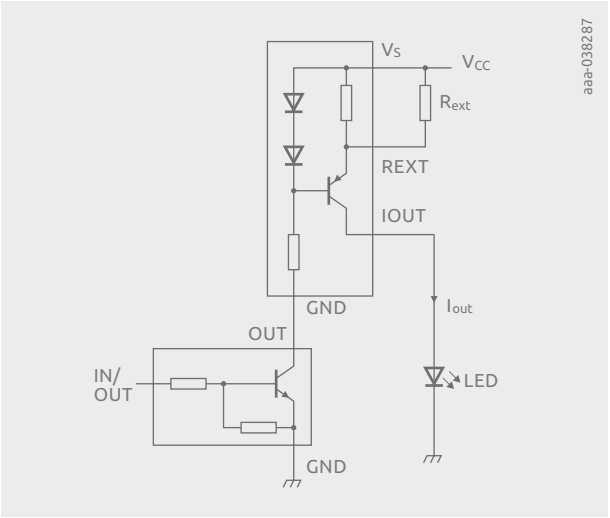


Figure 6 | Switching the output current on/off

Nexperia's product portfolio of NPN LED drivers is summarized in the table below.

Table 2. NPN LED driver family

Product	Adjustable I_{OUT}	Output voltage V_{OUT}	Enable voltage V_{EN}	Max. power dissipation*	Package
NCR420U	10 to 150 mA	40 V	40 V	750 mW	SOT457
NCR420Z				1250 mW	SOT223
NCR420PAS				530 mW	DFN2020D-6
NCR421U	10 to 150 mA	40 V	4.5 V	750 mW	SOT457
NCR421Z				1250 mW	SOT223
NCR421PAS				530 mW	DFN2020D-6
NCR320U	10 to 250 mA	16 V	25 V	750 mW	SOT457
NCR320Z				1250 mW	SOT223
NCR320PAS				530 mW	DFN2020D-6
NCR321U	10 to 250 mA	16 V	4.5 V	750 mW	SOT23
NCR321Z				1250 mW	SOT223
NCR321PAS				530 mW	DFN2020D-6

*Device mounted on an FR4 PCB, four-layer copper, tin-plated and standard footprint.

The NPN LED driver family consists of four basic types with regard to electrical performance: NCR420x, NCR421x, NCR320x and NCR321x.

These four basic types are released in three different packages: SOT457, SOT223 and DFN2020D-6.

All NPN LED driver types are equipped with R_{int} of 95 Ω and provide initial output current of 10 mA. With a connecting external resistor, the output current can be adjusted up to 250 mA.

NPN LED drivers can be used with two different application modes, as shown in Figure 7.

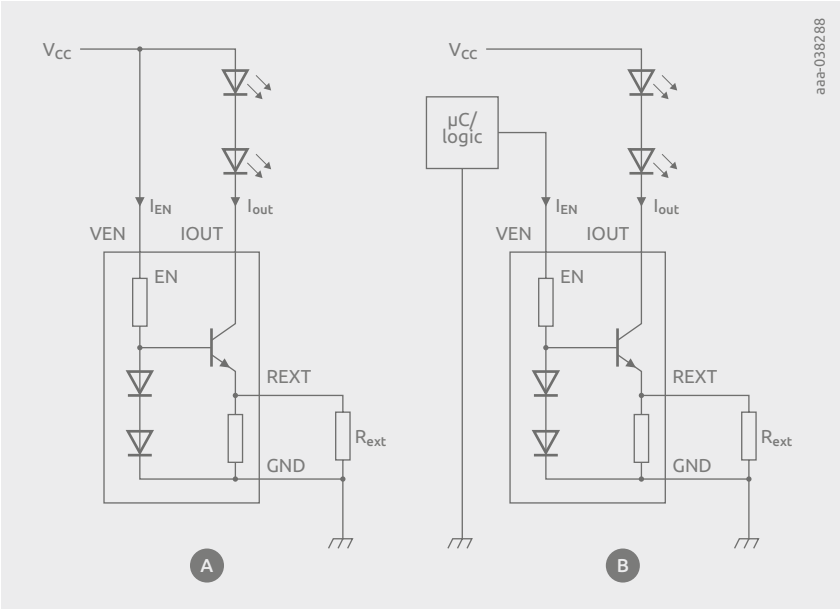


Figure 7 | NPN LED driver with different application modes

Figure 7a shows a comparable application mode with a PNP LED driver. Figure 7b shows a further application mode. The LED driver can be switched on/off by Enable Voltage VEN. The allowed range of the enable voltage for the NCR420x types is specified for 0 to 40 V. NCR421x types need a smaller enable voltage of 0 to 4.5 V and are suitable for driving via a microcontroller. Figures 8a and 8b show the output current characteristics of both application modes.

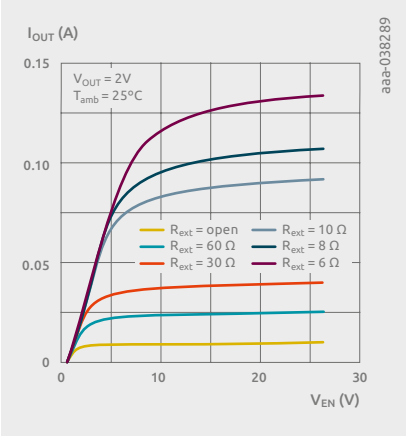


Figure 8a | Output current of Figure 7a

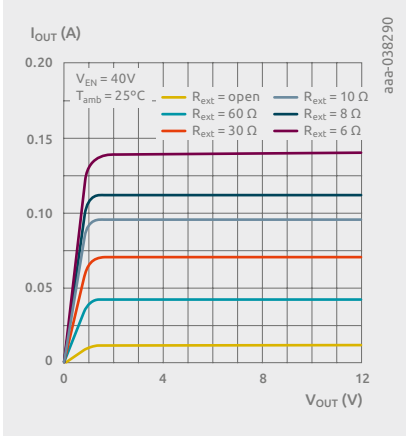


Figure 8b | Output current of Figure 7b

The operating conditions and guides given for PNP LED drivers are also valid for NPN LED drivers.

To safely drive currents that are above the limits of the LED drivers, two or more devices can be parallel connected, as shown in Figure 9. When choosing the same values for the external resistors, the drive current splits equally and the capability for handling excess power is doubled.

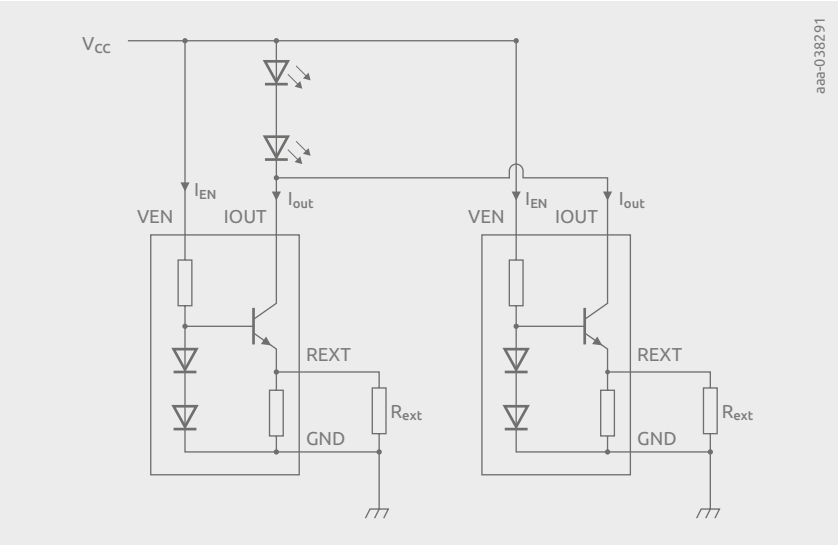


Figure 9 | Increasing output current by parallelization

2.3 BJT static behavior

In this chapter the static behavior of a bipolar junction transistor (BJT) is described, with a focus on the key facts.

If a BJT is run in the simple configuration shown in Figure 1, this means that the base-emitter path is biased with an adjustable DC supply to create base current pulses I_B. While the collector-emitter path is also connected to a DC supply, basic measurements of the static behavior can be performed.

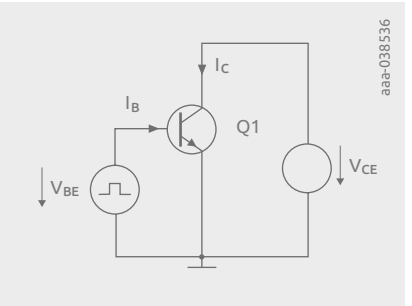


Figure 1 | NPN-BJT run in normal mode

For such measurements it is important to test with short I_B pulses to avoid self-heating of the BJT, because the transistor parameters are significantly influenced by temperature. For the tests the transistor is kept in normal mode; this means that the collector-base diode is kept in reverse mode while the base-emitter diode conducts in forward mode.
If the voltage of V_{BE} is increased carefully while testing IB, a forward conduction curve of a p-n diode can be found. I_B increases quite steeply once V_{BE} exceeds about 0.65 V. The impact of V_{CE} is very small. With an increase of V_{CE} the input curve I_B vs. V_{BE} shifts slightly in the right direction, as shown in Figure 2. This trend changes to the other direction for a high V_{CE}.

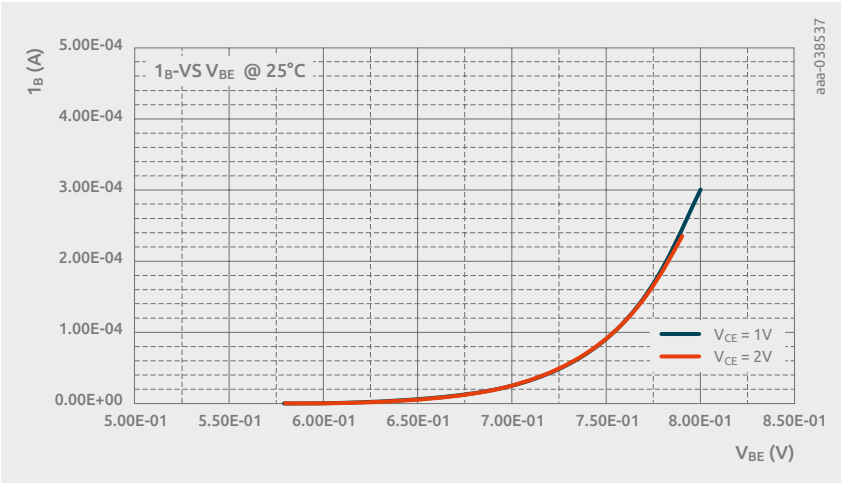


Figure 2 | Input characteristics diagram I_B vs. V_{BE} for BC847B

A similar curve can be found if a diagram is created where I_C vs. V_{BE} is measured and V_{CE} is modified additionally, as shown in Figure 3. The curves look quite similar if V_{CE} is modified and they get shifted to the left side, toward slightly lower V_{BE} values if V_{CE} is increased.

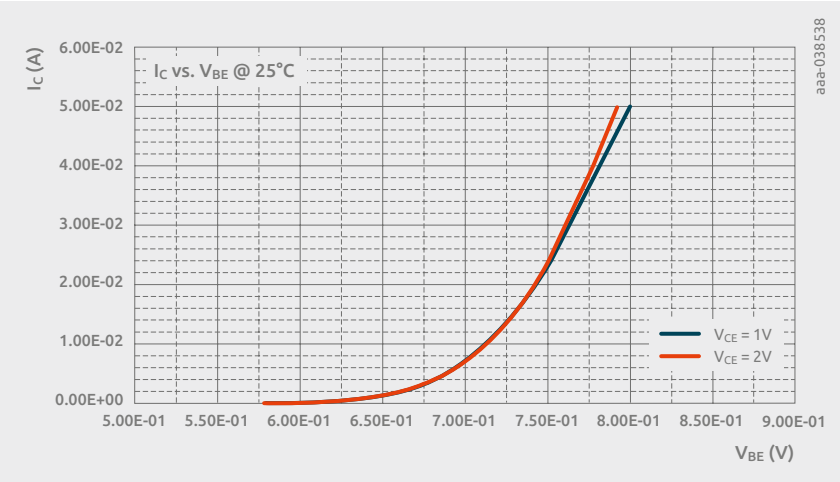


Figure 3 | Collector current I_C vs. V_{BE} for BC847B

If a constant base current is applied to a BJT and the collector current is measured vs. V_{CE}, a graph as shown in Figure 4 can be derived. In a rather small area at the left side of the diagram the curves ramp steeply. This is the so-called saturated mode, where the collector-base diode conducts in contrast to the normal mode. For higher V_{CE} values the curves show an almost constant collector current. The current amplification is almost constant, following the equation:

$$I_C = B \times I_B$$

For high collector current the curves rise moderately over the applied collector-emitter voltage.

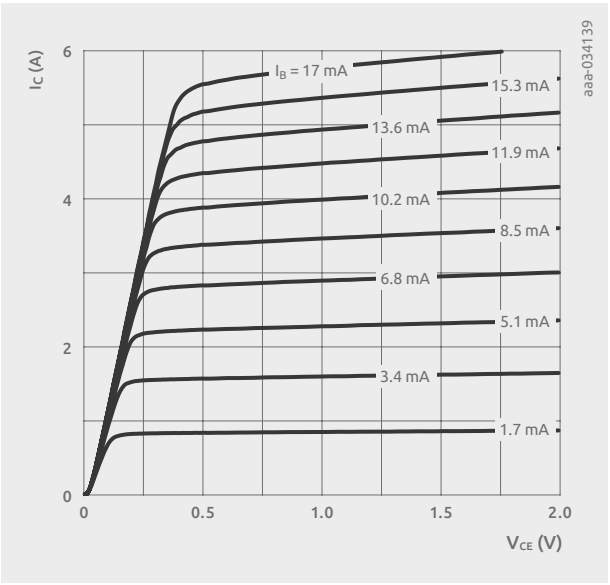


Figure 4 | Output characteristics diagram of PBSS4310PAS-Q, I_C vs. V_{CE}

In normal or active mode, the collector current mainly depends on the base current, which depends on V_{BE} as shown in the input diagram in Figure 2. To create a formula describing the I_C vs. V_{BE} function, a BJT parameter called V_A is introduced. If the active area parts of the curves of an output diagram are extrapolated in the direction of negative V_{CE} values, all curves have one common intersection.

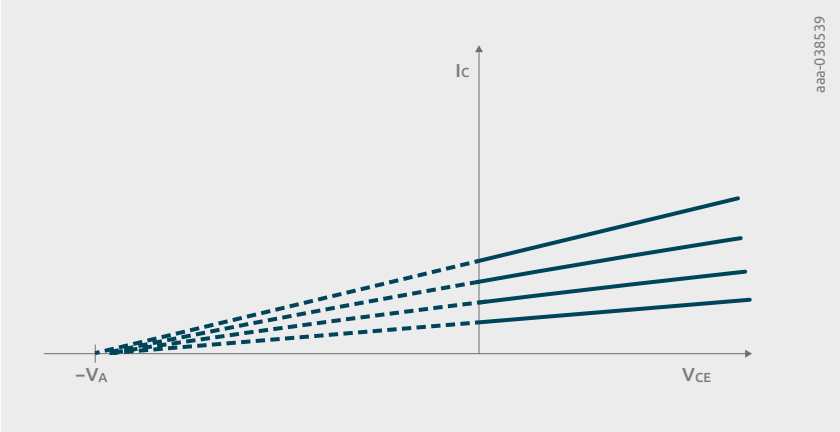


Figure 5 | Early voltage V_A derived from the output characteristics diagram

The voltage at the intersection point is called Early voltage, named after James Early, who discovered that the effective width of the base (W_{eff}) varies with the base-to-collector voltage applied. If the reverse bias across the collector-base junction is increased, this increases the collector-base depletion width, and so the width of the charge carrier portion of the base gets decreased. This is called the Early effect:

$$I_C = I_S\, e^{V_{BE}/V_T} \times (1 + V_{CE}/V_A)$$

I_S = saturation current, typically in the league of 10^{-12} A

$V_T = kT/q$ = thermal voltage, ~26 mV for BJTs at room temperature,

with k the Boltzmann constant (1.380649×10^{-16} VAs/K),

T the absolute temperature and

q the elementary charge (1.602×10^{-19} As)

The term in the brackets of the formula ($1 + V_{CE}/V_A$) represents the variation of the current amplification created, related to V_{CE} by the Early effect.

For I_B dependent on V_{BE} the below equation can be applied. B0 is the current amplification if no collector-emitter voltage is present. With a collector-emitter voltage there, no collector current can flow, so this value is derived from extrapolation down to V_{CE} equal to 0 V.

$$I_B = I_S/B_0 \times e^{V_{BE}/V_T}$$

In Chapter 3 "Data sheet Parameters", further facts relating to the static behavior are discussed. As many of the BJT parameters show a strong temperature dependency, this aspect is given further attention.

2.4 BJT dynamic behavior

Many parameters in data sheets and the related diagrams are related to static operation of a bipolar junction transistor (BJT). However, this information does not help with understanding the dynamic behavior of a a BJT if it is used as a switch and controlled by rectangular base signals, or if the BJT needs to work as an amplifier for sine-wave signals.

If a BJT is used as a simple switch, it does not react instantaneously on a control signal, but there is a delay for turn-on as well as for turn-off. The reason for this is the presence of non-linear p-n junction capacitances. Additionally, charges are stored again in non-linear diffusion capacitances present in the base zone of a BJT, and influence the dynamic performance.

For discrete BJTs, two junction capacitances must be considered. For integrated BJTs an additional third capacitance to the substrate is present, which is not discussed in this handbook. Furthermore, two diffusion capacitances need to be added. Figure 1 shows the so-called Gummel-Poon model circuit diagram for a BJT, which is used for SPICE simulators like PSpice, LTspice® and other simulator variants.

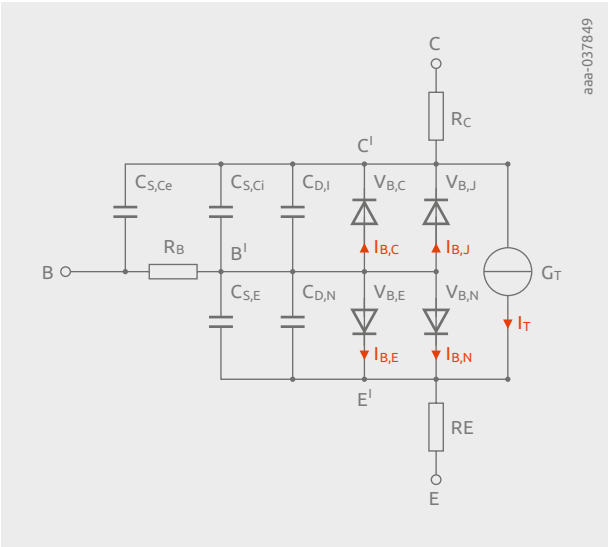


Figure 1 | Gummel-Poon model for discrete (single) BJT meant for static and dynamic behavior

In the base-emitter path $C_{J,E}$ represents the junction capacitance. The collector junction capacitance $C_{J,C}$ is formed by the internal junction capacitance $C_{J,Ci}$ related to the active base zone and the external junction capacitance $C_{J,Ce}$ located at the base connection. These two collector junction capacitances are connected in parallel with the base resistor RB in between, as shown in Figure 1.

$$C_{J,C} = C_{J,Ci} + C_{J,Ce}$$

The portion that the external and internal junction capacitances have for the collector junction capacitance can be written using a factor x. This parameter is called x_{CSC} in literature and the following simple formulas can be noted down:

$$C_{J,Ci}(V_{B'C'}) = \chi_{CJC} \times C_{J,C}(V_{B'C'})$$
$$C_{J,Ce}(V_{BC'}) = (1 - \chi_{CJC}) \times C_{J,C}(V_{BC'})$$

For discrete BJTs x_{CJC} is in the range from 0.5 to 1. This means that $C_{J,Ci}$ is normally bigger than $C_{J,Ce}$. All junction capacitances depend on the voltage applied and furthermore on the area of the junction, the doping of the areas adjacent to the junction and the doping profile. The capacitances increase with the junction area as well as the level of doping. The formula below can be used for CS if the voltage V applied is smaller than ~$0.5 \times V_{DIFF}$. The diffusion voltage V_{DIFF} increases with the doping and is normally in the range from 0.5 to 1 V. mS brings the influence of the doping profile into the equation. The value is about 0.3 for a linear progression of the doping concentration and 0.5 for a step-like progression.

$$C_J(V) = C_{J0} / (1 - V/V_{DIFF})^{mS}$$

For voltages higher than $V = fs \times V_{DIFF}$, CJ(V) follows the equation below. f_s is in the range from 0.4 to 0.7 in practice:

$$C_J(V) = C_{J0} \times [1 - f_S (1 + m_S) + m_S \times V / V_{DIFF}] / (1 - f_s)^{1 + mS}$$

In Figure 2 the resulting curve for the junction capacitance C_J vs. the voltage applied is shown.

Two examples for mS equal to ½ and ⅓ are shown. The dashed lines show how the curves look according to the formula for $V < f_s \times V_{DIFF}$, but the second equation needs to be a applied for this voltage region.

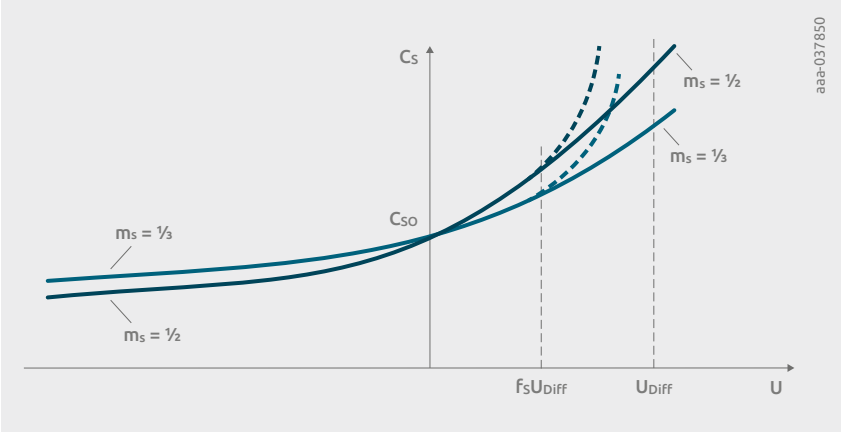


Figure 2 | Junction capacitance curve

In the diagram in Figure 1, two additional diffusion capacitors can be seen beside the junction capacitors, $C_{D,F}$ for the emitter diode and $C_{D,R}$ for the collector diode. Below, the equations for these diffusion capacitors dependent on the voltage applied are provided. τF and τR are called transit times. The characters F in the lower-case naming of the parameters stands for a forward mode operation, and R for reverse mode.

$$C_{D,F}(V_{B'E'}) = \tau_F \times I_S / U_T \times e\, V_{B'E'} / V_T$$

$$C_{D,R}(V_{B'C'}) = \tau_R \times I_S / U_T \times e\, V_{B'C'} / V_T$$

In normal mode the collector diffusion capacitance $C_{D,R}$ is very small and can be ignored compared to the junction capacitance $C_{J,Ci}$, and can also be ignored for calculations and modeling. The emitter diffusion capacitance $C_{D,F}$ is small for low current in relation to $C_{J,E}$ but this changes for high current. Therefore, it is very important that τ_F is precisely modeled to achieve a realistic dynamic behavior for high current.

Chapter 3

Data sheet parameters

To select the most suitable bipolar junction transistor (BJT) for a specific application, it is necessary to study the components' data sheets in detail. Also, to compare different types, it is important to have a good understanding of data sheet parameters. The test conditions used for parameters in transistor specifications can differ between semiconductor suppliers. This fact must be considered carefully before deciding on the most suitable device.

The objective of this chapter is to accurately explain all parameters that are usually present in Nexperia data sheets for bipolar transistors, including related test setups, thus helping engineers use the data and the provided curves efficiently. The data sheet for PBSS4310PAS-Q is taken as an example. Due to the wide bipolar transistor portfolio, and the fact that many generic BJTs have already existed in the market for quite a long time, data sheets can deviate from the examples used in this chapter.

The BJT data sheets start with a "General description". Section 1 states the basic facts of the transistor such as polarity (NPN/PNP), technology specifications and package type.

Section 2, "Features and benefits", is a brief list of major component features and product highlights, such as a very low V_{CE} saturation voltage (V_{CEsat}) and a high current amplification h_{FE}, even provided at high IC. Additionally, extended thermal operating ranges are mentioned ($T_{j(max)}$ = 175°C) alongside package facts such as solderable side pads and the support of an automatic optical inspection (AOI) of the solder joints.

Section 3, "Applications", highlights typical application areas. In this example, these are linear voltage regulation, load switches, battery-driven devices and charging circuits.

Section 4 contains the "Quick reference data", which are the most important data for a BJT and give a quick evaluation of whether the component meets the basic requirements for a target application. Table 1 shows the quick reference data for PBSS4310PAS-Q.

V_{CEO} is the maximum allowed collector-emitter voltage with an open base. As a further parameter, the maximum allowed constant collector current is provided. The minimum current gain h_{FE}, which is the ratio of collector current to base current, is listed next. The test condition applied for this parameter is a collector current of 100 mA, with a voltage of 2 V across the collector-emitter path tested in pulsed mode with a pulse length of 300 µs and a duty cycle δ of less than 0.02. The reason for the pulsed test method is that the component should not heat up significantly compared to the ambient temperature of 25°C, because this would impact the value of the parameter and lead to an undesired h_{FE} increase. With the pulsed measurement approach, the results do not depend on the mounting

condition and show the behavior of the bipolar transistor without the impact of self-heating. The thermal performance of the PCB and the test fixture has no influence on the test measurement results. The maximum value for V_{CEsat}, the collector-emitter saturation voltage, is provided in Table 1: this would be important if the BJT were to be used as a switch to get an understanding of how large the residual voltage in an on-state will be. Again, it is important to study the test condition for this parameter if parts are being compared. In the example, the collector current is 1 A and the base current is 10 mA, which means that I_C/I_B is equal to 100. As for the parameter h_{FE}, it is necessary that the test condition is pulsed to avoid heating.

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	–	–	10	V
I_C	collector current		–	–	3	A
h_{FE}	DC current gain	V_{CE} = 2 V; I_C = 100 mA; pulsed; $t_p \leq 300$ µs; $\delta \leq 0.02$; T_{amb} = 25°C	325	–	–	–
V_{CEsat}	collector-emitter saturation voltage	I_C = 1 A; I_B = 10 mA; pulsed; $t_p \leq 300$ µs; $\delta \leq 0.02$; T_{amb} = 25°C	–	–	55	mV

Section 5 provides the pinning information shown in Table 2. The three contacts of a BJT – base, emitter and collector – are assigned to the package pins. A simplified package outline clarifies the location of each contact. The package diagram shows a transparent top view, so the view is through the plastic molding down to the bottom with the flat contact areas of the leadless 2 mm × 2 mm DFN2020 package.

Table 2: Pinning information

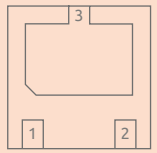
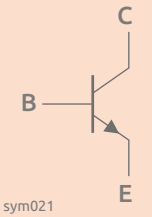
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 Transparent top view **DFN2020D-3** (SOT1061D)	 sym021
2	E	emitter		
3	C	collector		

Table 3 from Section 6 in the data sheet gives ordering information, with the exact type number or name and further package-related details. The last letters in the name indicate the package type; "PAS" in the example shown stands for a DFN2020D-3 package. The additional "-Q" informs the user that the component meets the high quality requirements for use in automotive applications. The package description also lists the package dimensions. Furthermore, it is mentioned that the leadless component features side-wetTable flanks (SWFs). The side flanks of the contacts are tin-plated and allow the solder paste to produce a meniscus from the solder lands up to the BJT. This supports an AOI after soldering, which is very important for automotive electronic devices.

Table 3: Ordering information

Type Number	Package		
	Name	Description	Version
PBSS4310PAS-Q	DFN2020D-3	plastic, leadless thermal enhanced ultra thin small outline package with side-wetTable flanks (SWF); no leads; 3 terminals; 1.3 mm pitch; 2 × 2 × 0.65 mm body	SOT1061D

Every BJT has a laser marking on the top side, as detailed in Section 7 of the data sheet. The marking code is unique for every Nexperia package type. It cannot be unique across all Nexperia products because of the limited space available on SMD packages, and therefore the limited number of characters present on a single marking.

Table 4: Marking codes

Type Number	Marking code
PBSS4310PAS-Q	F2

Section 8 gives the limiting values of the product. Table 5 contains more data than in the quick reference data chapter discussed above.

V_{CBO} is the maximum allowed voltage across the collector-base diode while the emitter is kept open. The maximum V_{CEO} is listed again. For the collector-emitter path, three ratings are common: V_{CES}, V_{CER} and V_{CEO}. V_{CES} is measured with a base that is short-circuited to the emitter. To derive V_{CER}, the base is connected via a resistor to the emitter, and for V_{CEO} the base is kept open or floating.

The voltages follow the relation:

$$V_{CES} \geq V_{CER} \geq V_{CEO}$$

Table 5: Limiting values.
In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		–	10	V
V_{CEO}	collector-emitter voltage	open base		–	10	V
V_{EBO}	emitter-base voltage	open collector		–	8	V
I_C	collector current			–	3	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		–	5	A
I_B	base current			–	500	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$°C	[1]	–	560	mW
			[2]	–	1.1	W
			[3]	–	1.54	W
T_j	junction temperature			–	175	°C
T_{amb}	ambient temperature			−55	175	°C
T_{stg}	storage temperature			−65	175	°C

[1] Device mounted on a FR4 Printed-Circuit Board (PCB), single sided copper, tin-plated and standard footprint.
[2] Device mounted on a FR4 PCB, single sided copper, tin-plated mounting pad for cathode 1 cm².
[3] Device mounted on a FR4 PCB, single sided copper, tin-plated mounting pad for cathode 6 cm².

V_{EBO} is the emitter-base voltage. The maximum reverse voltage for the base-emitter diode is not high for most BJTs independent of the V_{CEO} rating. To operate the base-emitter path degrades a BJT with respect to h_{FE}, even if a low reverse current is driven. In some special applications bipolar transistors are run in the reverse direction, which means that the collector and emitter are swapped. In this case it is necessary to pay great attention to the V_{EBO} parameter.

The next limiting values provided are I_C (the constant collector current) and I_{CM} (the peak collector current tested with a single pulse shorter than 1 ms). The maximum value for the base current I is listed again. Next, the total power dissipation P_{tot} for different mounting conditions is listed.

The footnotes describe the test board specifics, which is a minimal-size standard footprint, and alternatively 1 cm² as well as 6 cm² as examples with enhanced cooling areas. The standard footprint as recommended by Nexperia can be found at the end of data sheets in the "Soldering" chapter. The reason for the differences between the P_{tot} values is the size of the cooling pad connected to the collector pad on the board. The collector contact provides the best thermal path from the crystal down into the PCB for conventional plastic molded SMD packages. Finally, the maximum junction temperature is defined as well as the allowed ambient temperature and storage temperature range. BJTs with gold bond wires should not be allowed to become warmer than 150°C because of a degradation risk for the bond wire joints in the case of overheating. For copper bond wires the maximum temperature is 175°C, which allows these parts to operate under hotter conditions compared to gold wire components.

Figure 1 shows the so-called power derating curve. Power is derated starting with T_{amb} = 25°C, with a linear curve down to 0 mW at $T_{j(max)}$.

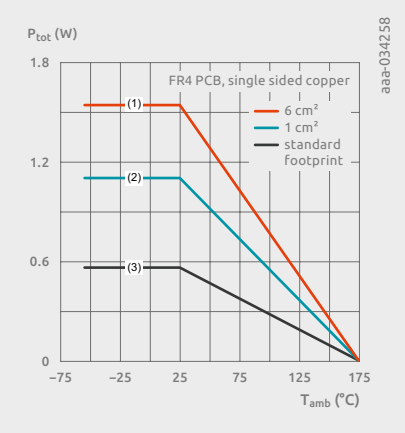


Figure 1 | Power derating curves

Section 9 of the data sheet shows the thermal characteristics of the BJT. Three thermal resistance values are provided for different mounting conditions. The junction temperature can be calculated with a simple formula, as shown below:

$$T_j = R_{th(j-a)} \times P + T_{amb}$$

The junction temperature T_j is equal to the thermal resistance $R_{th(j-a)}$ multiplied by the device power plus the ambient temperature.

Table 6: Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	–	–	268	K/W
			[2]	–	–	137	K/W
			[3]	–	–	98	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			–	–	7	K/W

[1] Device mounted on a FR4 Printed-Circuit Board (PCB), single sided copper, tin-plated and standard footprint.
[2] Device mounted on a FR4 PCB, single sided copper, tin-plated mounting pad for cathode 1 cm².
[3] Device mounted on a FR4 PCB, single sided copper, tin-plated mounting pad for cathode 6 cm².

The junction-to-ambient values for the thermal resistance can be calculated from the limiting values for P_{tot} at 25°C room temperature in Table 5. Using the formula above for the maximum allowed junction temperature of 175°C, we can state:

$$R_{th(j-a)} = (T_j - T_{amb})/P_{tot}$$

To give an example for standard footprint, this means:

$$R_{th(j-a)} = 150\ K/560\ mW = 268\ K/W$$

This is the value listed in Table 6.

$R_{th(j-sp)}$ is the thermal resistance for the mounting condition that the solderpoint is kept at 25°C constantly, independent of the power dissipated. Either the collector lead pad for conventional SMD packages or the center thermal collector contact for leadless DFN packages is intended as the solderpoint. This thermal resistance is a pure component-related parameter, and does not depend on the thermal performance of the test board. However, $R_{th(j-a)}$ values from different vendors need to be compared carefully; the layout of the PCB will not be fully identical. It is also important to know the thickness of the copper. A thermal pad with a rather thick copper layer of 70 µm, for example, can conduct heat much better than a standard 35 µm thickness. Furthermore, the material of the PCB itself and its overall thickness contribute to the thermal performance of the test board.

Figure 2 shows a $Z_{th(j-sp)}$ graph as a function of pulse duration and duty cycle. This diagram is very helpful if the thermal behavior for a single power pulse or for repetitive power pulses needs to be investigated. To create the curves, rectangular power pulses have been applied to the device.

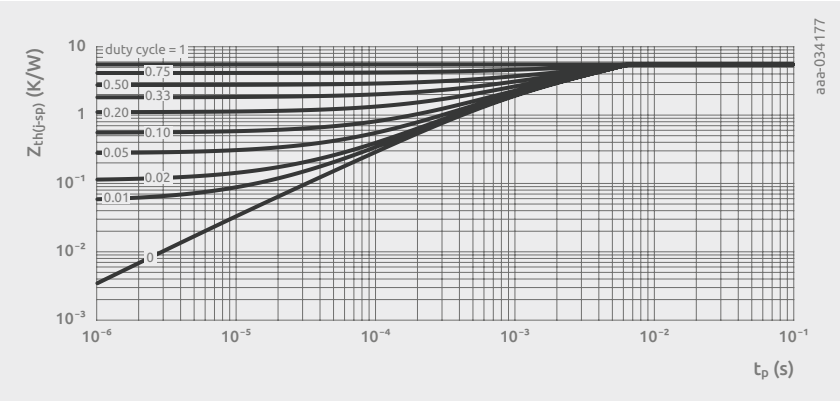


Figure 2 | Transient thermal impedance from junction to solderpoint as a function of pulse duration; typical values

In the thermal evaluation of a use case the corresponding pulse length tp must be selected. The diagram contains curves for single pulses with a duty cycle of d = 0, up to a DC case with d = 1.

The duty cycle is defined as:

$$d = \frac{t_p}{T}$$

where T is the repetition time.

For d = 1, $Z_{th(j-sp)}$ is identical to the $R_{th(j-sp)}$ as corner case. For short power pulses the component can accept a higher pulse power, reflected in smaller Z_{th} values. All curves start with the same Z_{th} value of $R_{th(j-sp)}$ on the right side of the diagram. This means that pulses longer than about 60 ms stress the device like a DC case. The small die reaches the same temperature within the pulse time.

If the pulse length becomes smaller than 60 ms, Z_{th} decreases with linear decay. This effect is more pronounced for a smaller duty cycle. Toward the left side of the diagram, the curves are flattening toward a constant value. This fact has a simple cause: if the pulse length for a given duty cycle is reduced, the repetition time gets smaller as well, or in other words the frequency of the pulses increases. If the

frequency is high enough, the device sees the average of the power pulses because the ripple in the temperature created by the incoming power pulses becomes smaller and smaller.

This means we get the equation below for very short pulses:

$$Z_{th} = d \times R_{th(j-sp)}$$

In other words, the part sees the average power of the pulses simply if the pulses are short enough.

With the Z_{th} value derived from the diagram for the customer operation case, the junction temperature can be calculated with the equation below.

$$T_j = Z_{th(j-a)} \times P_{pulse} + T_{amb}$$

Section 10 of a typical Nexperia data sheet contains detailed electrical characteristics. To make a comparison using this data, it is very important to study and understand the complete test conditions. The list starts with the minimum breakdown voltages $V_{(BR)CB}$, $V_{(BR)CE}$ and $V_{(BR)EB}$, with open condition for the contact which is not part of the reverse-driven electrical path. The leakage current used for testing these VBR parameters is also published.

The following three parameters are the maximum cut-off currents: I_{CBO}, I_{CES} and I_{EBO}. Test voltage 8 V has been applied for all the three currents. I_{CES} is tested with a base-to-emitter short-circuit.

The minimum h_{FE} is provided for several collector current ratings and a voltage of 2 V across the collector-emitter path. For these parameters it is important to test with pulses to avoid significant self-heating of the BJT. 300 µs is chosen as a pulse length, with a duty cycle of 0.02. This means that the testing frequency is about 67 Hz with f = d/tp (d = duty cycle).

Table 7: Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100\ \mu A$; $I_E = 0\ A$	10	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 10\ mA$; $I_B = 0\ A$	10	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage (collector open)	$I_E = 100\ \mu A$; $I_C = 0\ A$	8	–	–	V
I_{CBO}	collector-base cut-off current	$V_{CB} = 8\ V$; $I_E = 0\ A$; $T_{amb} = 25°C$	–	–	100	nA
		$V_{CB} = 8\ V$; $I_E = 0\ A$; $T_j = 125°C$	–	–	50	µA
I_{CES}	collector-emitter cut-off current	$V_{CE} = 8\ V$; $V_{BE} = 0\ V$; $T_{amb} = 25°C$	–	–	100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 6.4\ V$; $I_C = 0\ A$; $T_{amb} = 25°C$	–	–	100	nA
h_{FE}	DC current gain	$V_{CE} = 2\ V$; $I_C = 100\ mA$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	325	–	–	
		$V_{CE} = 2\ V$; $I_C = 500\ mA$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	325	–	–	
		$V_{CE} = 2\ V$; $I_C = 1\ A$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	300	–	–	
		$V_{CE} = 2\ V$; $I_C = 2\ A$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	275	–	–	
		$V_{CE} = 2\ V$; $I_C = 3\ A$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	250	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 500\ mA$; $I_B = 50\ mA$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	–	–	25	mV
		$I_C = 1\ A$; $I_B = 50\ mA$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	–	–	35	mV
		$I_C = 1\ A$; $I_B = 10\ mA$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	–	–	55	mV
		$I_C = 2\ A$; $I_B = 20\ mA$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	–	–	85	mV
		$I_C = 3\ A$; $I_B = 150\ mA$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	–	–	90	mV
		$I_C = 3\ A$; $I_B = 30\ mA$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	–	–	110	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = 1\ A$; $I_B = 100\ mA$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	–	–	1	V
		$I_C = 3\ A$; $I_B = 300\ mA$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	–	–	1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = 2\ V$; $I_C = 2\ A$; pulsed; $t_p \leq 300\ \mu s$; $\delta \leq 0.02$; $T_{amb} = 25°C$	–	–	845	mV
t_d	delay time	$I_C = 2\ A$; $I_{Bon} = 100\ mA$; $I_{Boff} = -100\ mA$; $T_{amb} = 25°C$	–	16	–	ns
t_r	rise time		–	55	–	ns
t_s	storage time		–	190	–	ns
t_f	fall time		–	48	–	ns
f_T	transition frequency	$V_{CE} = 5\ V$; $I_C = 100\ mA$; $f = 100\ MHz$; $T_{amb} = 25°C$	–	80	–	MHz
C_c	collector capacitance	$V_{CB} = 10\ V$; $I_E = 0\ A$; $i_e = 0\ A$; $f = 1\ MHz$; $T_{amb} = 25°C$	–	75	–	pF

The maximum collector-emitter saturation voltage is the next parameter, provided here for different load current conditions, and for values of I_C/I_B equal to 100 and 20. With the stronger base drive at a factor of 20, V_{CEsat} is smaller compared to the lower base current condition.

Very often designers like to know the maximum V_{BEsat} for a load-switch application. Values for two load current scenarios with an I_C of 1 A and 3 A are provided based on an I_C/I_B equal to 10, so a strong base drive. Finally, the parameter V_{BEon} is listed in the Table of characteristics. The operating mode tested for this parameter is V_{CE} = 2 V, while a collector current of 2 A is flowing. The value is shown as a maximum value. This voltage is what a worst-case part requires as turn-on voltage. For the user it is the minimum voltage to be applied.

The next parameters shown are switching characteristics, also called dynamic parameters. Figure 3 shows the test circuit applied. The switching condition chosen is a collector current of 2 A with a base current I_{Bon} of 100 mA and an I_{Boff} of −100 mA. The controlled negative turn-off current via the termination resistors accelerates the turn-off process.

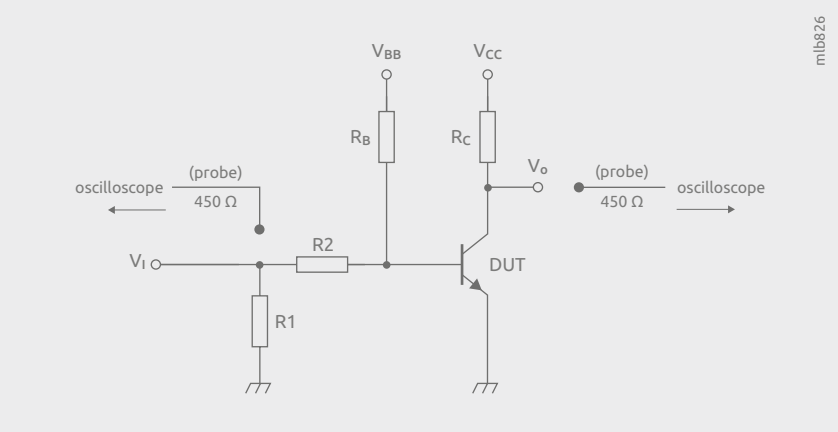


Figure 3 | Test circuit for BJT switching times

In Figure 4 the waveforms for the base current and collector current are depicted. The reference levels for the times tested are 10% and 90% of the related signals. The delay time t_d starts once I_B has reached 10% of the final turn-on current and ends once I_C reaches 10% of the desired on-state value. The time ton starts together with t_d but ends when I_C reaches 90% of the final current.

From the waveform Figure the equation below can be derived:

$$t_{on} = t_r + t_d$$

The sum of rise time and delay time is the turn-on time. Therefore, ton is not listed in the data sheet because it can be calculated easily.

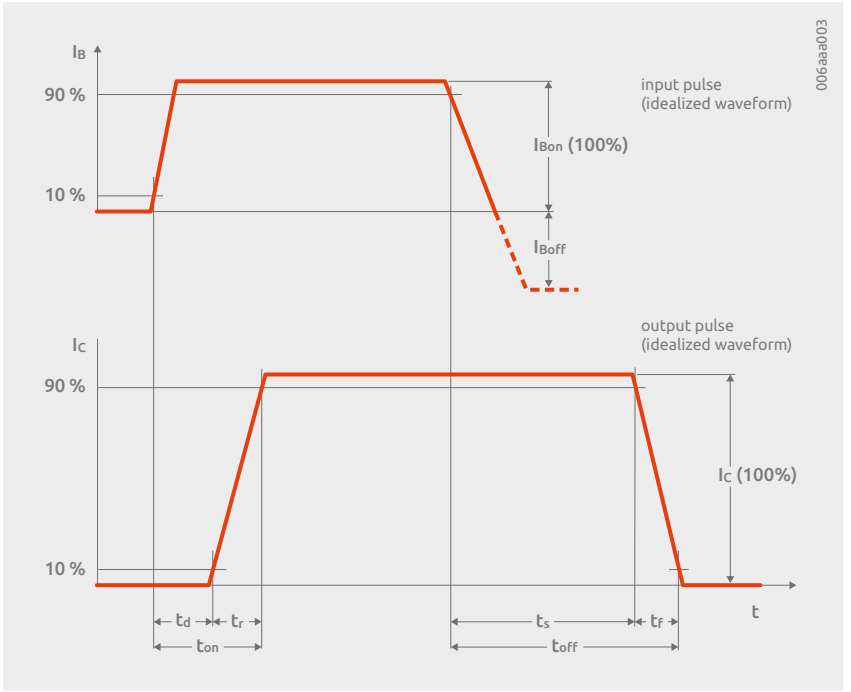


Figure 4 | Switching time definition

For turn-off of the BJT the related times are also shown in Figure 4. The parameters t_s for storage time and tf for fall time are provided in the data sheet table. toff can be calculated with:

$$t_{off} = t_s + t_f$$

The next parameter listed in the characteristics Table is the transition frequency f_T. At this frequency the transistor has a current amplification of 1 or 0 dB, so there is no longer any current amplification. The test condition shows that 100 MHz is applied to the BJT with a collector current of 100 mA and V_{CE} = 5 V as the operating point. As shown in Figure 5, f_T can be derived from the fact that h_{FE} decreases by 20 dB per decade along a linear curve for higher test frequency.

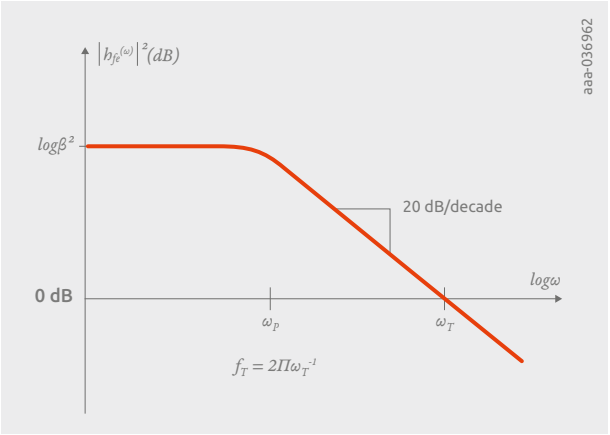


Figure 5 | h_{FE}^2 vs. Ω, Ω = 2π*f

The last parameter provided is the collector capacitance C_C, which is tested with a 1 MHz test signal while V_{CB} is biased with 10 V. Figure 6 shows how this capacitance is measured. C_C is also referred to as C_{OBO} by other BJT vendors. The test signal is applied to a common base circuit as shown, between collector and base; the emitter is kept open. Testing capacitances between two pins and the third pin open leads to the three parasitic capacitances C_{EB}, C_{CE} and C_{CB}.

C_C then puts C_{CB} in parallel to the capacitors C_{CE} and C_{EB} connected in series:

$$C_C = C_{CB} + C_{CE} \times \frac{C_{EB}}{C_{CE} + C_{EB}}$$

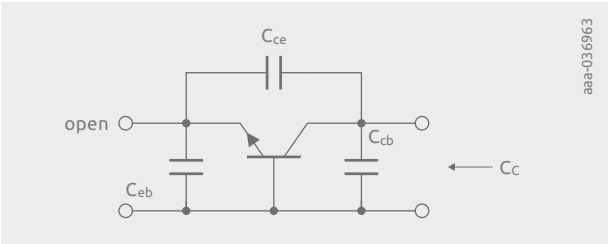


Figure 6 | Parasitic capacitors of a BJT

Many parameters discussed above for a particular operating point or test condition are shown for different operation temperatures with the dependency on collector current or emitter-collector voltage. In Figure 7 h_{FE} as a function of collector current is shown for different ambient temperatures.

For example, for type PBSS4310PAS-Q, it can be seen that the current gain starts to decrease, but above about I_C = 1 A it stays comparably high and stable. h_{FE} increases with temperature as explained in the chapter about the basic physics of BJTs.

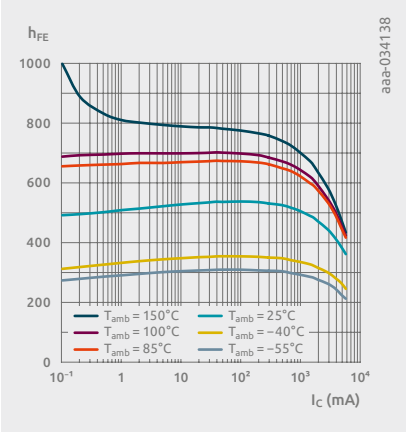


Figure 7 | DC current gain as a function of collector current; typical values

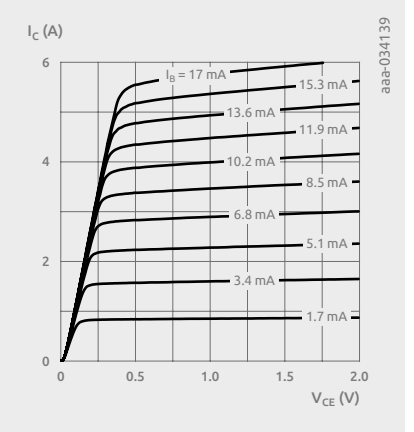


Figure 8 | Collector current as a function of collector-emitter voltage for a fixed I_B; typical values

Figure 8 shows the output characteristic of bipolar transistors, in particular how the collector current depends on V_{CE} for different I_B levels. The curves start with a linear increase of I_C with an increase of V_{CE} and then become almost flat, meaning that I_C is clipped. In the steep part of the curves, the BJT is run in a saturated mode with an almost constant R_{CEon}. If a BJT is used as a load switch, it should be kept in this region and a suitable base current should be applied. Once the collector current starts to clip, the power dissipation of the transistor increases steeply if the current increases further. R_{CE} increases in the clipping region.

Figure 9 and Figure 10 show the V_{BE} saturation voltage as a function of the collector current. Figure 9 shows typical values for a fixed ratio for I_C/I_B of 20 at the ambient temperatures −55°C, 25°C, 100°C and 150°C. For Figure 9, the chosen temperature is 25°C, but I_C/I_B is modified to the values 10, 20, 50 and 100.

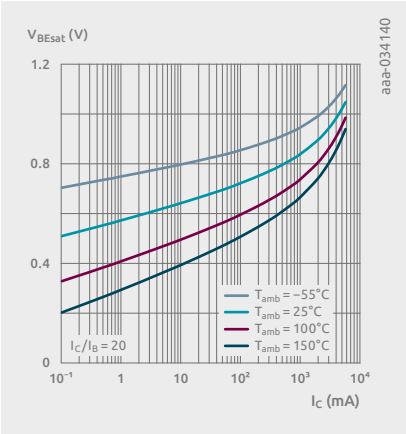


Figure 9 | Base-emitter saturation voltage as a function of collector current; typical values as a function of collector current

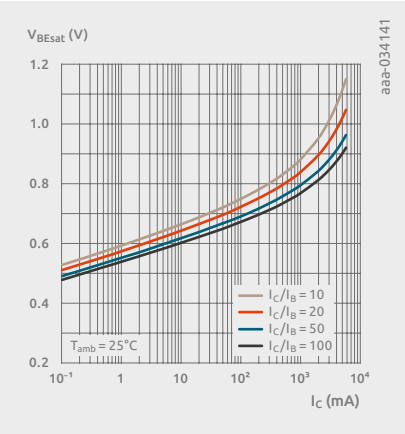


Figure 10 | Base-emitter saturation voltage as a function of collector current; typical values for different I_C/I_B ratios

The next two diagrams show the collector-emitter saturation voltage as a function of the collector current. Figure 11 is based on a ratio of 20 for I_C/I_B and shows the influence of ambient temperature.

In Figure 12 I_C/I_B is modified at T_{amb} = 25°C in steps from 10 to 100.

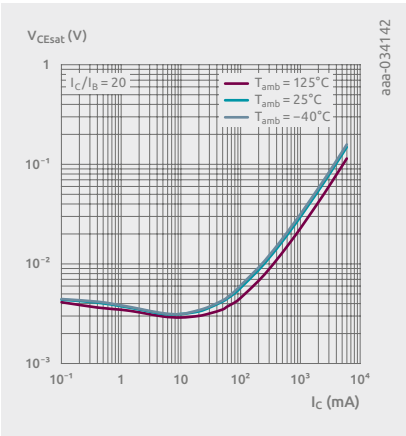


Figure 11 | Collector-emitter saturation voltage as a function of collector current; typical values for different temperature

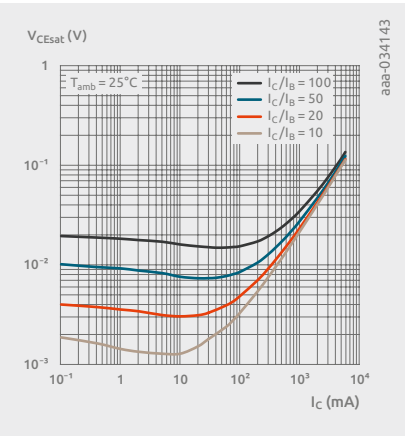


Figure 12 | Collector-emitter saturation voltage as a function of collector current; typical values for different I_C/I_B ratios

Figure 13 and Figure 14 show the on-state resistance R_{CEsat} as a function of the collector current. Figure 13 shows different temperatures and Figure 14 shows different I_C/I_B ratios.

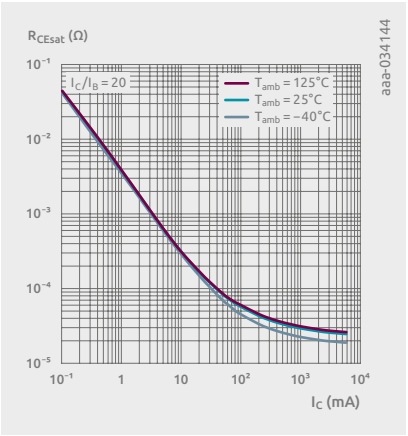


Figure 13 | Collector-emitter saturation resistance as a function of collector current; typical values

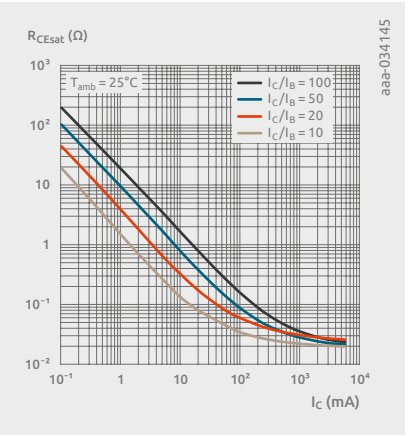
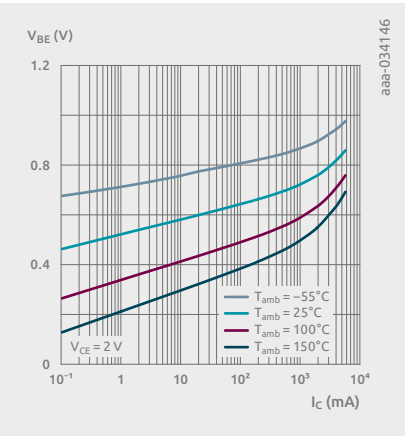


Figure 14 | Collector-emitter saturation resistance as a function of collector current; typical values for different I_C/I_B ratios

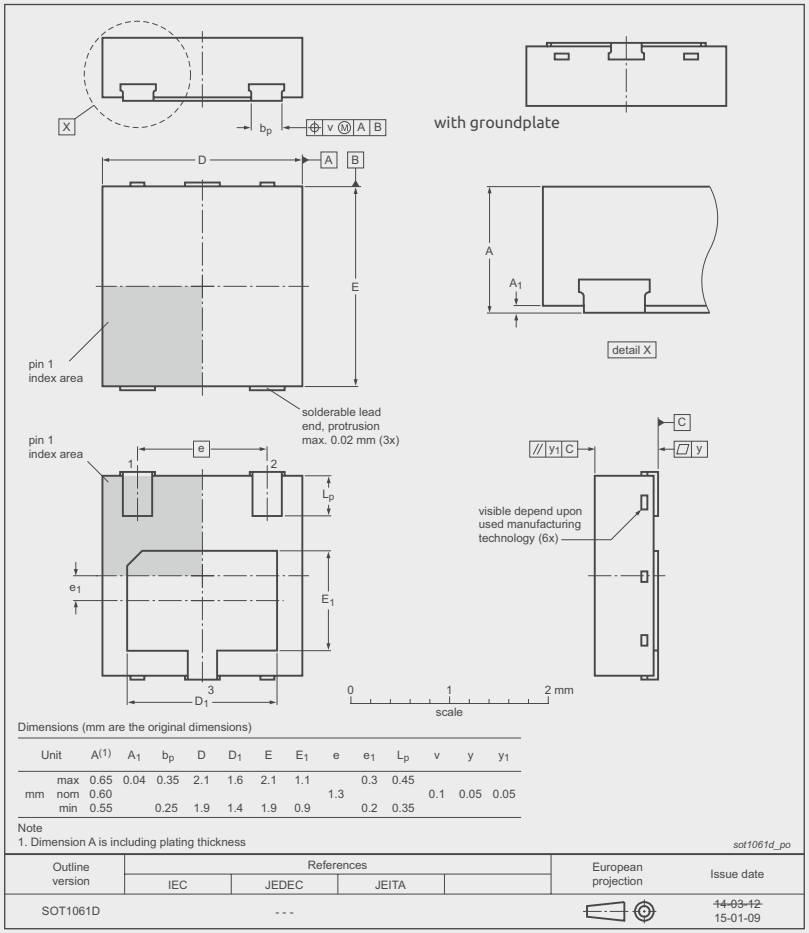
Figure 15 shows which V_{BE} is required to achieve a V_{CE} of 2 V for a desired collector current. Curves from −55°C up to 150°C are shown. At low temperatures a bigger base drive voltage is required because of the negative thermal coefficient of the forward voltage drop of the base-emitter path and a decrease of h_{FE}.

Figure 15 | Base-emitter voltage as a function of collector current; typical values



The next two chapters in the data sheets give information about the package outline and the recommended footprint for reflow soldering.

Figure 16 shows detailed drawings of the package from different projections. The package dimensions are provided in a Table with minimum and maximum values for the most relevant data.



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b_p	D	D_1	E	E_1	e	e_1	L_p	v	y	y_1
mm	max	0.65	0.04	0.35	2.1	1.6	2.1	1.1	1.3	0.3	0.45	0.1	0.05	0.05
	nom	0.60												
	min	0.55		0.25	1.9	1.4	1.9	0.9		0.2	0.35			

Note
1. Dimension A is including plating thickness

sot1061d_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1061D		---			~~14-03-12~~ 15-01-09

Figure 16 | Package outline DFN2020D-3 (SOT1061D)

Figure 17 shows the recommended dimensions of the footprint. The occupied area of the SMD component on the PCB is shown. Furthermore, the areas where no solder resist should be found are shown, with dimensions. Then the so-called solder lands, meaning the copper areas, are defined. Finally, the portions of the solder lands where solder paste should be applied are specified.

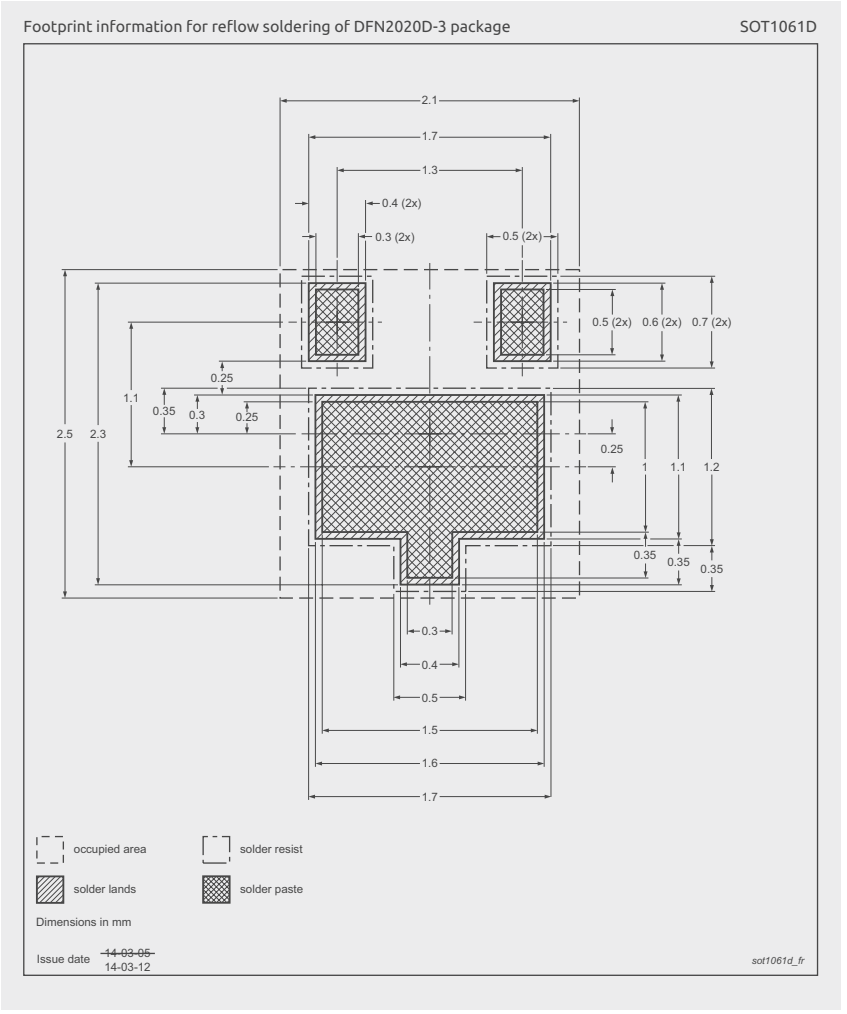


Figure 17 | Reflow soldering footprint for DFN2020D-3 (SOT1061D)

Chapter 4

Thermal considerations

4.1 A BJT as a thermal system

A typical small-signal or medium-power semiconductor device can be broken down into some main components which define the thermal behavior of the device.

Figure 4.1a shows a simple structural drawing of a wire-bonded semiconductor device with its major components: leadframe, semiconductor chip, wire bonding and encapsulation. For some of the more power-oriented package architectures, the wire bond is replaced with clipframe connection, which is more comparable to the leadframe itself. This is shown in Figure 4.1b.

A third class of packages includes additional terminals with comparably large areas to allow for efficient dissipation of heat from the device to ambient temperature, referred to as "package heatsink". A wire-bonded device with a package heatsink is shown in Figure 4.1c. The combination of a package heatsink with a clipframe is also available, for efficient heat dissipation and robust package performance (Figure 4.1d). These are referred to as "clip-bonded packages".

PCBs connect small-signal devices to the environment. They supply electrical power to the device, and they are also the main element to dissipate heat away from the device. For higher-power device packages (e.g., TO220) a second path can be added by introducing a cooling element such as a passive heatsink.

PCBs can have a significant impact on the overall thermal device performance. They can limit the performance of the device or make use of its full potential by smart design of the thermal dissipation paths. For all Nexperia bipolar junction transistors (BJTs), the collector is connected to the leadframe (a vertical device with Si substrate as the collector side), thus forming the main heat dissipation path. There is more about the main heat dissipation path in the following chapters.

PCB design for good thermal behavior is a science of its own, and is beyond the scope of this handbook.

In the upcoming chapters the formal definition of thermal resistances as used by Nexperia will be given. This is followed by considerations relating to the different package architectures and then with some explanations going beyond single-chip semiconductor devices.

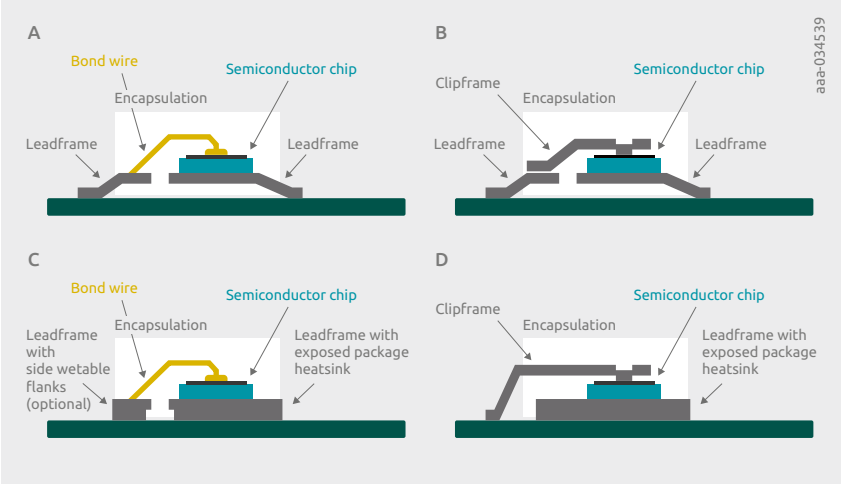


Figure 4 | A: Wire-bonded package, e.g., SOT23 — B: Clip-bonded package, e.g., CFP15 (SOT1289) C: Wire-bonded package with heatsink, e.g., DFN2020D-3 (SOT1061D) — D: Clip-bonded package with heatsink, e.g., LFPACK56 or CFP15

4.1.1 Measurement of thermal resistances

Nexperia measures the thermal resistances of its small-signal devices on standardized PCBs with different footprints. The outcome is commonly visible in the data sheets of the devices as the R_{th}(j–amb) values for different PCBs.

The extraction of R_{th}(j–sp) values follows the transient dual interface method (TDIM) according to JESD51-14. While larger, power-related packages (e.g., D2PAK, TO220) follow the method with a water-cooled heatsink and different interface materials, the smaller packages without a package heatsink follow an alternative method with dedicated PCB layouts instead.

4.1.2 Definition of thermal resistances

The definition of thermal resistance is completely analogous to that of electrical resistance. This analogy helps in many situations to think "thermally" when considering heat dissipation.

Definition:
The resistance R(X–Y) between two physical points is defined as the temperature difference ΔT_{X-Y} between these points divided by the power P_{X-Y} dissipated along the path between points X and Y.

$$R(X-Y) = \frac{\Delta T_{X-Y}}{P_{X-Y}}$$

The reference points X and Y can be any point in the thermal system. In Nexperia data sheets the common situation is for point X to be the junction of the semiconductor device and for point Y to be the solder point of the package or the ambient (temperature). This is shown in Figure 4.2.

In this way Nexperia defines and uses several common R_{th}(j–Y) values, as shown in Table 4.1.

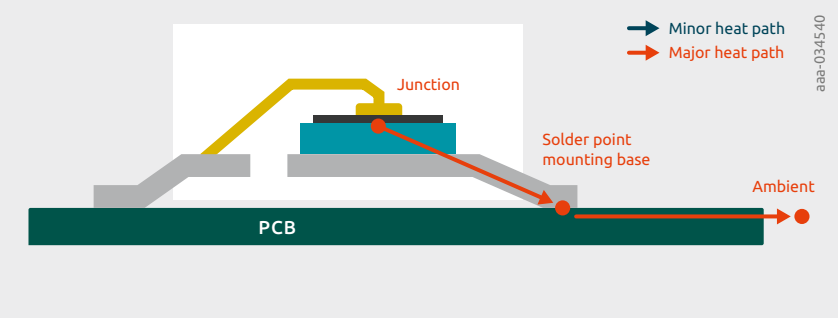


Figure 4.2 | Main heat dissipation path of a wire-bonded package

Table 4.1: Common R_{th} values

Value	Sign	Description
Junction to ambient	R_{th}(j–amb)	Overall thermal resistance of the system including package, solder joints, PCB and optional other thermal design relevant components.
Junction to solder point/ mounting base	R_{th}(j–sp), R_{th}(j–mb)	Thermal resistance of the device. Reference point on the outside of the package is the pin or package heatsink of the main heat dissipation path. *Mounting base* is mainly used for power-oriented packages with a package heatsink, *solder point* is mainly used for smaller SMD or DFN packages.
Junction to top/case	R_{th}(j–top), R_{th}(j–c)	Thermal resistance of the minor heat dissipation path from device junction to the hottest spot on the top surface of the device. This parameter is neither used nor accessible in the real application (see 4.1.6 for details).
Solder point to ambient	R_{th}(sp–amb)	Thermal resistance of the whole system without the packaged device. Reference point on the device side is always the connection point to the main heat dissipation path of the device. Ambient reference point is always the ambient air temperature (commonly 25°C or room temperature).
Coefficient: junction to top	Ψ(j–top)	Coefficient characterizing the temperature difference from device junction to the hottest spot on the top surface of the device in correlation to the overall device power. Strictly speaking, not a thermal resistance (see 4.1.6 for details).

4.1.3 Approximations

Looking at the formal definition of thermal resistance in Chapter 4.2, we can see that for the commonly used Rth values from Table 4.1 some approximations and inaccuracies apply, which are often not mentioned in the field and on data sheets.

Beside the main heat dissipation path shown in Figure 4.2 for a wire-bonded semiconductor device, there are also minor heat dissipation paths, as shown in Figure 4.3.

Looking at R_{th}(j–amb) values, we can use Table 4.1 to calculate the thermal resistance, since in the end all power from the device is dissipated to the ambient between the reference points' junction and ambient.

The first approximation is applied to R_{th}(j–sp) values. The minor power dissipation paths as shown in Figure 4.3 are considered negligible, and their contribution is omitted in the calculation of thermal resistances. In reality, the power dissipated between the reference points is lower than the overall power dissipated at the device.

For wire-bonded devices this approximation is reasonable, since all the minor paths are low in contribution. The situation becomes more complex when looking at clip-bonded or multi-die devices, or even at thermal resistances which are considered minor paths. The next chapters will cover clip-bonded devices and multi-die devices, and will look at the commonly used R_{th}(j–c) or R_{th}(j–top) value.

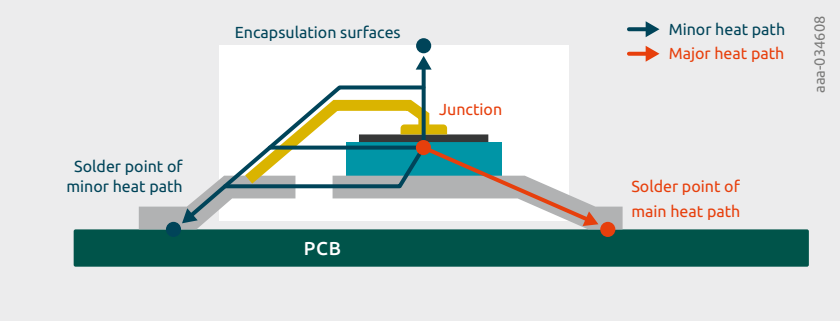


Figure 4.3 | Major and minor heat dissipation paths in a wire-bonded package

4.1.4 Clip-bonded packages

Clip-bonded packages differ thermally in one significant way from wire-bonded packages. The heat dissipation from the junction of the device has two different paths it can follow, as shown in Figure 4.4: along the leadframe, as for wire-bonded packages, and along the clipframe, which is a similarly good dissipation path as through the leadframe. This brings some interesting implications and opportunities in thermal design of the PCB in the application.

First, the definition of a R_{th}(j–sp) value is not as straightforward as for wire-bonded packages. While wire-bonded packages have only one significant dissipation path, clip-bonded packages have two. Looking at the definition of the thermal resistance, this means that the solder reference point is split into two. The thermal resistance of the whole device is now a parallel network of two resistances, which don't necessarily have to be at the same temperature.

Nevertheless, Nexperia follows the same procedure to extract the R_{th}(j–sp) values for clip-bonded devices as for wire-bonded devices (see 4.1.2). The value characterizes the main dissipation path through the die, through the leadframe to the solder point (collector pin of the BJT). This makes the values of clip-bonded products comparable to those of wire-bonded products, if used in a similar PCB layout. Nevertheless, the overall potential of the device is typically higher, since the second path is not used to its full potential while extracting the R_{th}(j–sp) value.

As previously stated, the fact that there is a second significant dissipation path presents opportunities for PCB design. While with wire-bonded devices we are stuck with extracting the heat via a single path (collector pin), here we can use both terminals for clip-bonded devices to effectively remove heat. This helps to improve the thermal performance of the system significantly by offering good thermal paths on the PCB for all terminals.

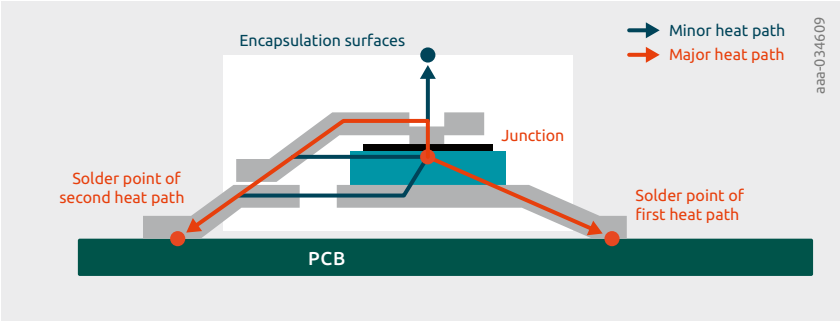


Figure 4.4 | Clip-bonded package containing two major heat dissipation paths

4.1.5 Multiple-chip devices

Devices with more than one chip can be very complex in terms of thermal considerations in live operation, because the operational state of the first chip will influence the (thermal) behavior of the second, and vice versa. Strictly speaking, the R_{th}(j–sp) of the first device is a function of the temperature of the second chip.

Nexperia data sheets provide the R_{th}(j–sp) of one of the chips while the second one is inactive (no heat generation). In this way the R_{th}(j–sp) values of dual- or multi-chip devices are also comparable to single-chip devices, and each chip of the device can be characterized independently. Because the vast majority of multi-chip devices are symmetrical dual-chip devices, we only give one R_{th}(j–sp) value valid for each chip in the device (while the others are inactive).

To give a rough overview of the influence of the second chip in the device, thermal resistances R_{th}(j–amb) are given "per chip" (only one chip active) and "per device" (both chips on the same Tj). These mark the thermal range within which the whole device can be operated.

4.1.6 R_{th}(j–c) and why we call it Ψ(j–top)

The topic of R_{th}(j–c) is in some ways confusing. There are several definitions of this resistance, and most of the time it is not stated clearly what this parameter means. From discussions with customers, Nexperia considers it as the thermal resistance of the device from junction to a package heatsink (e.g., screw hole of TO220, which would be the same as Nexperia's R_{th}(j–sp) or R_{th}(j–mb) values); others refer to it as the thermal resistance from the junction to the top of the plastic body of the package. The latter is discussed in the following.

The question of the R_{th}(j–c) parameter for small-signal devices mostly originates from the question of junction temperature in comparison to the temperature of the plastic body. The application behind this is the measurement of the plastic body temperature with an infrared (IR) camera (or similar) to calculate the junction temperature together with the overall power dissipated in the device. Doing this is perfectly valid, but there are some considerations when doing so. This is why Nexperia calls this parameter Ψ(j–top) and not R_{th}(j–c).

First, we need to know that we are looking at a minor heat dissipation path, which is usually ignored in the overall picture (compare 4.1.3 and Figure 4.3). If we follow the definition of thermal resistance (4.1.1) to calculate the thermal resistance from junction to case (top of the plastic body) R_{th}(j–c) = R_{th}(j–top), we need to take the temperature difference from the junction of the device to the top of the plastic body and divide by the power dissipated along the same (!) path. Now, this is not the overall power of the device in operation, nor is it near to it. It is a fraction of the overall power, which for most of the small-signal devices is below 1% of the overall

power consumption. Or, in other words, the real R_{th}(j–top) is not accessible in real applications, nor is it useful for the purpose of calculating the junction temperature via the top package temperature and the overall device power consumption.

The value in question is not even really a thermal resistance, since temperature difference and power dissipation are between different reference points. Nexperia calls this coefficient Ψ(j-top).

As in the previous chapters about clip-bonded packages or multiple-die devices, we have been talking about a resistor network. The parameter is now dependent on the condition of the reference points. We need to consider that the fractions going through the different heat dissipation paths (major and minor) may shift depending on the ambient conditions, i.e., conditions on the reference points. For example, looking at devices on a PCB with an overall low R_{th}(sp–amb), they are dissipating a higher percentage of the power over the main dissipation path than devices on a PCB with high thermal resistance. Consequently, the relation between these two paths is shifted and the value of Ψ(j-top) changes with the ambient conditions.

This value will be affected not only by the PCB, but also by all ambient conditions which affect the heat transport away from the device. This would be for example forced air flow vs. free air flow, high overall temperature level vs. low overall temperature level, temperature gradients or even heat radiation from nearby surfaces.

The Ψ(j-top) parameter is currently only available on request and there will be no single value, but always a range. The parameter is retrieved via thermal simulations of the system on different PCB layouts (i.e., ambient conditions).

4.2 Thermal impedance and RC modelling

The thermal behavior of discrete semiconductor devices can be predicted using RC thermal models. The model types presented in this application note are known as Foster and Cauer models, and they consist of networks of resistors and capacitors. Foster and Cauer models are equivalent representations of the thermal performance of a discrete device, and they can be used within a SPICE environment. This document provides some basic theory behind the principle, and explains how to implement Foster and Cauer RC thermal models. For convenience, Foster and Cauer RC thermal models are referred to as RC models in the rest of this chapter. Several methods of using RC thermal models, including worked examples, are described.

4.2.1 Thermal impedance

RC models are derived from the thermal impedance (Z_{th}) of a device (see Figure 1). This Figure represents the thermal behavior of a device under transient power pulses. The Z_{th} can be generated by measuring the power losses as a result of applying a step function of varying time periods.

A device subjected to a power pulse of longer than ~1 second, i.e., steady-state, has reached thermal equilibrium and the Z_{th} plateaus and becomes the R_{th}. The Z_{th} illustrates the fact that materials have thermal inertia. Thermal inertia means that temperature does not change instantaneously. As a result, the device can handle greater power for shorter duration pulses.

The Z_{th} curves for repetitive pulses with different duty cycles are also shown in Figure 1. These curves represent the additional RMS temperature rise due to the dissipation of RMS power.

To assist this discussion, the thermal resistance junction to solder point ($R_{th(j-sp)}$) from the PBSS4310PAS-Q data sheet has been included in Table 1. The Z_{th} in Figure 1 also belongs to the PBSS4310PAS-Q data sheet. This graph shows the thermal behavior of a DFN2020D-3 low-V_{CEsat} transistor. The method described can be applied to any other discrete devices, such as diodes or MOSFETs.

Table 1: Steady-state thermal impedance of PBSS4310PAS-Q

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
$R_{th(j-sp)}$	Thermal resistance from junction to solder point			–		7	K/W

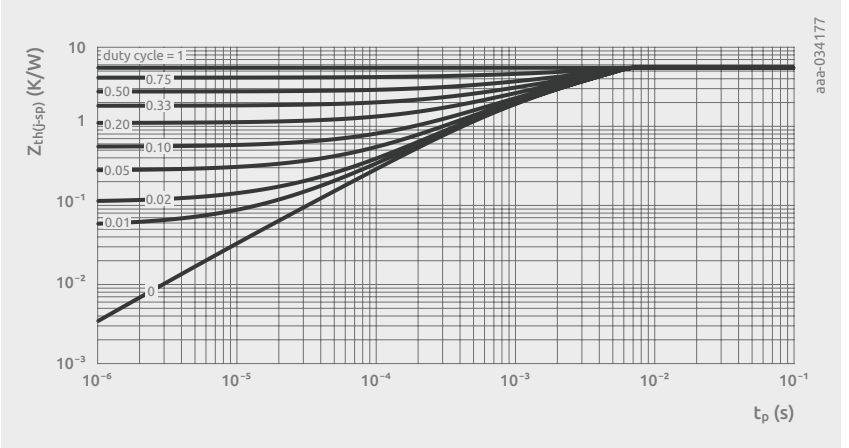


Figure 1 | Transient thermal impedance from junction to solder point as a function of pulse duration for PBSS4310PAS-Q, typical values

4.2.2 Calculating junction temperature rise

To calculate the temperature rise within the junction of a semiconductor device with a single active area (i.e., a heat source at the junction), the power and duration of the pulse delivered to the device must be known. If the power pulse is a square, then the thermal impedance can be read from the Z_{th} chart. The product of this value with the power gives the temperature rise within the junction.

If constant power is applied to the device, the steady-state thermal impedance can be used, i.e., R_{th}. Again, the temperature rise is the product of the power and the R_{th}.

For a transient pulse, e.g., sinusoidal or pulsed, the temperature rise within the device junction becomes more difficult to calculate.

The mathematically correct way to calculate T_j is to apply the convolution integral. The calculation expresses both the power pulse and the Z_{th} curve as functions of time, and uses the convolution integral to produce a temperature profile.

$$T_{j(rise)} = \int_0^{\tau} P(t) \frac{dZ_{th}(\tau - t)}{dt} dt$$

However, this is difficult as the $Z_{th(\tau-t)}$ is not defined mathematically.

An alternative way is to approximate the waveforms into a series of rectangular pulses and apply superposition.

While relatively simple, applying superposition has its disadvantages. The more complex the waveform, the more superpositions that must be imposed to model the waveform accurately.

To represent Z_{th} as a function of time, we can draw upon the thermal electrical analogy and represent it as a series of RC charging equations or as an RC ladder. Z_{th} can then be represented in a SPICE environment for ease of calculation of the junction temperature.

4.2.3 Association between thermal and electrical parameters

The thermal electrical analogy is summarized in Table 2. If the thermal resistance and capacitance of a semiconductor device are known, electrical resistances and capacitances can represent them respectively. Using current as power, and voltage as the temperature difference, any thermal network can be handled as an electrical network.

Table 2: Fundamental parameters

Type	Resistance	Potential	Energy	Capacitance
Electrical (R = V/I)	R = resistance (Ohms)	V = PD (Volts)	I = current (Amps)	C = capacitance (Farads)
Thermal (R_{th} = K/W)	R_{th} = thermal resistance (K/W)	K = temperature difference (Kelvin)	W = dissipated power (Watts)	C_{th} = thermal capacitance (thermal mass)

4.2.4 Foster and Cauer RC thermal models

Foster models are derived by semi-empirically fitting a curve to the Z_{th}, the result of which is a one-dimensional RC network; see Figure 2. The R and C values in a Foster model do not correspond to geometrical locations on the physical device. Therefore, these values cannot be calculated from device material constants as they can be in other modeling techniques. Finally, a Foster RC model cannot be divided or interconnected through for example having the RC network of a heatsink connected.

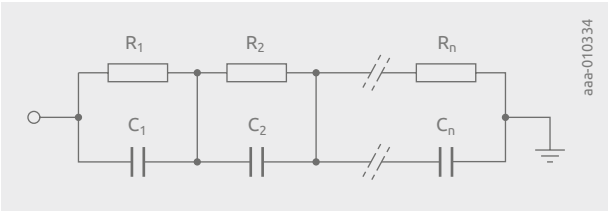


Figure 2 | Foster RC thermal models

Foster RC models have the benefit of ease of expression of the thermal impedance Z_{th}, as described earlier. For example, by measuring the heating or cooling curve and generating a Z_{th} curve, Equation 2 can be applied to generate a fitted curve, as shown in Figure 3:

$$Z_{th}(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}}\right) \text{ where } \tau_i = R_i C_i$$

The model parameters Ri and Ci are the thermal resistances and capacitances that build up the thermal model shown in Figure 2. The parameters in the analytical expression can be optimized until the time response matches the transient system response by applying a least square fit algorithm.

The individual expression "i" also draws parallels with the electrical capacitor charging equation. Figure 3 shows how the individual Ri and Ci combinations sum to make the Z_{th} curve.

Foster models have no physical meaning since the node-to-node heat capacitances have no physical reality. However, a Foster model can be converted into its Cauer counterpart by means of a mathematical transformation.

An n-stage Cauer model can be derived from an n-stage Foster model, and they will be equivalent representations of the device's thermal performance.

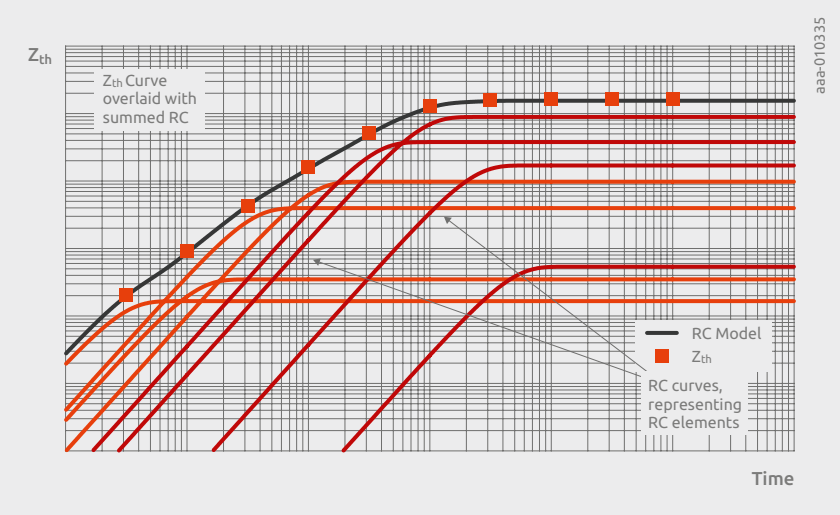


Figure 3 | Foster RC thermal models

As seen for the Foster model, the Cauer model also consists of an RC network, but the thermal capacitances are all connected to the thermal ground, i.e., ambient temperature as shown in Figure 4. The nodes in the Cauer model can have physical meaning and allow access to the temperature of the internal layers of the semiconductor structure.

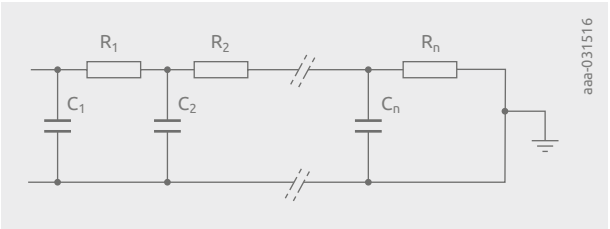


Figure 4 | Cauer RC thermal model

Nexperia provides Foster and Cauer RC models for many of its products on the product information pages, e.g. the bipolar junction transistor (BJT) used as a reference part for this chapter:

- PBSS4310PAS-Q

The models can be found under the "Documentation" and "Support" tabs, as shown for PBSS4310pAS-Q in Figure 5.

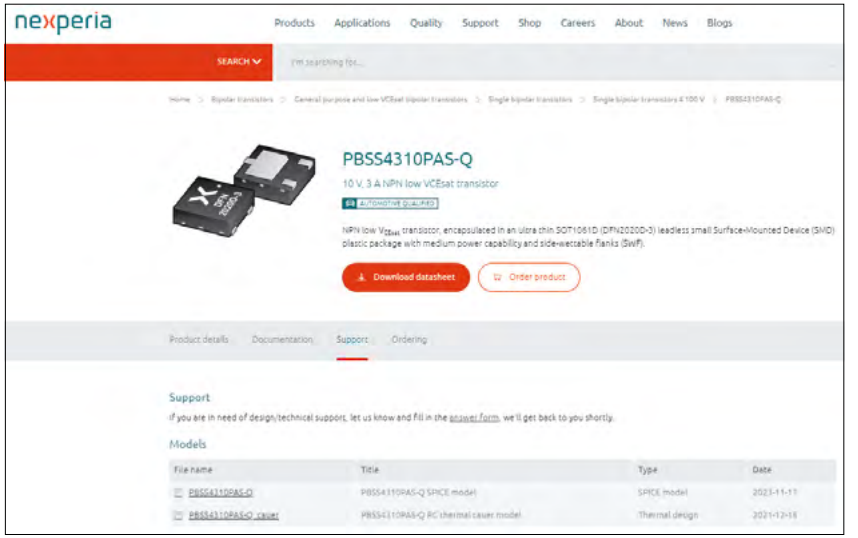


Figure 5 | Nexperia RC thermal model documentation

Foster and Cauer RC thermal models allow application engineers to perform fast calculations of the transient response of a package to complex power profiles.

In the following sections several examples of using RC thermal models are shown. Foster models and Cauer models are equivalent representations of the device's thermal behavior, but in the examples described Cauer models will be used as more representative of the physical structure of the device.

Table 3 shows what the Cauer model looks like in detail for the example BJT chosen.

Table 3: PBSS4310PAS-Q Cauer model netlist

**********			
* Part: PBSS4310PAS-Q			
* Extraction date (yyyy-ww): 2021-51			
* Version: 2v6			
* Cauer style thermal RC network model of $R_{th(j-sp)}$.			
**********			
.subckt cauer 1 4 5			
R1	1	2	1.98625
R2	2	3	3.57064
R3	3	4	0.0249939
C1	1	5	0.000311884
C2	2	5	0.000386809
C3	3	5	0.0143883
.end cauer			

The netlist describes the same Cauer network as in Figure 8, and can be used to build the same schematic. Pin 1 in the netlist can be identified as the junction temperature pin T_j in the schematic. Similarly, pins 4 and 5 are the Tamb pins in the schematic.

In order to simulate only the device pins 4 and 5 will both be tied to the ambient voltage source, as shown in Figure 8.

However, one of the advantages of using Cauer models is that this allows the addition of external networks to the device model, for example to model PCBs, heatsinks, etc. In order to do this, pin 5 will be tied to ambient and pin 4 to the first pin of the external Cauer network. For correct results, it is crucial to make sure that the end pin of the external Cauer network is tied to the ambient source.

4.2.5 Thermal simulation examples

For highest simulation accuracy, all component losses must be considered, depending on the chosen semiconductor technology:

Total losses for BJTs: $P = (V_{CE} \times I_C + V_{BE} \times I_B)$
Total losses for MOSFETs: $P = (V_{DS} \times I_D + V_{GS} \times I_G)$
Total losses for diodes: $P = (V_F \times I_F)$

Example 1

RC thermal models are generated from the Z_{th} curve. This example shows how to work back from an RC model and plot a Z_{th} curve within a SPICE simulator. It allows for greater ease when trying to read values of the Z_{th} curve from the data sheet.

This and subsequent examples use the RC thermal model of PBSS4310PAS-Q. T_{sp} represents the solder point temperature. It is treated as an isothermal, and for this example it is set as 0°C. A single-shot pulse of 1 W power is dissipated in the device. Referring to Figure 7; for a single-shot pulse, the time period between pulses is infinite and therefore the duty cycle δ = 0. Then the junction temperature T_j represents the transient thermal impedance Z_{th}.

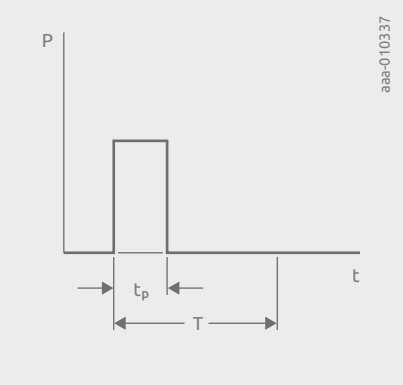


Figure 7 | Single-shot pulse

$$T_j = T_{sp} + \Delta T = 0°C + \Delta T = \Delta T$$
$$\Delta T = P \times Z_{th} = 1W \times Z_{th}$$

Equation 5 demonstrates that with P = 1 W, the magnitude of Z_{th} equates to ΔT. The following steps are used to set up and run simulations:

1. Set up the RC thermal model of BUK7S1R0-40H in SPICE as shown in Figure 8.
2. Set the value of voltage source Vmb to 0, which is the value of T_{sp}.
3. Set the value of the current source I1 to 1.
4. Create a simulation profile and set the run time to 1 s.
5. Run the simulation.
6. Plot the voltage at node T_j.

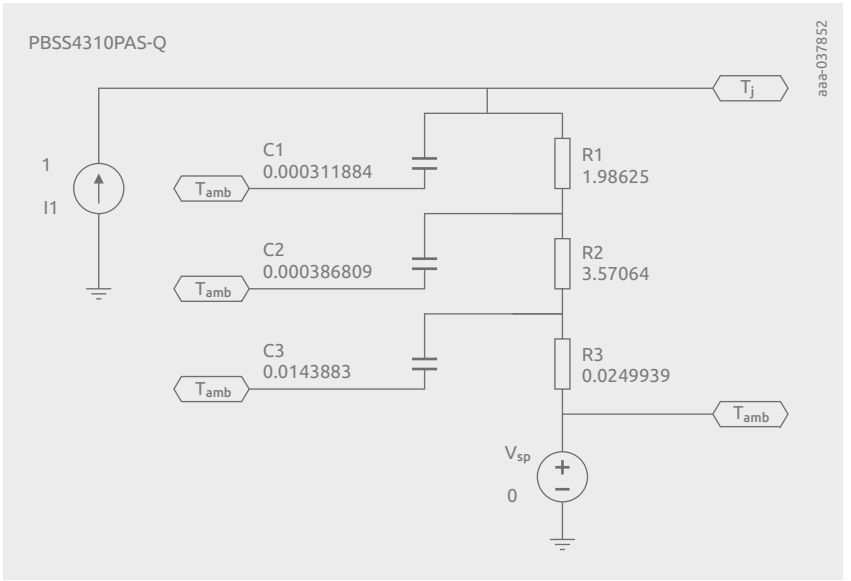


Figure 8 | PBSS4310PAS-Q thermal model setup in SPICE

The simulation result in Figure 9 shows the junction temperature (voltage at T_j), which is also the thermal impedance of PBSS4310PAS-Q in K/W, because a current of 1 A stands for 1 W of power. The values of Z_{th} at different times can be read using the cursors on this plot within SPICE.

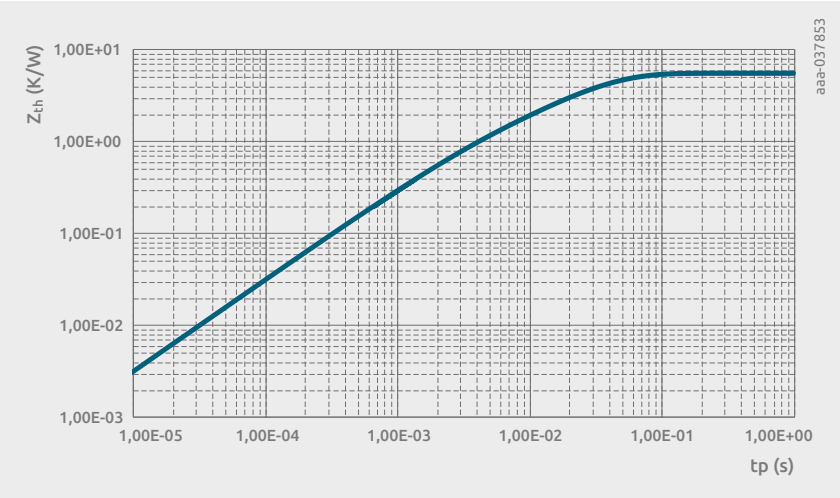


Figure 9 | A plot of Z_{th} as a result of the SPICE simulation for PBSS3410PAS-Q

The value of the current source in this example is set to 1 A to represent 1 W dissipated through the device. It can be easily changed to represent any value of power. The simulation command can be changed for any duration to represent a range of square power pulses.

Example 2

Another method of generating the power profile is to use measurements from the actual circuit. This information is presented to the SPICE simulation in the form of a comma-separated value (CSV) file giving pairs of time/power values. It can be generated either as a summary of observations showing the points of change or from an oscilloscope waveform capture.

Two further methods of generating a power profile are discussed. One method is using a PWL file. The other is to generate the power from a semiconductor device electrical circuit modeled in SPICE. The former is outlined first.

A source within a SPICE simulator can use a PWL file as an input. The contents of a typical PWL file are shown in Table 4. These can list the current, voltage or, as in this example, power over time. These files can be generated by typing values into a spreadsheet editor and saving as a .csv file, or alternatively exporting waveforms from an oscilloscope. The file itself should not contain any column headings.

To implement this procedure within a SPICE environment, follow the same steps as described in Section 6.1 "Example 1", but with the following exceptions:

1. Set the property value of the current source to read from a PWL file and point it to a .csv file, for example: C:\Pulse file\filepulse.csv, which contains the power profile listed in Table 4.
2. Set the mounting base T_{sp} (V_{sp}) to 125°C.
3. Set the simulation run time to 0.6 s.

Table 4: Data example for use in a PWL file

Time (s)	Power (W)
0.000000	0
0.000001	6
0.002000	6
0.002001	2
0.002002	2
0.100000	2
0.100001	2
0.100002	8
0.200000	8
0.200002	8
0.200003	0

Time (s)	Power (W)
0.300000	0
0.300001	8
0.315000	8
0.315001	2
0.400000	2
0.400001	0
0.500000	0
0.500001	6
0.515000	6
0.515001	2
0.600000	2

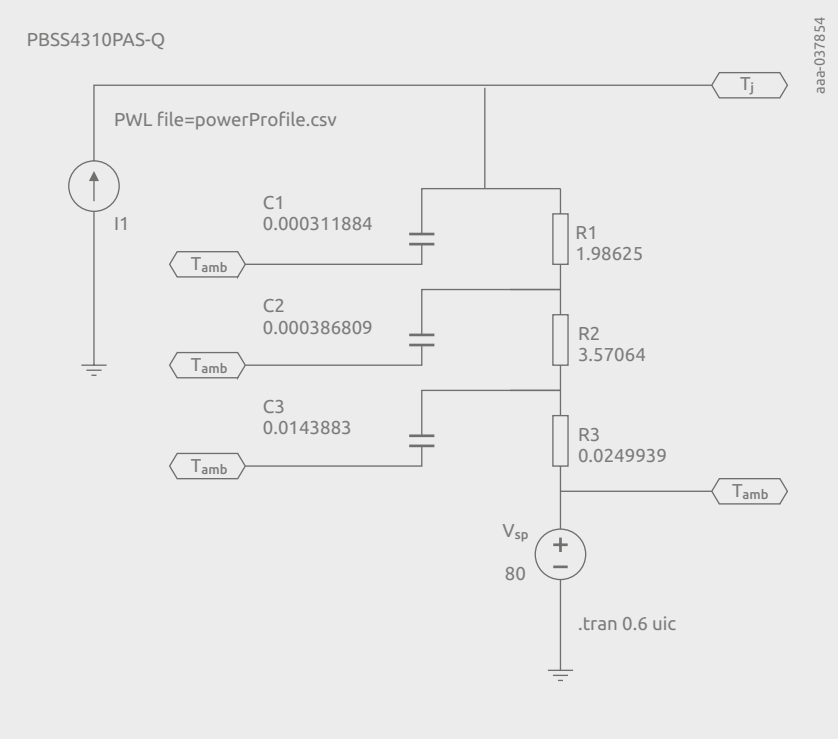


Figure 10 | SPICE circuit implementing a PWL file with the thermal model of PBSS4310PAS-Q

The simulation result is shown in Figure 11. The junction temperature and thermal impedance values labeled in Figure 11 demonstrate that the Z_{th} value at 2 ms, and the R_{th} value, are in line with Figure 12. This represents the thermal impedance waveform shown in the PBSS4310PAS-Q data sheet. The power applied is 6 W and the pulse length Tp is 2 ms. The temperature at the end of the pulse is 98°C. From Figure 12 a Z_{th} of 3 K/W can be derived. The simulated rise in temperature is 18 K. This fits perfectly with $\Delta T = Z_{th} \times P = 3\ K/W \times 6\ W = 18\ K$.

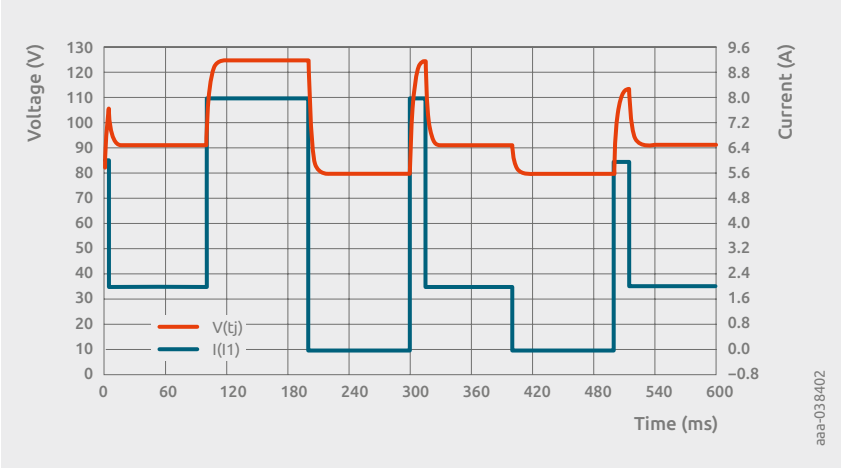


Figure 11 A | Simulation results for 0 s < t < 0.6 s

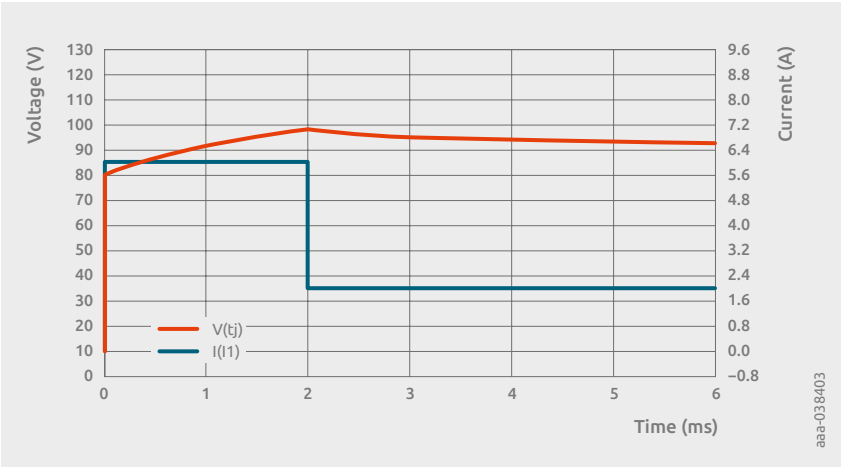


Figure 11 B | Simulation result for first power pulse width Td = 2 ms shown as zoomed view for the first 6 ms

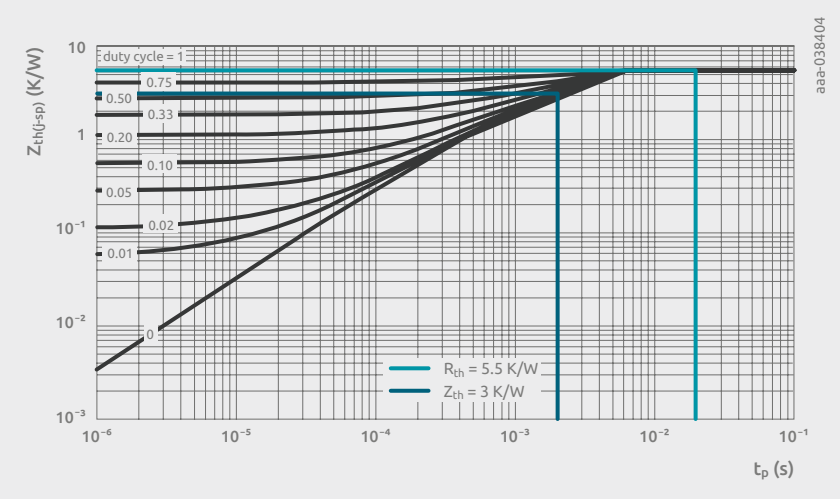


Figure 12 | Thermal transient impedance graph of PBSS4310 with highlighted value at $T_p = 2$ ms and R_{th} for $T_p > 7$ ms

Example 3

The aim of this example is to show how to perform thermal simulation using the power profile generated from a BJT circuit.

Following the steps in Section 6.1, set up the thermal model of PBSS4310PAS-Q, and set the mounting base temperature to 85°C.

To set the power value in the current source, construct a BJT electrical circuit as provided in Figure 13. The power supply is 12 V. The gate drive supply is assigned a value of 10 V. It is set to run for 50 cycles with a 1 ms period and a 10% duty cycle.

The power dissipated in the BJT can be calculated from Equation as:

$$P = (V_{CE} \times I_C + V_{BE} \times I_B)$$

The current source into the thermal model can now be defined as:

$$I = V_C \times I(V_C) + V_B \times I(V_B)$$

Figure 13 demonstrates the link between the electrical circuit and the thermal model circuit.

The resultant plot of the T_j simulation is shown in Figure 14.

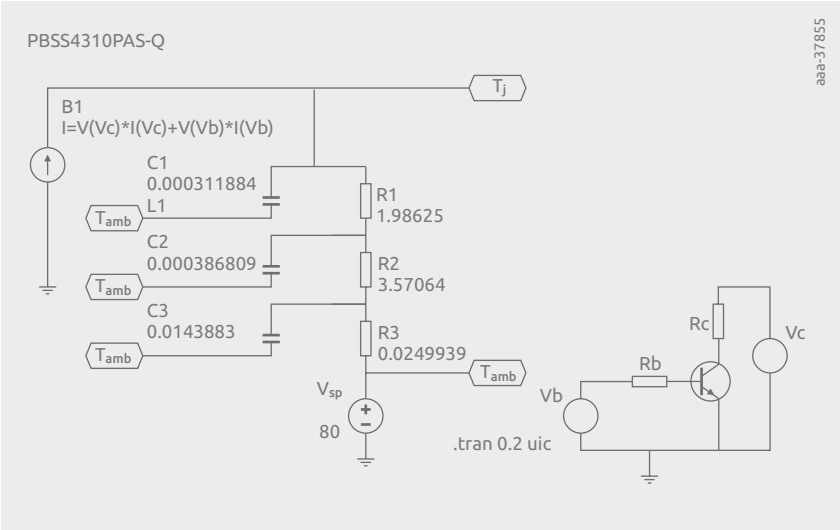


Figure 13 | SPICE circuit illustrating how to integrate an electrical circuit with a thermal model

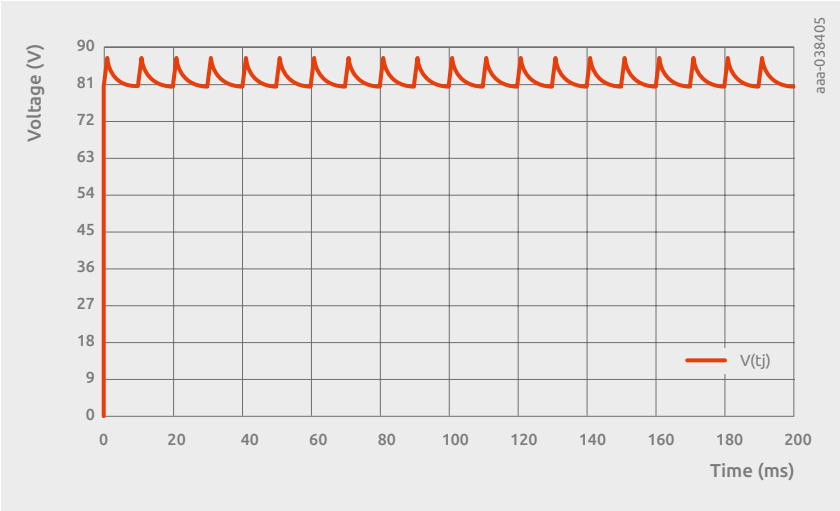


Figure 14 | Inferred junction temperature T_j rise created from the switching operation according Figure 13

4.2.6 Summary

RC thermal models are not perfect. The physical materials used to build semiconductors have temperature-dependent characteristics. These characteristics mean that thermal resistance is also a temperature-dependent parameter, whereas in Ohm's law, the ohmic resistance is usually considered to be constant and independent of the voltage. This means the correspondence between electrical and thermal parameters is not perfectly symmetrical, but it gives a good basis for fundamental thermal simulations.

A further limitation of the models presented is that the mounting base temperature of the device T_{mb} is set as an isothermal. This is rarely the case in real applications where a rise in the mounting base temperature must be considered. This rise is determined by calculating the temperature rise due to the average power dissipation (i.e., the heat flow) from the mounting base through to ambient. It means that the models are of limited use for pulses greater than 1 s, where heat begins to flow into the environment of the device. In this situation, the thermal model for the devices, PCB, heatsink and other materials in proximity must be included.

RC thermal models are available for Nexperia products such as BJTs and power MOSFETs on the Nexperia website. The models can be used in SPICE or other simulation tools to simulate the junction temperature rise in transient conditions. They provide a quick, simple and accurate method for application engineers to perform thermal design.

Chapter 5

BJT packages

Nexperia offers a wide range of SMD packages for bipolar junction transistors (BJTs), ranging from the legacy SOT23 package to the most modern packages in the industry. An overview is shown in Figure 1.

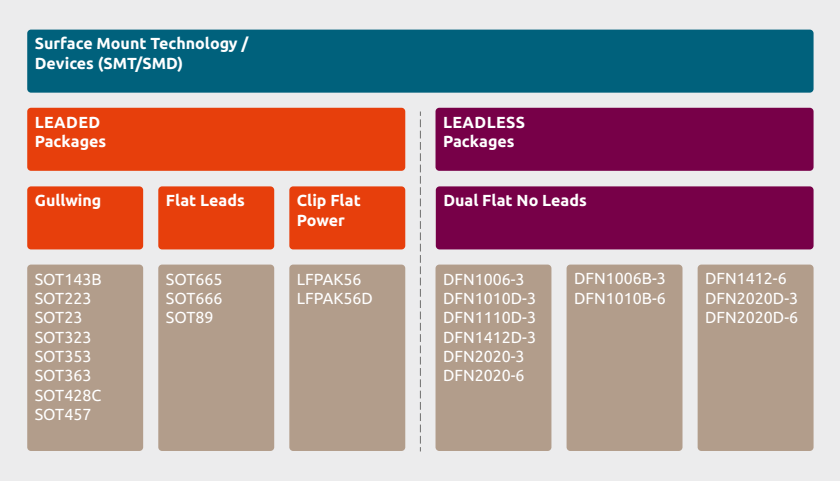


Figure 1 | Categorized overview of Nexperia BJT package portfolio

Through-hole packages were the dominant production technology from the 1950s until the early 1980s, before the introduction of surface-mounted devices (SMDs) to mass production in the 1980s marked a big step forward, leading the way for the cost-efficient production of ever more complex electronic applications thanks to the rapid increase of the component density on a PCB. This was enabled by significant and frequent miniaturization steps at component and board level. For PCBs this meant the steady reduction of the line width of the printed circuit tracks, resulting in a massive increase in the line density, and a steady increase in the number of layers in the PCB. Furthermore, the introduction of SMD products allowed the use of both sides of the PCB for mounting devices.

Surface-mount technology also reduced the parasitic inductances of the products, formerly caused by the long leads of the through-hole packages. This was necessary in order to increase the operating frequencies of the electronic applications.

Development of surface-mount technology started in the 1960s. For Nexperia, the era of SMDs began with the introduction of the popular SOT23 package in 1969, and this still performs well in the market.

In the chapters that follow, the package families Nexperia offers for its BJTs are presented, along with their individual benefits in the applications.

5.1 Leaded packages

5.1.1 Wire-bonded lead packages

Nexperia offers a wide variety of wire-bonded lead packages. These packages are the best choice for standard application requirements where there is no need for enhanced capabilities concerning power, heat dissipation, parasitic inductance or capacitance.

This package family includes the oldest and most common SMD packages in the discrete semiconductor industry, which still represent the largest volume in the market by number of products sold.

All packages in this category (see Figure 2) except SOT665/666 are suitable for wave soldering and reflow soldering. For SOT665/666, only reflow soldering is recommended due to the small pitch of the leads. The quality of the soldering process can be easily monitored by automated optical inspection (AOI). Apart from SOT665/666, all these packages are qualified for automotive use according to AEC-Q101.

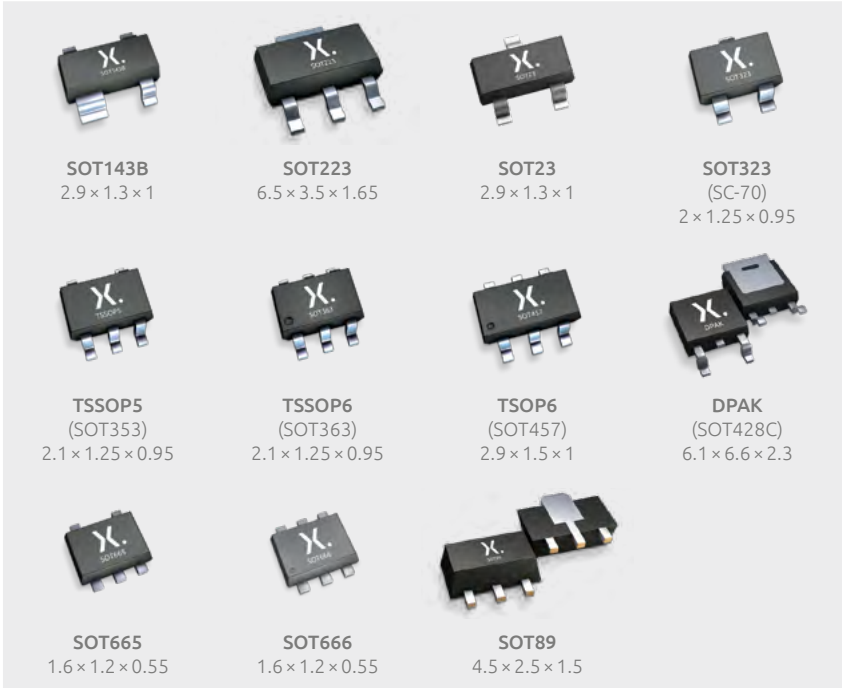


Figure 2 | Nexperia BJT wire-bonded lead packages with outline dimensions

5.1.2 Clip flat power (CFP) packages

CFP packages are designed for increased power requirements. The clip bonding used in these packages reduces the on-resistance of the product due to the enlarged contact areas compared to single-wire bonds. Parasitic inductance is also reduced thanks to the elimination of the wire bonds. Furthermore, the architecture of the clip-bonded packages improves the heat dissipation significantly, making them the preferred choice for power applications.

The CFP packages used for Nexperia's BJTs (see Figure 3) are all qualified for automotive use according to AEC-Q101 and are suitable for reflow soldering.

Due to the strict requirements around power and heat dissipation, clip-bonded packages in 2023 still use solder alloys with high lead content for internal package soldering. These solder alloys are chosen for their unique properties such as high melting points and high thermal conductivity, which ensure the performance and reliability of these packages. Nexperia and other semiconductor manufacturers are working on potential lead-free solutions to replace these alloys and support environmental initiatives.

LFPAK56
(SOT669)
5 × 6 × 1

LFPAK56D
(SOT1205)
5 × 6 × 1

Figure 3 | Nexperia BJT-CFP packages with outline dimensions

5.2 Leadless packages

5.2.1 Leadframe-based dual-flat-no-leads (DFN) packages

DFN packages are the next significant step in miniaturization. They also offer improved performance in terms of parasitic inductance and capacitance due to shorter bond wires and no leads. Furthermore, they show an improved thermal performance by providing one contact pad – or even a large exposed die pad – for direct heat transfer from the silicon to the PCB. The small footprints of DFN packages also simplify PCB trace routing.

For a growing part of Nexperia's DFN package portfolio, alternative pad architectures with side-wettable flanks (SWFs) are offered. These pads are not completely terminated on the bottom side of the product but offer a solderable area at the side wall of the device. This means that after successful reflow soldering, a solder meniscus is visible at the side wall of the device pad. This meniscus can easily be detected using AOI equipment, which makes these packages the preferred choice for applications that need to be extremely reliable.

The DFN packages for Nexperia's BJTs (see Figure 4) are all qualified for automotive use according to AEC-Q101 and are suitable for reflow soldering.

DFN1006-3
(SOT883)
1 × 0.6 × 0.48

DFN1006B-3
(SOT883B)
1 × 0.6 × 0.37

DFN1010D-3
(SOT1215)
1.1 × 1 × 0.37

DFN1010B-6
(SOT1216)
1.1 × 1 × 0.37

DFN1110D-3
(SOT8015)
1.1 × 1 × 0.48

DFN1412D-3
(SOT8009)
1.4 × 1.2 × 0.47

DFN1412-6
(SOT1268-1)
1.4 × 1.2 × 0.47

DFN2020(D)-3
(SOT1061[D])
2 × 2 × 0.65

DFN2020(D)-6
(SOT1118[D])
2 × 2 × 0.65

Figure 4 | Nexperia BJT-DFN packages with outline dimensions

5.3 Soldering techniques

5.3.1 Wave soldering

Wave soldering is the oldest way of mass soldering devices onto PCBs. Wave soldering was introduced when the boards were single sided, and devices used packages with through-hole technology (THT). The packages had pins or wires that penetrated plated holes in the PCB and were wave soldered on the underside of the PCB.

The next evolutionary step was the double-sided PCB with circuitry on both sides of the board. This technology enabled SMD packages to be placed on the solder side of the PCB and fixed with glue underneath the package body. These SMD packages and the through-hole packages were then fluxed and soldered using a wave-soldering process.

With advancing miniaturization in PCB and package technology, wave soldering has increasingly been replaced by new soldering techniques such as reflow soldering. If wave soldering is still required, for mechanical reasons for connectors or large capacitors, for example, selective wave-soldering technologies have been developed which allow the application of a solder wave on very small areas measuring just few square millimeters.

5.3.2 Reflow soldering

With ongoing miniaturization, the need for higher and higher pin counts for integrated circuits (ICs), and the accompanying introduction of new package architectures (QFN, BGA, chip-scale package, etc.), wave-soldering technology was replaced by reflow soldering. Today this is the most common way to mass solder devices on PCBs. The fact that modern package architectures use the area underneath the package body for solder contacts or heatsinks means that wave soldering is no longer an option. Furthermore, the pitch sizes between the contacts have often been reduced to a level which makes reflow soldering a necessity.

Solder paste is printed onto the PCB through a mask (stencil). For very advanced requirements or prototyping there are also tools available for direct solder paste printing (dispenser) – comparable to inkjet printers. Solder paste is a suspension of flux and solder powder. It forms the solder joint between the PCB pad and the device pad after the reflow and fixes the device after the pick-and-place process on the PCB before the reflow. If required, a dot of glue can be applied to the PCB underneath the device to support adhesion. The classification of the solder paste

(determined by parameters such as viscosity and particle size of the solder powder) needs to fit the PCB and stencil characteristics (minimum pad/hole sizes, stencil thickness, etc.).

After solder paste printing and device placement, the PCB – with the devices stuck onto the solder paste – is driven at a defined speed through the heating zones of a reflow oven. The result of these defined conditions is a temperature-over-time profile, which each individual device experiences. For a successful reflow process this temperature profile must fulfill certain criteria:

- Limits in the rate of heat-up and cool-down steps
- Limits for the time period above liquid temperature

The temperature profile depends on many parameters, including the number of PCB layers, the copper density on the PCB, the device size and its thermal mass, to name just a few. It is obvious that the temperature profile will not be the same across the whole board – there will be local differences. This is why the solder reflow process must be optimized for each individual PCB layout. The semiconductor manufacturer can only specify the range of what the temperature profile should look like for an individual integrated circuit or discrete device. The definition of the reflow process is the task of the board manufacturer.

Chapter 6
Quality and reliability

As Nexperia we follow our ZERO quality policy:

- **Z** **ZERO** customer incidents is our ambition
- **E** **EVERYONE** is responsible for quality
- **R** **RECOGNIZED** leadership in quality
- **O** **OBSESSION** for consistent quality

To achieve its ambitions, reliability testing is one of the major considerations for Nexperia during the qualification of products as well as while monitoring production.

Reliability testing can guarantee that products will perform according to their specifications over the specified lifetimes of the electronic applications.

Parts can fail in the field for several main reasons:

- Fundamental wearout of part mechanism (silicon or package)
- Drift in device parameters
- Latent manufacturing defects
- Manufacturing process deviations

Reliability qualification can address only some of these causes of field failures.

Because reliability qualification is a one-time event, it normally does not address issues such as deviations in the manufacturing process or "maverick lots" (a maverick lot is an outlier lot which is still within specifications).

Reliability qualification mainly focuses on:

- Detecting fundamental wearout of part mechanisms
- Detecting design marginality combined with parameter drift
- Determining failure rates due to latent manufacturing defects

6.1 Probability of failure

Figure 1 shows three different types of failure rates: early failure rate (EFR), intrinsic failure rate (IFR) and the wearout period.

The two important periods for the product reliability assessment are EFR and IFR. EFR is a declining failure rate. These are failures due to weak products with macroscopic defects. Meanwhile, the flat portion of the failure rate curve (IFR) consists of random failures, and here the failure rate is relatively constant. This is the behavior observed in large populations of mature parts and is commonly referred to as the useful life of the product.

Wear-out is generally not a concern for well-developed semiconductor technologies.

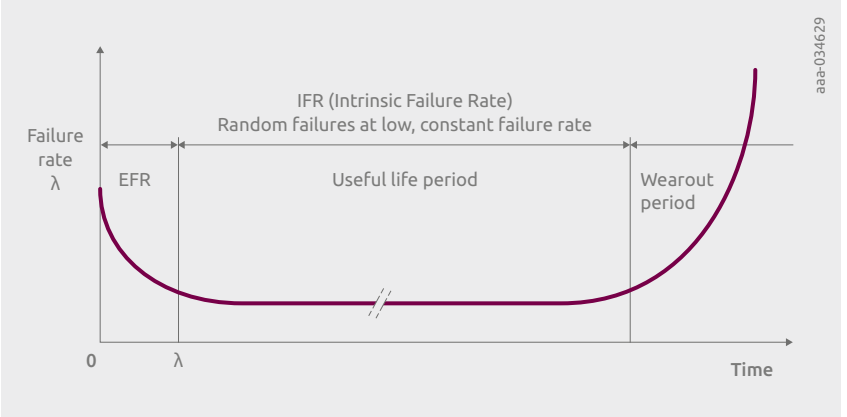


Figure 1 | Plot of typical failure rate over time, commonly known as the "bathtub curve"

6.2 Reliability tests and failure modes

To check the product reliability before a general release to production, several tests are necessary which focus on a calculated accelerated aging of different parts of the product (die, package and interconnections). Acceleration usually takes the form of high temperature or a high applied voltage.

The tests are categorized as follows:

- Manufacture
- Operation
- Thermo-mechanical
- Standby/storage

Reliability tests – manufacturing and design

Table 1: Reliability tests for investigation of failure modes caused by manufacturing and design

Test	Explanation	Conditions
Preconditioning	Simulate temperature and humidity prior to reflow solder (defines the moisture sensitivity level (MSL))	24-hour bake at 125°C, 168-hour humidty storage (85°C/85%), 3x reflow
Solderability	Test proper lead finish (tin) to ensure high-speed soldering	Reflow simulation test: parts placed on non-wetting surface together with solder paste; device may be pre-aged by 8-hour steam or 16-hour dry bake
Solder heat	Test ability to withstand immersion during wave soldering[1]	Immerse in Pb-free solder bath for 30 seconds

1: This test is not carried out for products that are not suitable for wave soldering, e.g. DFN-packages.

Potential failure modes:

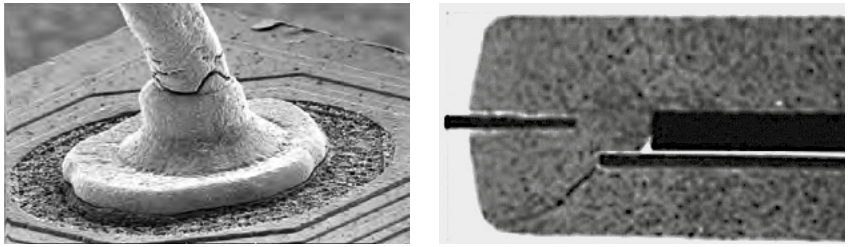


Figure 2 | Potential failure modes can be caused by manufacturing: broken stitch (left), package crack (right)

Reliability tests – operation

Table 2: Reliability tests for investigation of failure modes caused during operation

Test	Explanation	Conditions
HTRB	High-temperature reverse bias *Acceleration:* Arrhenius model, temp., V_{bias}	Oven at 150°C, 1,000 hours, max. reverse bias
HTOL	High-temperature operating life *Acceleration:* Peck model, temp., V_{bias}	Oven at 150°C, 1,000 hours, max. forward bias

Potential failure modes:

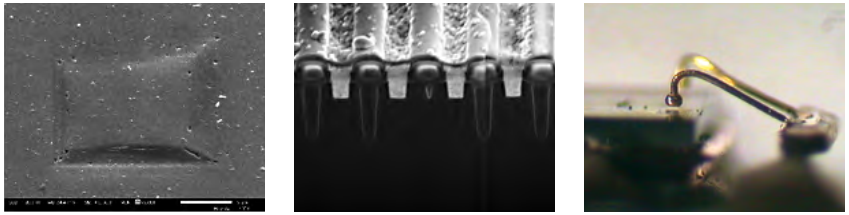


Figure 3 | Potential failure modes during device operation: crystal defects (left), incomplete trench (center) and lifted bond due to intermetallic corrosion (right)

Reliability tests – thermo-mechanical

Table 3: Reliability tests for investigation of failure modes caused by thermo-mechanical stress

Test	Explanation	Conditions
TC	Temperature cycling *Acceleration:* Coffin-Manson, dT	Dual climate chamber at up to −65°C, +150°C device swaps every 20 minutes, 1,000 cycles
IOL	Intermittent operational life *Acceleration:* Coffin-Manson, dT	Electrical test rack, device powered on/off every 2 minutes, min. temp swing: 100°C (due to P_{tot} during ton); 15 kcycles
TS	Temperature shock Like TC but with liquid baths *Only for development purposes, not for qualification*	Dual climate chamber at up to −65°C, +150°C

Potential failure modes:

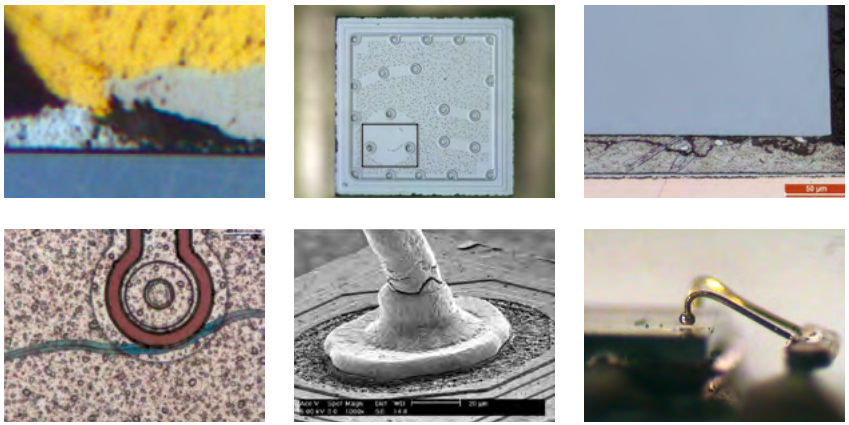


Figure 4 | Potential failure modes caused by thermo-mechanical stress (from left to right on top and bottom rows): intermetallic corrosion, cracks in silicon caused by wire bonding, cracks in bond line, cracks in passivation layer, broken wire, lifted bond wire

Reliability tests – standby/storage

Table 4: Reliability tests for investigation of failure modes caused by exposure to harsh environment

Test	Explanation	Conditions
H3TRB	High humidity/high temperature reverse bias Acceleration: Hallberg-Peck model, temp., %RH, V_{bias}	Climate chamber, 1,000 hours, 85°C, 85% rH, biased at 80% of rated breakdown voltage
AC	Autoclave *Acceleration:* Hallberg-Peck model, temp., %RH	Pressured steam chamber 96 hours, 121°C, 100% rH, 1 bar
UHAST	Highly accelerated stress test *Acceleration:* Hallberg-Peck model, temp., %RH, unbiased	Pressured steam chamber 96 hours, 130°C, 85% rH, 1.5 bar
HAST	Highly accelerated stress test *Acceleration:* Hallberg-Peck model, temp., %RH, V_{bias}	Pressured steam chamber 96 hours, 130°C, 85% rH, 1.5 bar, biased at 80% of rated voltage

Potential failure modes:

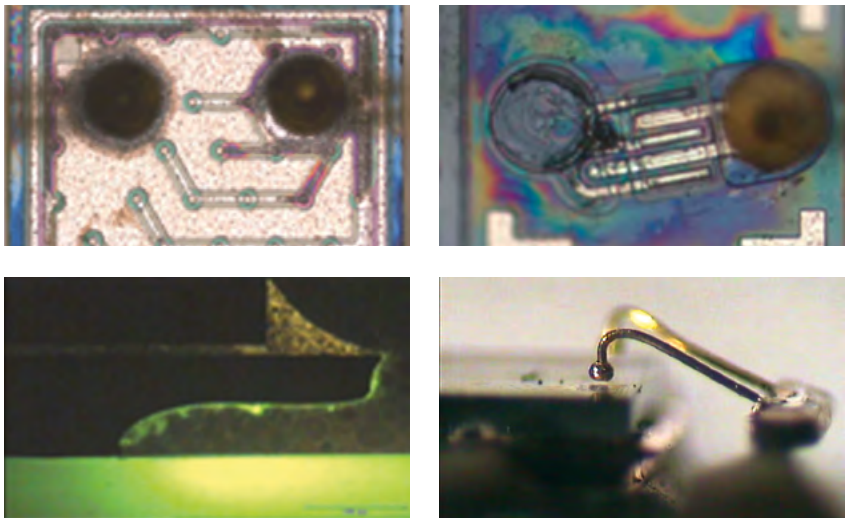


Figure 5 | Potential failure modes caused by exposure to humidity and harsh environment: corrosion (top row), moisture penetration into package, lifted bond (from left to right)

During qualification, Nexperia never runs all these listed tests, as some of them duplicate each other with higher stress levels or extended test duration.

During the setup of Nexperia's qualification strategy, and in parallel to this test selection for a new product family, it also considered a structural similarity approach to allow it to perform reliability tests on specific products from the new product family (e.g., smallest and biggest die within a certain family from the same wafer process).

For reliability testing Nexperia uses its Reliability Qualification Specification as well as the related JEDEC standards for the different tests.

6.3 Automotive-grade qualification

Aside from its large consumer-/industrial-grade qualified portfolio, Nexperia has released most of its parts with AEC-Q101 certification, the official automotive qualification guideline.

The difference between the reliability tests for consumer/industrial and automotive products is the test duration (e.g., 500 cycles vs. 1,000 cycles TC) which results in a guarantee of longer product lifetime of the automotive qualified products.

6.4 Mission profiles

A product's intended application area is characterized by a mission profile (MP), which is a collection of relevant environmental and functional loads that a product will be exposed to during its full life cycle.

Nexperia uses the following generic MPs:

- Automotive for discrete devices, according to AEC-Q101
- Non-automotive, based on MP for Industrial, Infrastructure, Infotainment from Nexperia internal standards and JESD47
- Non-automotive, based on MP for Consumer, Commercial from Nexperia internal standards and JESD47

If the customer MP deviates from the generic MPs, Nexperia is happy to work closely with the customer to calculate and align on the test conditions and duration to meet the customer's expectations.

6.5 Nexperia's high robustness specification

Nexperia's aim is to produce high-quality products. Therefore, it defines its High Robustness Specification accordingly. This document describes the qualification requirements for products to be released as "High Robustness Products", which can be used in extreme automotive customer applications such as engine control units or gearboxes.

On top of AEC-Q101, Nexperia runs some stringent tests:

2x AEC-Q101:
The test time of all reliability tests according to AEC-Q101 or -Q100 (whichever is applicable) must be extended by a factor of 2.

Zero delamination:
The products must not show any sign of delamination of the mold compound from any other component of the device (e.g., leadframe, clip, wire, die) after pre-conditioning according to MSL 1.

PCB bending test:
The products must withstand at least 1.0 mm of PCB bending according to IEC-60068-2-21. In addition, the maximum possible bending deflection before the parts fail electrically must be determined.

Vibration test:
A vibration test in accordance with IEC60068-2, 64 using the specified conditions must be passed.

Drop test:
A drop test using the following conditions must be performed: pulse width (measured at 10% of amplitude): 0.5 ms +/−30%, $C_{pk} > 1.33$, acc. peak 1500 g +/−20%, $C_{pk} > 1.33$ (see Figure 6). The samples are monitored electrically throughout the test. The number of samples to be tested are 135 per (leader-)type, distributed on nine test boards.

Power thermal cycling:
The PTC test is a combination of TC and IOL, which leads to a high stress at the interconnection between PCB and product. 2600 PTC test cycles are required.

- TCT condition: −40°C to 105°C, 90 minutes/cycle
- IOL condition: Seven powered component cycles (5 minutes on, 5 minutes off) with a temperature rise of 30 K ±2 K between solder joints of the component on the PCB and an aluminum base plate attached to the PCB are required.

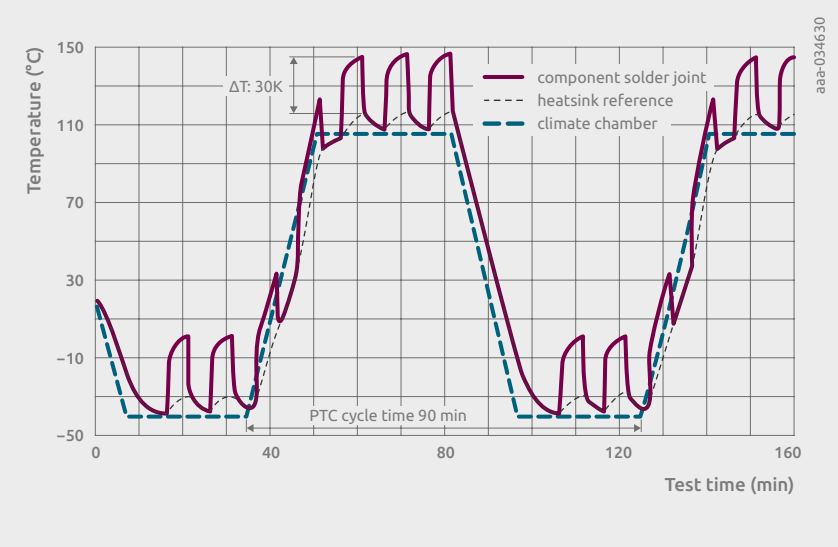


Figure 6 | Power temperature cycling – a very specific test combining TC and IOL, which leads to a high stress at the interconnection (solder joints) between PCB and product

For any questions on Nexperia's qualification strategy, please contact Nexperia.

6.6 Wiring during reliability test

During HTRB and H³TRB, the maximum HTRB, respectively 80% of the maximum (H³TRB) collector-emitter voltage, is applied to the respective pins. When the base pin is left open, this can result in an unstable configuration and the transistor can turn on, which due to the high voltage may lead to damage of the transistor. Therefore, the base is also biased in the reverse direction, protecting the transistor from this state (see Figure 7). The base emitter reverse bias is normally 1 V.

Figure 7 | Bis setting during HTRB/H3TRB

For intermittent operation life (IOL), the device shall be operated such that the junction temperature during the on-time is more than 100°C higher than the ambient temperature (normally 25°C). In order to find the operation conditions, first the power consumption necessary to reach this junction temperature must be found. This is done by using the definition of the thermal resistance:

$$R_{th} = \frac{\Delta T_j}{P_{tot}} \quad with \quad \Delta T_j = T_j - T_A \geq 100°C$$

Rearranging this equation leads to:

$$P_{tot} = \frac{\Delta T_j}{R_{th}}$$

Rth is taken from the data sheet. The values specified in the data sheet are maximum values and the typical values are 15% lower than that. Assuming a typical R_{th} of 360 K/W and aiming for a ΔT_j of 110°C (to be safely over 100°C), the required power is calculated as:

$$P_{tot} = \frac{110\ K}{360\ K/W} = 306\ mW$$

This power is applied to the transistor using the circuitry shown in Figure 8. First the emitter resistor R_E is chosen. The value itself is not important for the test, but is must be ensured that the resistor is not overloaded according to its specifications. For this example, 135 Ω is chosen.

By impedance matching, the emitter current I_E is then set so that $P_{RE} = P_{Transistor}$ = 306 mW. It follows that:

$$I_E = \sqrt{\frac{P_{RE}}{R_E}} = \sqrt{\frac{306\ mW}{135\ \Omega}} = 48\ mA$$

As $P_{RE} = P_{Transistor}$ and $I_{RE} \approx I_{CE}$, it follows that:

$$V_{CE} = V_{RE} = \frac{P_{tot}}{I_E} = \frac{306\ mW}{48\ mA} = 6.38\ V$$

The supply voltage U_b is set to $U_b = V_{RE} + V_{CE} = 6.38\ V + 6.38\ V = 12.76\ V$, following the impedance matching requirement.

The base resistors R_{B1} and R_{B2} are chosen from one of the combinations $R_{B1}/R_{B2} = 220\ \Omega/270\ \Omega$ for supply voltages $U_b < 12\ V$ and $R_{B1}/R_{B2} = 470\ \Omega/560\ \Omega$ for supply voltages $U_b \geq 12\ V$. These resistors ensure that the base current is supplied in order to turn the transistor on.

After these operation points are set, the surface temperature of the device case is checked. The case temperature lies slightly below the junction temperature, so during this check the case temperature must be around 125°C to ensure that the junction temperature is more than 125°C (but not exceeding 150°C). If the case temperature is too low or too high, the settings are recalculated using an adapted P_{tot}.

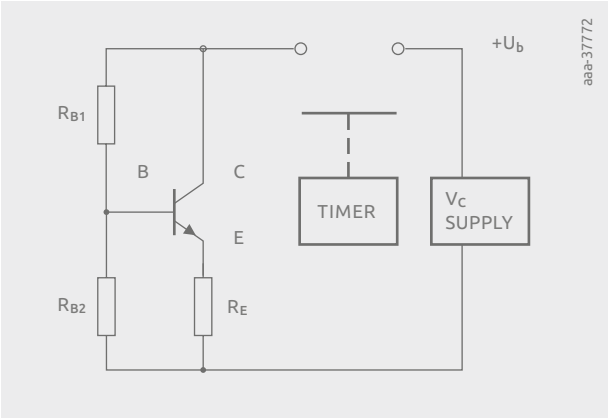


Figure 8 | Circuitry for IOL test of transistors – the timer switches the supply voltages on and off for 2 minutes, respectively (following the requirements of AEC-Q101)

Chapter 7
Application examples

7.1 Basic BJT circuits

There are three basic circuit configurations for operating bipolar junction transistors (BJTs), as shown in Figure 1. The circuits have an input and output port. Because a BJT has only three terminals, one contact is used in common for the input and output. This BJT pin defines the name of the basic configuration.

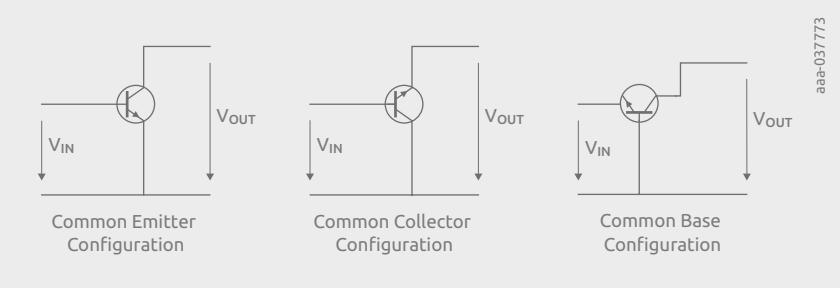


Figure 1 | Basic BJT configurations

In more complex BJT circuits, the input and output do not necessarily have a common node at the BJT pin. The configuration is denoted after the BJT pin, which is connected to neither the input nor the output signal of the related transistor stage. Figure 2 shows a simple example of a two-stage BJT circuit in a common emitter configuration to clarify this approach. The base of the transistor Q1 is connected to the input signal. The output of Q1 is the collector, which is connected to the base of the PNP transistor Q2 via a series resistor. Q1 and Q2 work in a common emitter configuration.

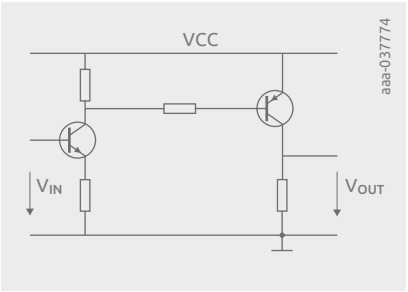


Figure 2 | Non-inverting transistor stage with two BJTs in emitter configuration

The common emitter configuration is most frequently used in amplifier circuits because it provides good voltage and current, and therefore also power gain. For an input voltage change in the positive direction the output reacts in the other direction. This means the output signal has a 180-degree phase shift toward the input. This is why the complete circuit in Figure 2 does not invert the input signal, because two common emitter stages are put in series.

Current gain β is defined as:

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Table 1 shows a comparison of key parameters for amplifiers realized with the three BJT basic configurations discussed above.

Table 1. Overview of key circuit parameters for the three basic BJT configurations

	Configuration		
Parameter	Emitter	Base	Collector
Input resistance	Medium	Low	High
Output resistance	Medium	High	Low
Voltage amplification	High	High	<1
Current amplification	High	<1	High
Phase input to output	180°	0°	0°
Bandwidth limit	(Medium) small	High	Medium

The common base configuration has a low input impedance because the input signal is connected to the emitter. The input current is applied to the emitter, so the stage has the current amplification of:

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

Because I_E is the sum of I_C and I_B, it is higher than I_C. This means that α is always smaller than 1. Below, the relationship between β and α is given:

$$\beta = \frac{\alpha}{(1-\alpha)} \quad and \quad \alpha = \frac{\beta}{(\beta+1)}$$

The common base configuration is mainly used for impedance matching and in RF circuits. This configuration has a low input impedance and high output impedance, which limits the application usage. The voltage amplification is like the common emitter configuration.

The common collector configuration is very often used and is better known as emitter-follower. Voltage amplification is slightly below 1, so approaches unity. The common collector circuit approach is ideal to realize a low-impedance output stage with a rather high ohmic input. At the emitter, which is the output, the current is the sum of I_C and I_B. This means that the current amplification equals:

$$A_i = \frac{I_E}{I_B} = \frac{(I_C + I_B)}{I_B} = \beta + 1$$

This sum is roughly the value of β itself because β is in the region of 100 or higher.

7.1.1 Common emitter circuit examples

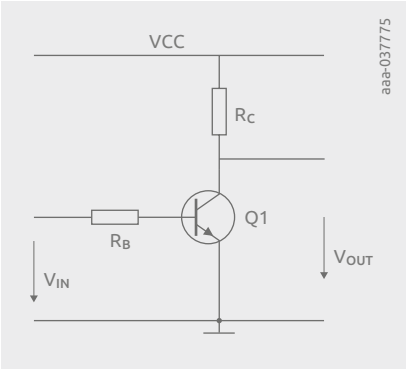


Figure 3 shows a simple application example with a common emitter configuration. The BJT is driven via a series base resistor R_B, and at the collector a load resistor R_C is applied to the supply voltage VCC.

Figure 3 | Common emitter circuit with series base resistor R_B and collector load resistor R_C

The circuit shown in Figure 4 was simulated with the general-purpose NPN transistor BC847B. The base emitter voltage V_{BE} and V_{OUT} are shown in Figure 5, dependent on the input voltage V_{IN}. From V_{IN} of about 0.55 V upward the BJT starts to conduct and V_{OUT} is dropping with a comparably steep transition, after the falling-edge V_{OUT} becomes almost stable at a low level. The BJT is run in saturation mode and is fully turned on. In this mode the base-collector diode is run in forward conduction. The difference between the green trace for V_{IN} and the V_{BE} is increasing, showing the voltage loss at R_B. This loss is equal to $I_B \times R_B$. The operating region left of the saturation mode is referred to as "normal mode".

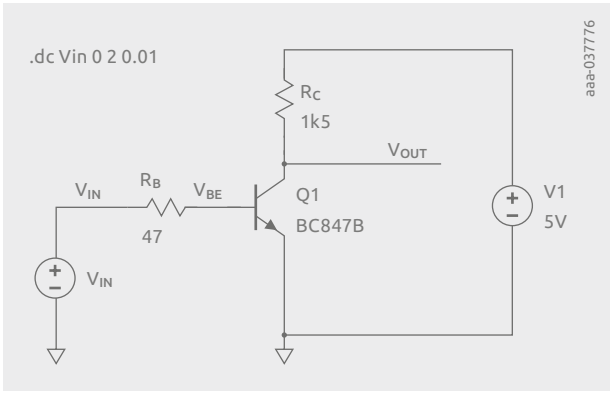


Figure 4 | Spice circuit diagram with BC847B

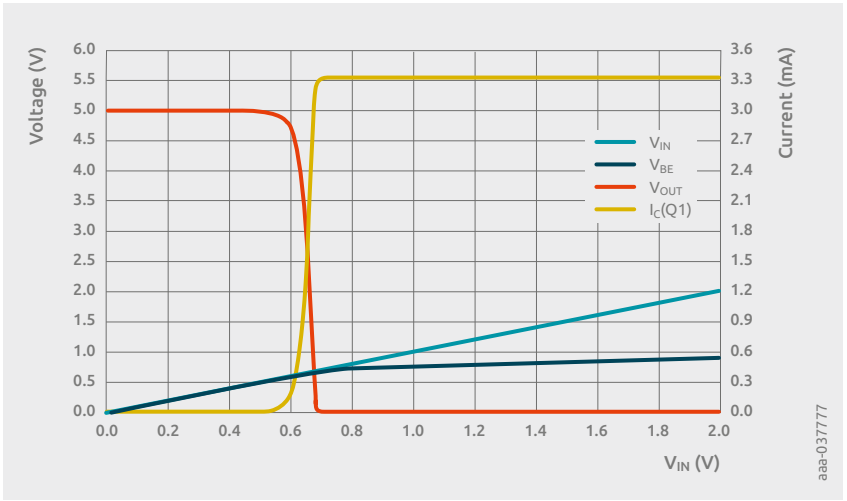


Figure 5 | Spice simulation results of the circuit shown in Figure 4

The circuit without a load V_{OUT} follows the equation:

$$V_{OUT} = V_{CC} - R_C \times I_C$$

In the region of the normal mode the loss at R_B can be ignored because of the low base current, which means that V_{BE} is almost equal to V_{IN}.

$$V_{BE} \sim V_{IN}$$

For a linear amplifier the operating point should be in the middle of the transition of the V_{OUT} curve to allow maximum range for positive and negative input voltage deviation. Voltage amplification for small-signal operation is:

$$A = \frac{\Delta V_{OUT}}{\Delta V_{BE}}$$

This formula can be written as:

$$A = -\Delta I_C \times \frac{R_C}{\Delta V_{BE}} = S \times R_C$$

S is the steepness that I_C changes vs. V_{BE} at the operation point:

$$S = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{I_C}{V_T}$$

VT is the so-called "thermal voltage". It can be calculated with the formula:

$$V_T = \frac{kT}{q}$$

the value for BJTs is about 26 mV at room temperature, with k the Boltzmann constant (1.380649×10^{-16} VAs/K), T the absolute temperature and q the elementary charge (1.602×10^{-19} As)

With R_C = 1.5 kΩ and I_C = 1.6 mA

S = 61.5 mS –> A = –92

From the Spice simulation shown in Figure 5, the voltage amplification can be derived. If we ignore the impact of R_B and expect that $V_{BE} \sim V_{IN}$,

$$A = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{(3.45\ V - 0.15\ V)}{-0.035\ V} = -94$$

The simulation result is close to the theoretical value.

The input resistance R_{IN} at the operating point is equal to

$$\frac{\Delta V_{IN}}{\Delta I_{IN}} \sim \frac{\Delta V_{BE}}{\Delta I_B} = \frac{\beta}{S}$$

For the example circuit discussed above with a BC847B, R_{IN} is 282/61.5 kΩ = 4.6 kΩ.

R_{OUT} is equal to R_C, or 1.5 kΩ.

Figure 6 shows that the location of the transition area in the output voltage curve of the simple amplifier circuit shifts significantly over temperature, since the forward conduction curve of the base emitter diode shifts with roughly –2 mV/K (–1.9 mV/K in simulation). This shift at the input is amplified by factor A, so that the operating point at the output shows a massive change over temperature. It is obvious that the operating point needs to be stabilized if the BJT is to be used as a linear amplifier. It is not a problem if the circuit is to be used as a switch only. In this case the input voltage needs to be small enough to allow turning off at high temperatures and high enough to safely turn on at low temperatures.

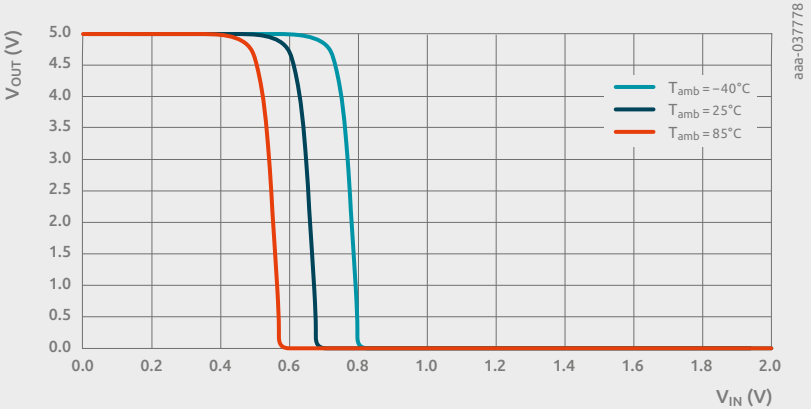


Figure 6 | V_{OUT} versus V_{IN} for different ambient temperatures

Nonlinearity and thermal drift can be reduced by means of negative feedback. It is very common to introduce current feedback with an additional emitter resistor R_E, as shown in Figure 7.

With an increased I_C the voltage drop at R_E also becomes larger, and the voltage of the emitter increases. With this effect the transistor gets a reduced base drive, and the amplification is reduced compared to the basic circuit in Figure 3.

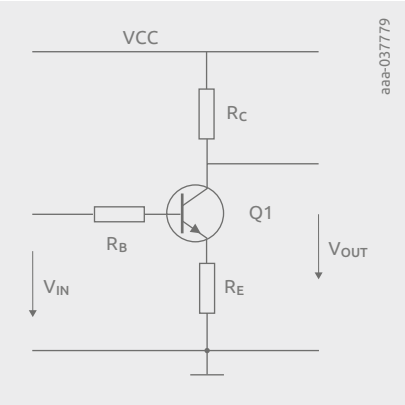


Figure 7 | Common emitter circuit with current feedback

The circuit example from Figure 8 is simulated with Spice. The transition from VCC to the voltage of the saturated mode is less steep than in the circuit without negative feedback. The voltage in saturation mode cannot go as low anymore because of R_E. $V_{OUT(min)} = (VCC - V_{CEsat}) \times R_E/(R_C + R_E) + V_{CEsat}$.

In Figure 9 the simulation results for V_{OUT}, V_B and V_{IN} are shown vs. V_{IN}. V_{IN} is included as a curve to show that V_B and V_{IN} start to have an increasing voltage difference if the BJT starts to saturate.

If we ignore the voltage loss at R_B and assume that V_{BE} is roughly 0.7 V once the base emitter diode conducts, it can be stated for the linear part of V_{OUT}:

$$V_{OUT} \sim VCC - \frac{R_C}{R_E}(V_{IN} - 0.7\ V)$$

This formula shows a steepness factor for the output voltage curve which is the small-signal voltage amplification. This factor A equals $-R_C/R_E$, the ratio of the collector resistor to the emitter resistor. The current feedback has the big advantage that the amplification depends on the ratio of resistors, which are linear components, and not on the nonlinear behavior of the transistor. For proper design of the circuit, production spread also does not play an important role. In saturation mode the base collector diode conducts, and the base current is split and increases significantly with further increase of V_{IN} but is limited by R_B.

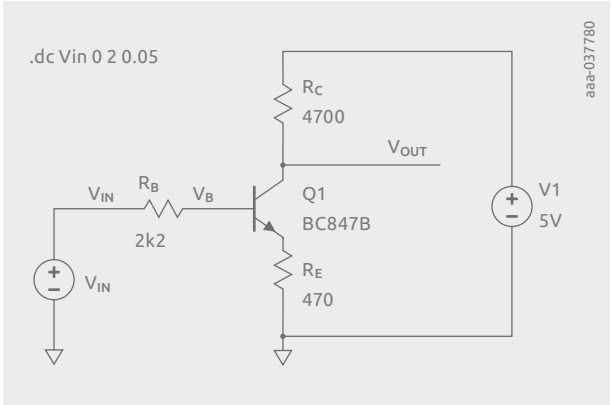


Figure 8 | Spice simulation example with a current feedback emitter circuit

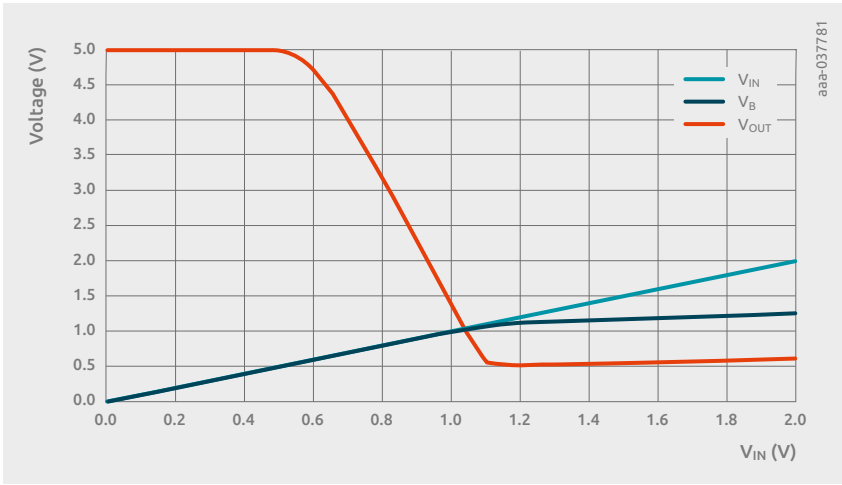


Figure 9 | Spice simulation results for the circuit example shown in Figure 8

The circuit diagram from Figure 7 can be converted into a small-signal equivalent circuit, as shown in Figure 10. The BJT itself is the components inside the dotted box with a current source controlled by the current $S \times V_{BE}$. Parallel to this current source a resistor r_{CE} is placed.The resistor r_{BE} represents the base emitter resistance at the operating point and r_{CE} is a resistor between the collector and emitter. Additionally, the external circuit resistors R_B, R_E and R_C can be found.

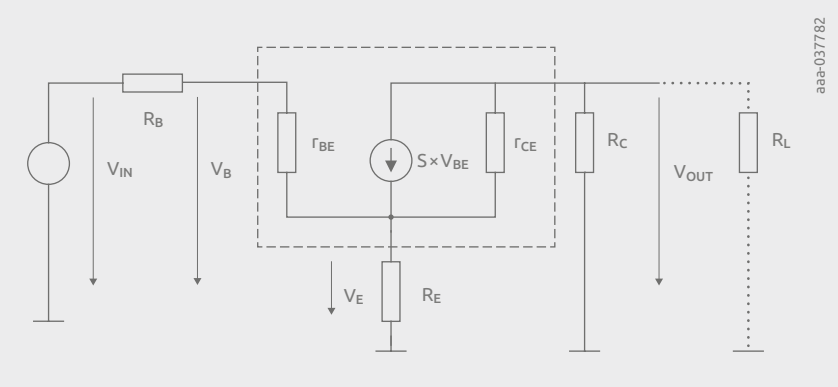


Figure 10 | Small-signal equivalent circuit – Figure 7 amplifier approach

Key facts for the common emitter configuration with current feedback, assuming that ß ≫ 1, $r_{CE} \gg R_C$, R_E and that there is an open output (RL not present):

$$A = \frac{-S \times R_C}{(1+S \times R_E)} \quad for \quad S \times R_E \gg 1 \rightarrow A \sim -\frac{R_C}{R_E}$$

$$re = \frac{V_B}{I_B} \sim r_{BE} + ß \times R_E = r_{BE}\,(1 + S{*}RE)$$

$$rA \sim R_C$$

With the negative current feedback the amplification A is reduced compared to a circuit without the emitter resistor RE. Thermal stability of the operating point is therefore much improved.

As an alternative to the current feedback, a voltage feedback can be realized by introducing a resistor from the collector to the base, as shown in Figure 11. R2 connects the collector of the BJT to the base, and the output voltage is coupled back to the input. R2 works as a negative feedback and reduces the amplification, because the lower the collector voltage becomes due to higher base drive the more R2 reduces this base drive.

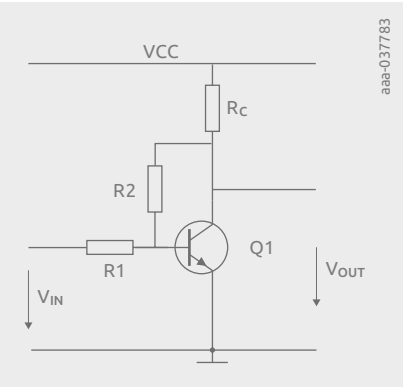


Figure 11 | Common emitter circuit with voltage feedback

A circuit example as shown in Figure 12 has been simulated with Spice. The value 2.2 kΩ has been chosen for R1. R2 has twice the resistance of R1, meaning 4.4 kΩ. The collector resistor is realized with the value of 1 kΩ. The input voltage V_{IN} ranges from −2 V to +2 V.

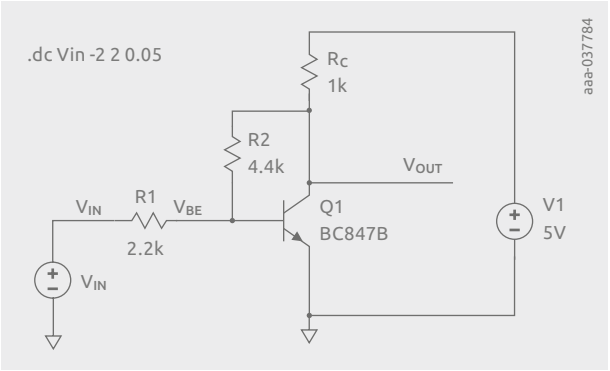


Figure 12 | Spice simulation example with a common emitter circuit with voltage feedback

In Figure 13 the simulation results are shown for V_{OUT}, V_{BE} and V_{IN} as a reference curve. The output voltage curve (red trace) has a linear region, and it can be seen that the steepness is much less than the output voltage curve from Figure 5, which showed an amplifier stage without feedback. V_{IN} must be negative to turn off the BJT entirely. This can be seen with the collector current curve (light-blue). Below about V_{IN} = −1.2 V no base current flows. Above this voltage V_{BE} starts getting clipped at about 0.6 V, with the base emitter diode conducting.

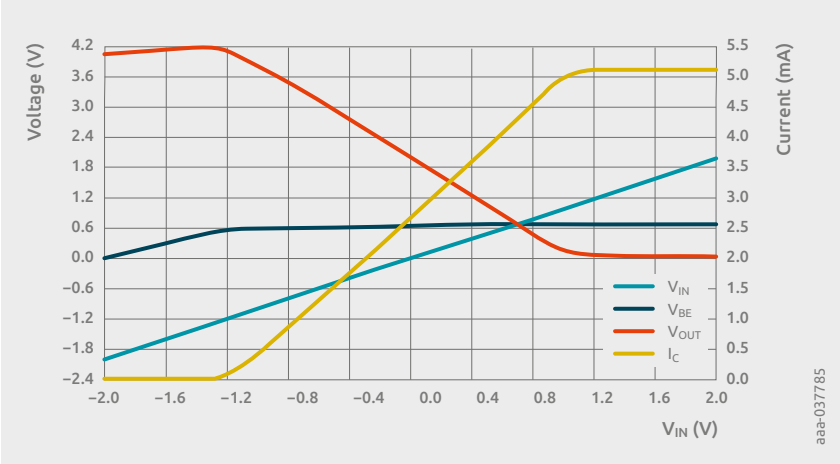


Figure 13 | Spice simulation results for the circuit example shown in Figure 11

From the nodes in the circuit diagram the following equations can be derived according to Kirchhoff's current law.

Base node: $(V_{IN} - V_{BE})/R1 + (V_{OUT} - V_{BE})/R2 = I_B$

Collector node: $(VCC - V_{OUT})/R_C + I_{OUT} = (V_{OUT} - V_{BE})/R2 + I_C$

As a third equation it is known that $I_C = B \times I_B$

With these equations and the facts $B \gg 1$ and $BRC \gg 1$ and having no load resistor connected:

$$V_{OUT} \sim \frac{VCC \times R2}{B \times R_C} + (1 + \frac{R2}{R1})\, V_{BE} - (\frac{R2}{R1}) \times V_{IN}$$

V_{BE} is almost constant in the linear output voltage region (blue trace is almost flat with about 0.7 V). This means that the input to output voltage depends mostly on the ratio –R2/R1, so again a ratio of resistors and not nonlinear BJT parameters, as for the current feedback solution.

For many applications it is not required to amplify a DC input voltage. Audio applications are a very obvious example. The lowest frequency that a human ear can perceive is about 20 Hz. If capacitors are placed at the input and output of an amplifier stage, the DC operating point can be chosen independent of bias voltages in the input signal, and the DC level of output signal is not linked directly to a following amplifier stage or to the output load. Thermal drift of one amplifier stage does not change the operating point of a following stage. However, the AC coupling introduces high-pass filters into the signal chain. The chosen capacitors need to be large enough in capacitance to support a cutoff frequency which is low enough for the targeted use case.

In Figure 14 a common emitter circuit with current feedback and AC-coupled input and output is shown. The same approach can be used for a current feedback configuration according to Figure 11.

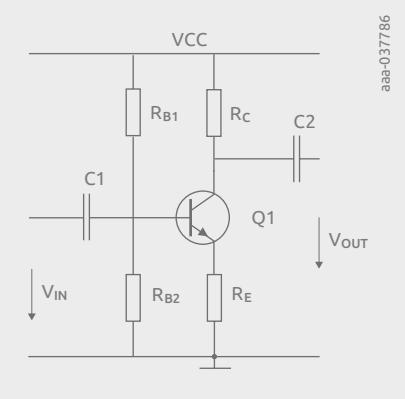


Figure 14 | Common emitter circuit with current feedback and AC-coupled input and output

The thermal drift is reduced if a feedback with an emitter resistor or a resistor put between collector and base is used. In either case, the thermal drift of V_{BE} is amplified, with the amplification factor of the transistor stage remaining, which is R_C/R_E for the current feedback solution. For an AC-coupled amplifier which cannot amplify DC content from the input signal it is not necessary to realize a rather high DC amplification. Therefore, the feedback can be made frequency dependent. Thermal drift is normally a slow process. In Figure 15 an example for an amplifier is shown, where the emitter resistor is split. For AC signals R1 is short-circuited by the capcitor C3. This means that the AC-amplification factor is about R_C/RE, whereas the DC amplification is $R_C/(RE + R1)$ only.

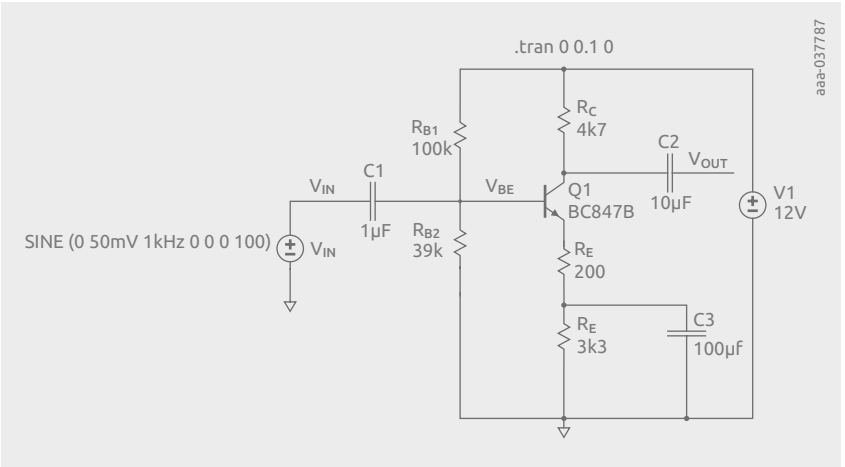


Figure 15 | Spice example for a common emitter circuit with small DC amplification and higher AC gain with frequency-dependent feedback approach

The current through the base divider should be significantly higher than the base current to safeguard a stable bias voltage. The operating point at the collector should be adjusted such that the AC signal has the maximum symmetrical range. At the emitter a voltage of roughly $V_{BE} - 0.7$ V can be expected. The current through the resistors at the emitter is then $I_E \sim (V_{BE} - 0.7\ V)/(R_E + R1)$. The collector current is $I_C = I_E - I_B$. With $I_B \ll I_E$ it can be assumed that $I_C \sim I_E$. The collector voltage is the supply voltage $VCC - I_C \times R_C$. The value of R_C needs to be chosen such that the desired DC operating point is realized. VOP should be put roughly to the voltage $VOP = VCC - VCC \times (1 - (R_E + R1)/(R_C + R_E + R1))/2$. In our example 12 V – (12 V(3.5 kΩ/8.2 kΩ))/2 ~ 8.5 V.

In Figure 16 the simulation results are shown. The signals at the BJT are shown, rather than V_{IN} and V_{OUT} behind the coupling capacitors so that the DC bias voltages can be seen. The circuit amplifies a 100 mVpp 1 kHz sine wave signal to about 2 Vpp at the output. Due to the BJT's base emitter resistance rE, the amplification is a little smaller than 23.5 (R_C/R_E). Increasing R_C can easily compensate for this effect.

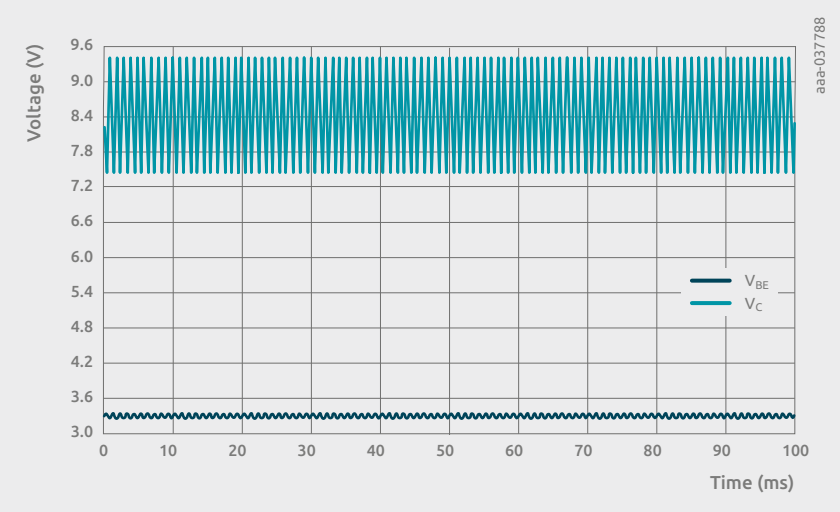


Figure 16 | Spice simulation of the amplifier shown in Figure 15

7.1.2 Common collector circuit applications

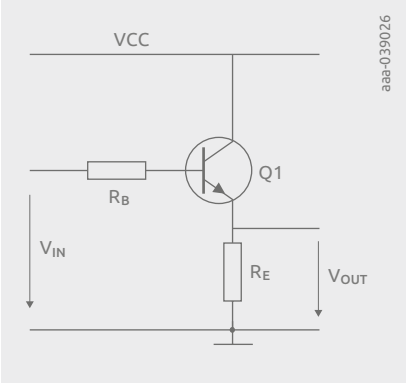


Figure 17 shows a common collector circuit with a base resistor and an emitter resistor. The circuit was simulated with Spice using 100 Ω for R_B and 220 Ω for R_E, as shown in Figure 18.

Figure 17 | Common collector configuration circuit with series base resistor R_B and emitter resistor R_E

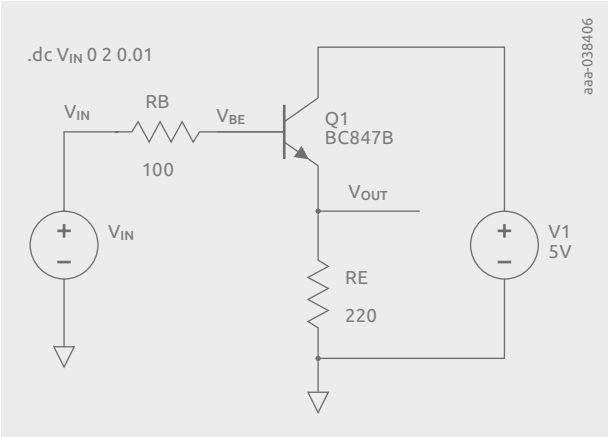


Figure 18 | Common collector configuration circuit Spice simulation

In Figure 19 the results of the simulation are shown for V_{IN} and V_{OUT}. V_{IN} and V_{BE} are almost identical. From about 0.6 V onward a collector current flows and V_{OUT} roughly follows the input voltage with an offset of V_{BE}. Because of this behavior the circuit is also referred to as emitter-follower. The operating point can be chosen across a wide range. It is limited by the supply voltage; the BJT does not saturate but stays in normal mode. The voltage amplification is very close to 1, with:

$$A \sim S \times \frac{R_E}{(1 + S \times R_E)} \sim 1$$

The current amplification is close to ß, so the same as for the common emitter base circuit approach from Figure 3.

The input resistance is quite high, and is roughly:

$$r_{IN} \sim ß \times R_E$$

It is assumed that no load is connected. With a load resistor applied, the equivalent resistor for R_E and RL put in parallel must be used in the formula.

The output resistance is $R_{OUT} \sim R_B/ß + 1/S$.

The thermal stability of the operating point $\Delta V_{OUT}/\Delta T$ is identical to the thermal behavior of V_{BE} of the BJT, so about 1.7 mV/K. As the emitter-follower has a wide linear range in the output characteristics, this thermal shift vs. temperature is not critical for most applications.

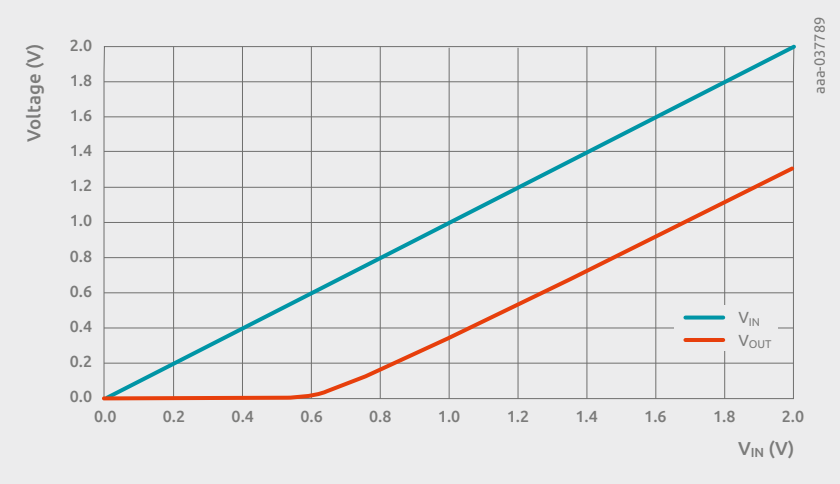


Figure 19 | Common collector Spice simulation traces for the circuit shown in Figure 18

The emitter-follower circuit can show problematic behavior if a capacitive load is connected. The circuit can start with high-frequency oscillations because the complex input impedance has a negative part. A series resistor to the base R_B in the range from 100 Ω to 300 Ω removes this issue in most cases.

7.1.3 Common base circuit examples

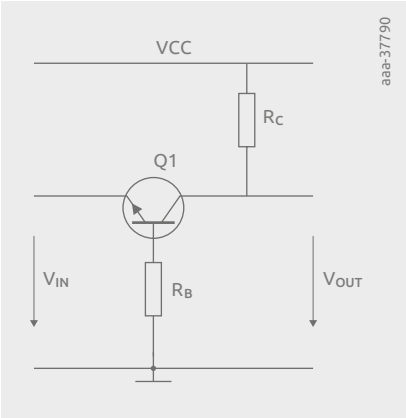


Figure 20 | Common base configuration circuit with base resistor R_B and collector resistor R_C

In Figure 20 a common base configuration circuit is shown. The base has a series resistor R_B connected to ground. This resistor is required in order to avoid excessive base currents if the circuit is not run in normal mode but with a high negative input voltage. A second resistor R_C is connected from the collector to the power supply line VCC. Figure 21 is a Spice example for this amplifier. For R_C the value 1 kΩ has been selected, and for R_B 220 Ω.

As long as V_{IN} is positive or more than about −0.6 V, there is no collector current and V_{OUT} is identical to VCC. If V_{IN} reduces, meaning V_{IN} is less than −0.6 V, there is a rather steep transition in the output voltage down to about −0.7 V. With additional drive at the input, the BJT is run in saturated mode and leaves normal mode. The collector base diode starts to conduct and there is a larger voltage drop across R_B. V_{IN} and V_{OUT} are almost identical in saturated mode.

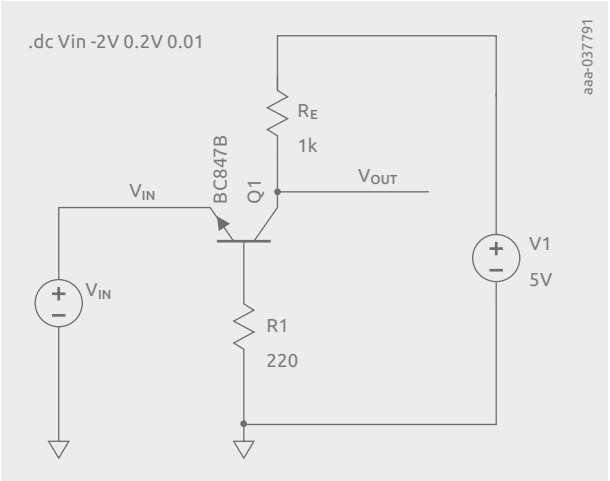


Figure 21 | Common base configuration Spice simulation circuit

These facts can be seen in the Spice simulation traces in Figure 22.

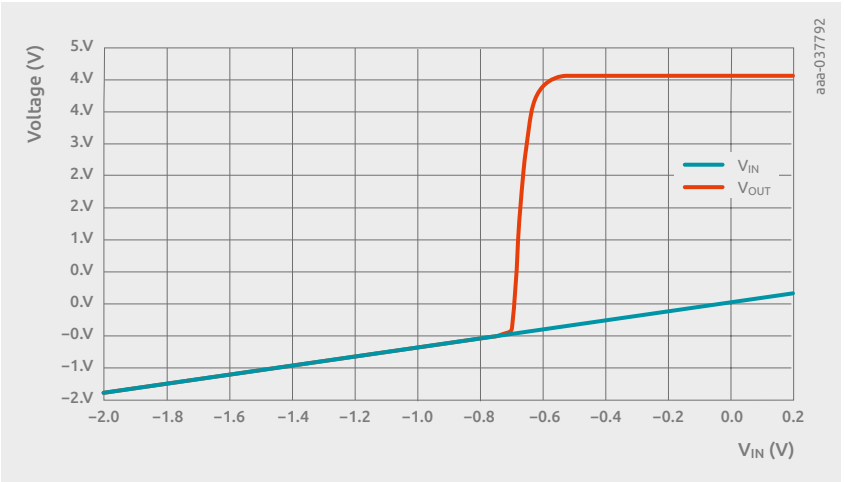


Figure 22 | Common base configuration Spice simulation circuit

The common base configuration without feedback shows some similarities for the key parameters. The reason is that the input voltage is applied between base and emitter for both topologies and the output signal is taken from the collector of the BJT, which has a resistor R_C connected to the supply voltage. The voltage amplification and the output resistance are the same. However, R_{IN} is significantly lower because the emitter current has to be provided by the input voltage stage and not just the base current. The key facts for the common base approach are:

$$A = S \times R_C \qquad R_{IN} \sim 1/S \qquad R_{OUT} \sim R_C$$

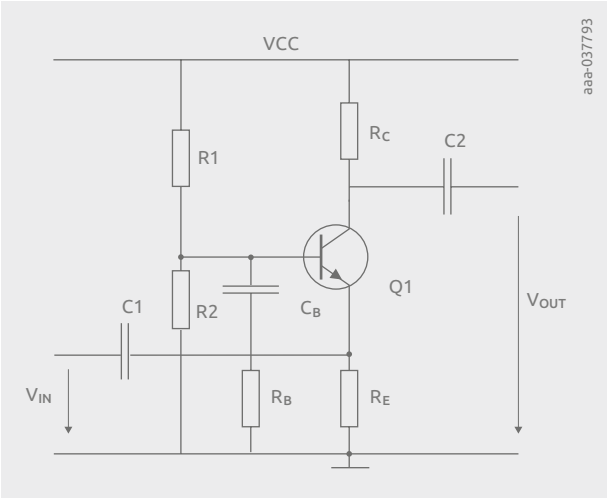


Figure 23 | AC-coupled common base configuration application example

Figure 23 shows an example where the amplifier is AC coupled at the input and output. The DC operating point is adjusted with a resistor base divider. Similar to the emitter circuit approach there is a voltage feedback supported by the resistor RE, which makes the operating point more stable in terms of thermal drift. The base circuitry has to be quite low ohmic for the common base configuration to avoid an undesired decrease of amplification. However, making the base divider very low ohmic has the disadvantage that the efficiency of the circuit also becomes low. The resulting resistor of R1 in parallel to R2 is equivalent to the base resistor R_B from Figure 20 and Figure 21. R_B in the discussion of the basic circuit did not have a significant impact on the amplification in normal mode due to the low I_B required. To solve the efficiency conflict with a low-ohmic base divider an additional high-pass R_C filter is placed from base to ground. The corner frequency of this high-pass filter has to be designed such that the lowest desired operating

frequency is not damped too much. A rather low-ohmic resistor R_B can be put into the R_C filter. R_B realizes the low impedance for the base circuitry for the AC range that the circuit is designed for. The current through the base divider only needs to be high compared to I_B, which is easy to realize.

In Figure 24 a Spice simulation example of the application discussed is shown. A sine wave input signal of 10 mVpp is amplified to about 1.6 Vpp at the output, so the circuit amplifies by a factor of about 160.

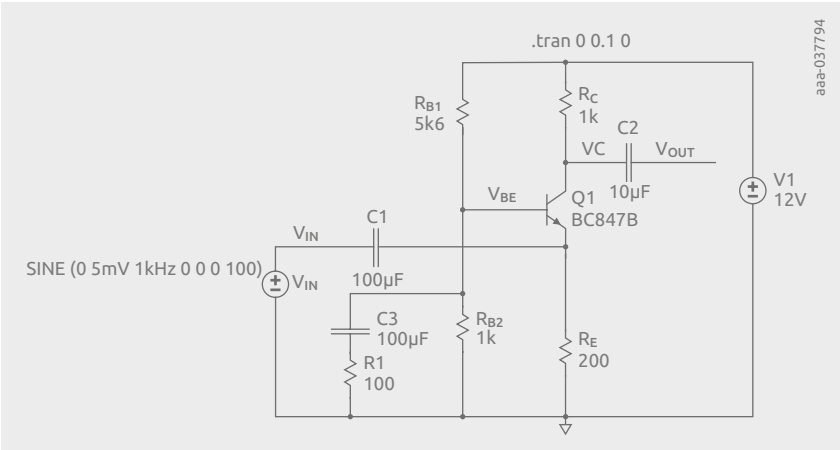


Figure 24 | AC-coupled common base configuration Spice simulation example

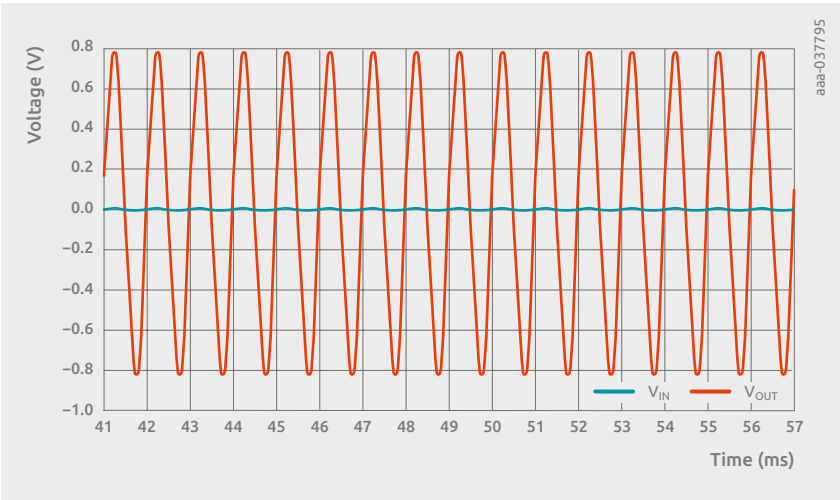


Figure 25 | AC-coupled common base configuration Spice simulation, input and output signal traces

7.2 Current mirrors

Current mirrors are an important application for bipolar junction transistors (BJTs). In Figure 1, a basic implementation of a current mirror is shown. A simple current mirror is realized with two transistors, where the two base contacts are connected to each other. If R1 and R2 do not exist, both transistors always have the same V_{BE} and thus should have almost the same collector current, assuming that the transistors are fully identical. The base of Q1 is connected to the collector of this BJT. A defined current I_{IN} is generated, driven by the supply voltage VCC over RV, which allows an adjustment of the current. The resistors R1 and R2 work for current feedback and make the circuit less dependent on the BJT characteristics. The circuit shown here works as a current source. As the name of the circuit indicates, I_{OUT} has an almost linear relation to I_{IN} if the BJTs do not operate in saturated mode. If R1 and R2 have the same value, the translation factor is 1.

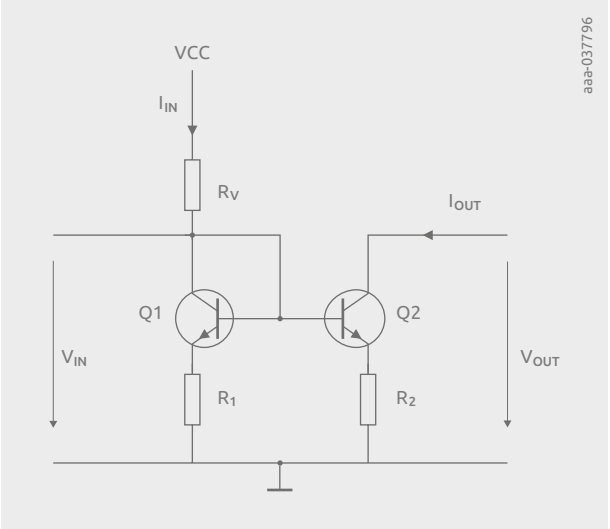


Figure 1 | Simple current mirror realized with two NPN BJTs

For the circuit in Figure 1, the mesh equation below can be noted down:

$$(I_C1 + I_B1) \times R1 + V_{BE}1 = (I_C2 + I_B2) \times R2 + V_{BE}2$$

If R1 and R2 are not applied (R1 = R2 = 0 Ω), the formula becomes very simple and states that:

$$V_{BE}1 = V_{BE}2$$

With the basic BJT equations the current factor I_{OUT}/I_{IN} can be calculated.

1: $I_C = I_B \times B$
2: $I_C = I_S \times e^{V_{BE}/V_T} \times (1 + V_{CE}/V_A)$
I_S = reverse saturation current of the base emitter diode (~ 10^{-15} A to 10^{-12} A)
V_T = thermal voltage (KT/q, approximately 26 mV at room temperature)
V_A = early voltage (~10 V to 150 V, lower for small devices)

For the transistor Q1 $V_{BE}1$ is equal to $V_{CE}1$. Therefore, the term V_{CE}/V_A can be ignored in the second formula.

With Kirchhoff's circuit law applied, it can further be stated:

$$I_{IN} = I_C1 + I_B1 + I_B2$$
$$I_{OUT} = I_C2$$

Using these formulas, the current factor k1 becomes:

$$k1 = \frac{I_{OUT}}{I_{IN}} \sim \frac{I_S2}{I_S1}$$

If the transistors are identical, the factor k1 is 1. Nexperia offers matched pair transistors. The parameters h_{FE} and V_{BE} are closely matched for these products. The matched pair BJTs are produced with dies that are picked from the same wafer from an adjacent position where it is very likely that the device physics are almost identical.

With the introduction of current feedback resistors R1 and R2, the current mirror circuit does not depend on the transistor characteristics anymore and the spread of BJTs is less problematic. In Figure 2 a Spice simulation example is shown, where R1 and R2 are equal and realized with 100 Ω resistors. The collector of Q2 is connected to 5 V. The resulting currents are shown in Figure 3. The input and output currents are almost equal.

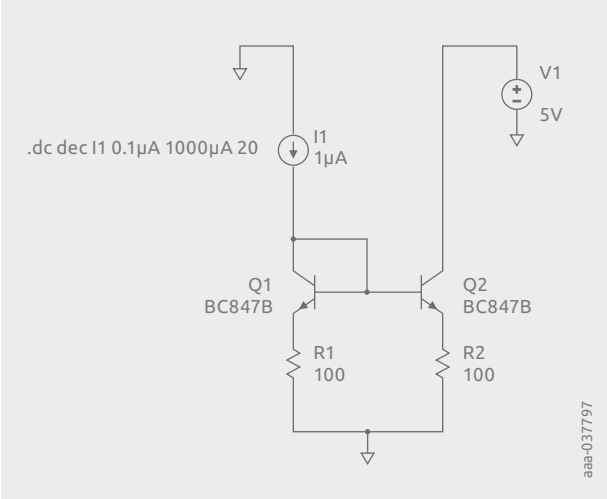


Figure 2 | Spice simulation example for a current mirror, ratio R1/R2 = 1

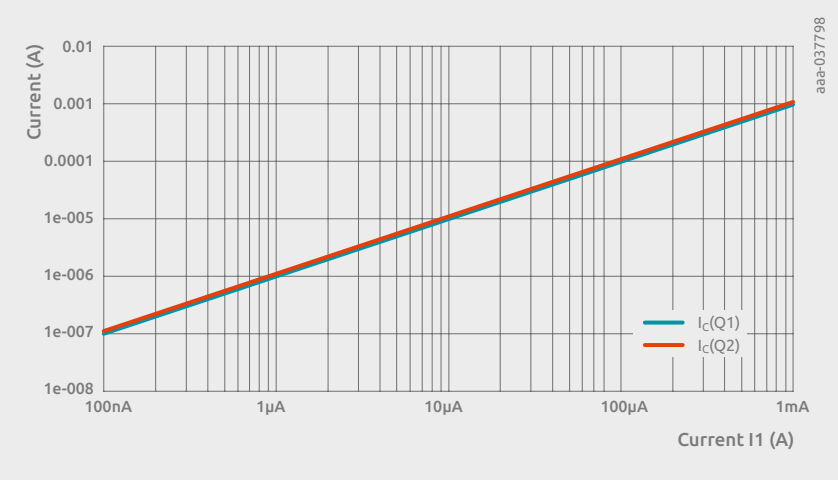


Figure 3 | Spice simulation results for the current mirror shown in Figure 2 showing the colector currents of the BJTs Q1 and Q2 versus the input current I1.

If the ratio R1/R2 is modified to a factor of 2 as shown in Figure 4, the current ratio is not constant but achieves this value for higher current, as shown in Figure 5.

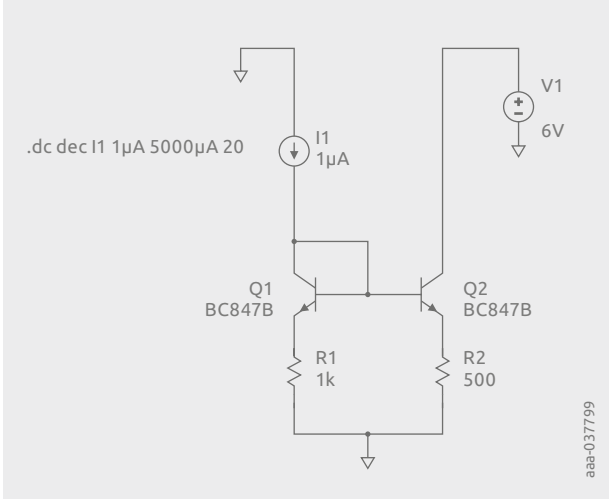


Figure 4 | Spice circuit of a current mirror with an R1/R2 ratio of 2

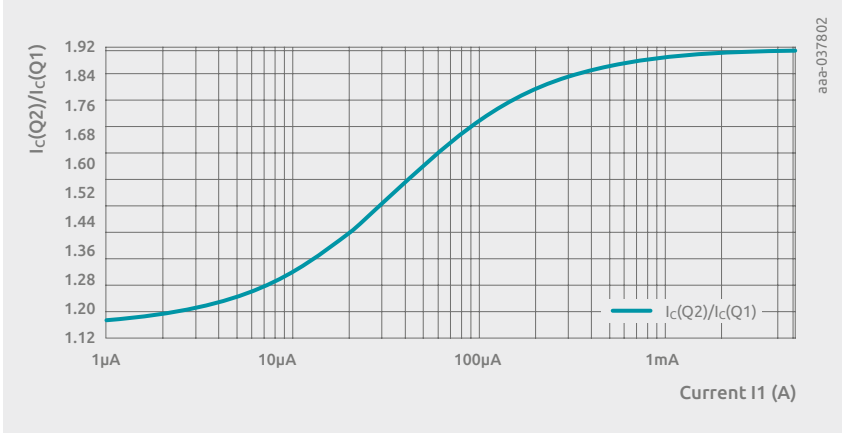


Figure 5 | Spice simulation results for the current mirror shown in Figure 4 showing the ratio $I_C(Q2/I_C(Q1)$ versus the input current I1.

A very effective method to increase the output resistance of a current source realized is to cascade two current mirrors, as shown in Figure 4. The circuit was simulated with an output resistor of 10 kΩ connected to a supply voltage of 12 V. Figure 5 shows that the output current follows the input current exactly. The current curves of Q3 and Q4 overlay each other, so the ratio of I_{C3} and I_{C4}, included as a blue trace, is a line parallel to the x-axis at the value 0.993, so almost 1.

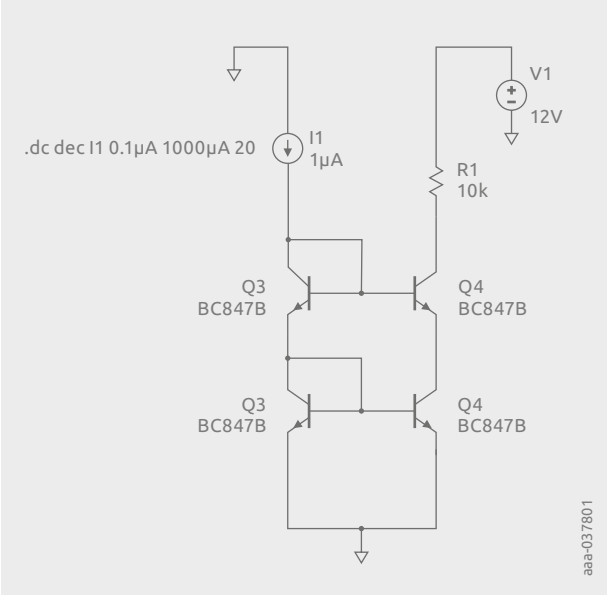


Figure 6 | Spice simulation example for a cascode current mirror

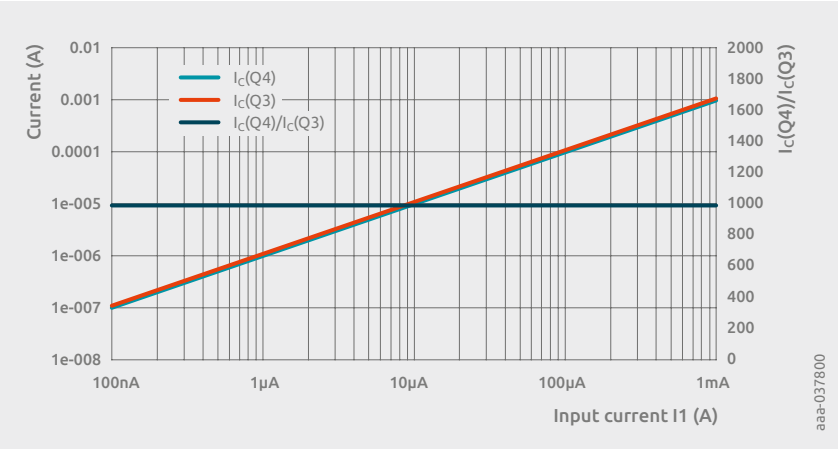


Figure 7 | Results of a Spice simulation for the cascode current mirror shown in Figure 3

7.3 Differential amplifiers

A differential amplifier has two inputs and outputs with a symmetrical design, as shown in Figure 1. The basic realization with bipolar junction transistors (BJTs) requires two transistors with connected emitters. A current source is connected to the emitter node, and the output voltages are present at the collectors of the amplifier stage. If the input voltage at the base of Q1 is increased, the collector current increases as well, and the collector current of Q2 decreases. The voltage drop at R_{C2} becomes smaller and the output voltage V_{OUT+} increases. Therefore, the input connected to Q1 is called V_{IN+}, and as the the collector signal at Q2 reacts with the same phase, it is called V_{OUT+}. Due to the symmetrical behavior the input connected to the base of Q2 is in phase with the collector signal at Q1. So, these input and output signals are referred to with a negative assignment in the names. In Figure 1 it is assumed that the circuit is supplied with a positive voltage VCC and a negative supply –VCC connected to the bottom node of the current source.

The current source provides the current $2 \times I_{E0}$. This name is chosen because the emitter current in both BJTs is identical if they both get the same input voltage. The following equation for the currents at the emitter node can be noted down:

$$2 \times I_{E0} = I_{E1} + I_{E2} = I_{C1} + I_{B1} + I_{C2} + I_{B1}$$

if the base currents are ignored because of $I_C \gg I_B$, the formula becomes:

$$2 \times I_{E0} \sim I_{C1} + I_{C2}$$

The operating point of the outputs is adjusted very easily with the selection of the collector resistors.

$$V_{OUT} \sim VCC - I_{EO} \times R_C$$

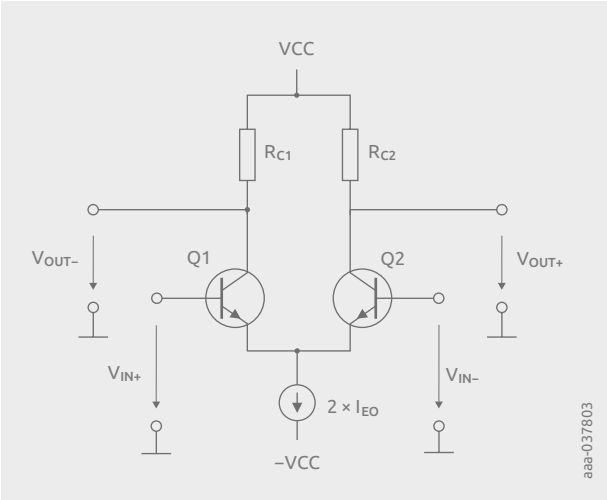


Figure 1 | Differential amplifier realized with NPN-BJTs

For further investigation of the circuit from Figure 1 we apply 10 kΩ as collector resistors RC1 and RC2 for a simulation, and a current value for the current source of 1 mA is chosen. Then we get 0.5 mA as emitter current for each of the BJTs. With a voltage supply VCC = 10 V, the collector or output voltages should show 5 V as idle condition if the impact of the base current is ignored. The related Spice circuit is shown in Figure 2. As a first experiment the two inputs of the amplifier are connected, and how the output voltages react on a common-mode input signal is checked. The two inputs get a voltage ramping up from −5 V to 5 V. The Spice simulation result shows the expected behavior that the output voltages stay at about 5 V of idle mode, meaning the condition where no input voltage is applied. This rather perfect behavior can be seen because of the ideal current source applied in the simulation. Ignoring the impact of the base currents, the collector current stays at I_{E0} independent of the common-mode input voltage. The voltage at the emitters changes, of course, so the stable behavior for V_{OUT} can be seen for a suitable voltage range only. If V_{COM} is made too high, the BJTs reach saturated mode and V_{OUT} would increase from about V_{COM} = 5.7 V onward in the given example.

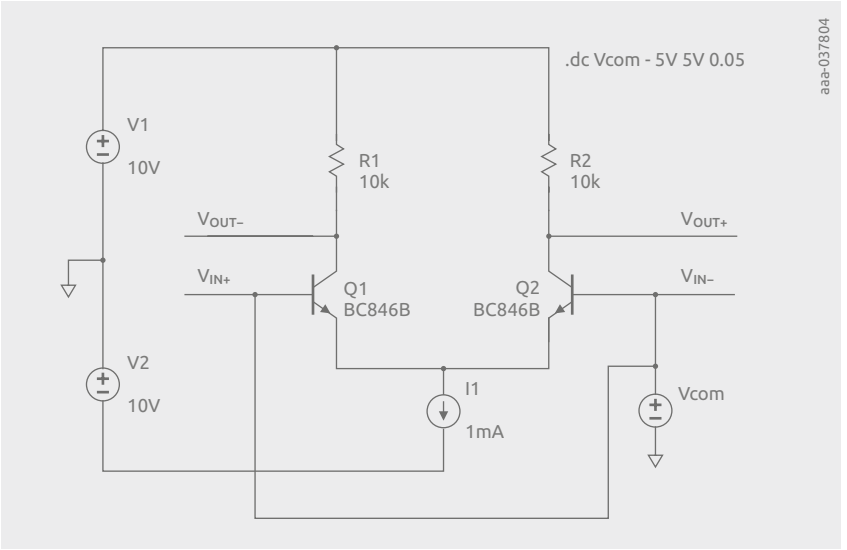


Figure 2 | Spice simulation circuit for a differential amplifier with a common-mode input voltage V_{COM}

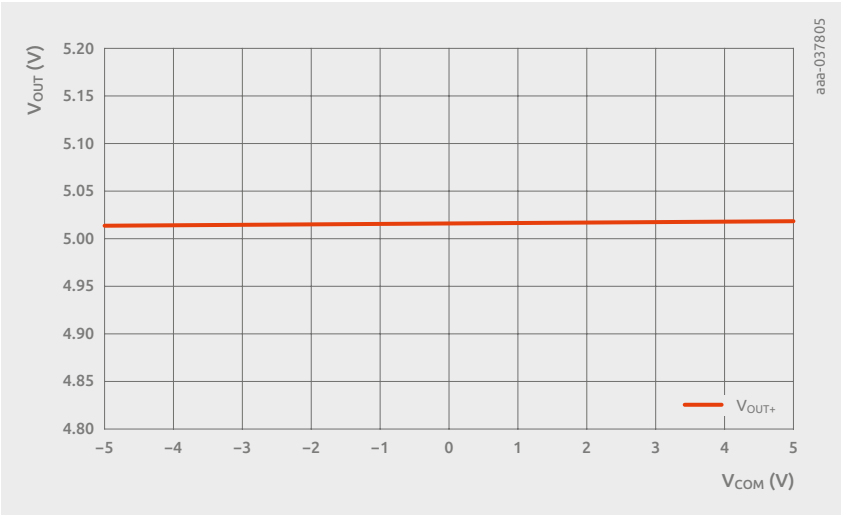


Figure 3 | Spice simulation result for a common-mode input signal ranging from −5 V to +5 V. V_{OUT} vs. V_{COM} is almost constant

As a next check the differential amplifier gets a symmetrical differential input voltage, as shown in Figure 4. The V_{IN+} signal ramps from −0.1 V to 0.1 V in a second, and the other input V_{IN-} gets the inverted voltage, so a signal falling from 0.1 V to −0.1 V.

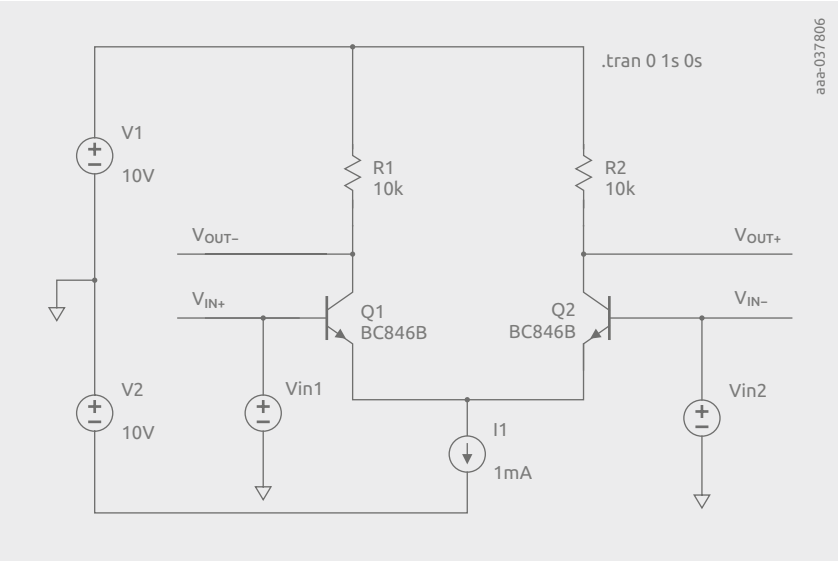


Figure 4 | Spice simulation circuit for a symmetrical differential amplifier. V_{OUT} vs. a symmetrical input voltage V_{DIFF} ranging from −0.2 V to +0.2 V is simulated

In Figure 5 the two input voltages are shown. The difference between the two traces is the differential voltage:

$$V_{DIFF} = V_{IN+} - V_{IN-}$$

In Figure 6 the two output voltages are shown. At the point without a differential input voltage the output voltages are 5 V. The positive output ramps up from about 0 V to 10 V, while the negative output curve shows inverted behavior and ramps down from 10 V to 0 V. There is a linear region in the middle of the transfer curves where the circuit works linearly and with a constant amplification factor.

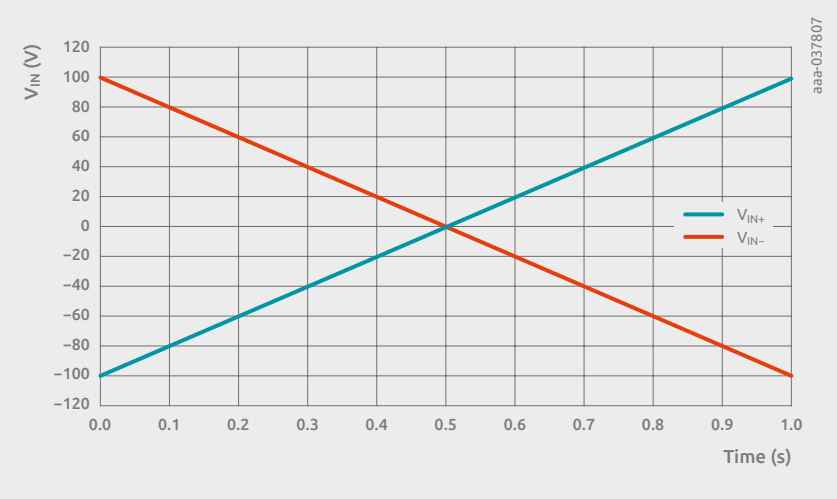


Figure 5 | Symmetrical input voltages for the Spice simulation in Figure 4

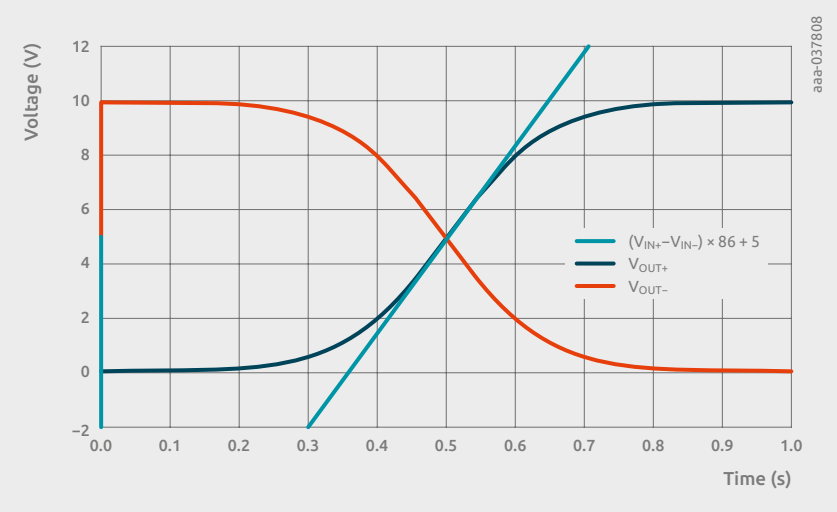


Figure 6 | Output voltages and a tangent added to the positive output as light-blue trace for the Spice simulation in Figure 4.

The amplification for an output of the simulated example is:

$$A_{OUT} \sim \frac{\Delta V_{OUT}}{\Delta V_{DIFF}}$$

From the tangent added as a light-blue line, an amplification factor of about 86 can be derived.

For many applications differential amplifiers are used with one active input only. The other input is tied to GND for a dual-supply design or any fixed voltage. In Figure 7 such a scenario is shown. Additionally, as a further simplification, the negative output has been removed and Q1 is connected to VCC directly without a collector resistor.

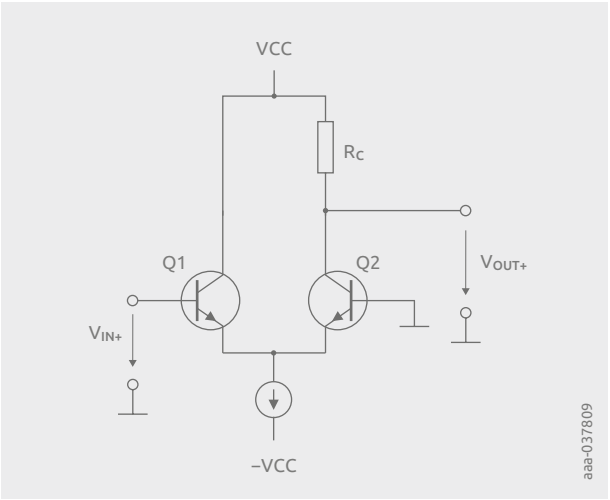


Figure 7 | Differential amplifier with one input and output as an asymmetrical approach

Figure 8 shows an example circuit in Spice for this scenario. An input signal from –0.1 V to +0.1 V is applied. In Figure 9, the simulation result is shown with the output voltage as a red trace and a reference line as a tangent shown in blue, symmetrically to the operating point at V_{IN} = 0 V. From the tangent an amplification factor of about 86 can be derived.

Differential amplifiers have the general advantage that the operating point does not change significantly over temperature. As shown, the common-mode amplification is extremely small. If the two BJTs are thermally closely coupled, the impact of temperature change is like applying a slow-changing common-mode input voltage. Besides the thermal stability it is of course also a big advantage that the operating point does not change if a common-mode voltage is applied to the inputs; if the variation stays in a moderate range. This makes differential amplifiers ideal for DC-coupled applications.

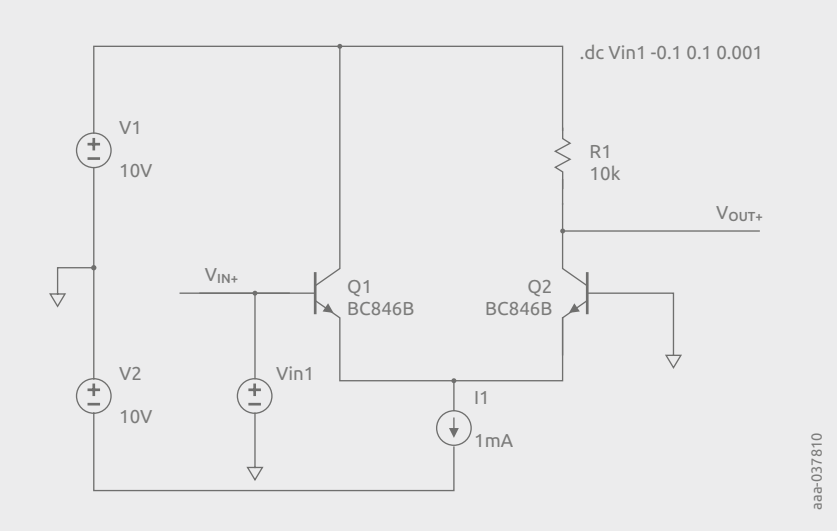


Figure 8 | Spice simulation of an asymmetrical differential amplifier with one input and output

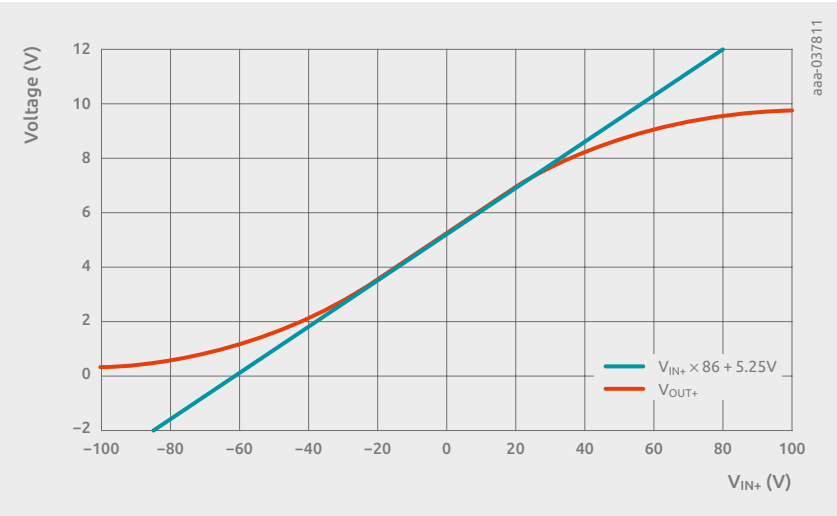


Figure 9 | Asymmetrical differential amplifier, V_{OUT} vs. V_{IN}

For differential amplifiers it is recommended to use dual BJTs; this means two BJTs that are assembled in one package. The temperature of the dies will be almost identical with the adjacent location of the two transistors. Selecting a matched pair of transistors guarantees that the electrical parameters of a transistor pair are almost identical too. This safeguards fully symmetrical behavior of the differential amplifiers.

A further advantage of differential amplifiers is the high bandwidth. The reason for this is the fact that a differential amplifier can be seen as a series combination of a common collector configuration stage (emitter-follower) and a common base configuration stage behind it. A differential amplifier designed like the example in Figure 8 does not suffer from the Miller effect, as is the case for amplifiers realized in a common emitter configuration.

The amplification in the area close to a differential input voltage of 0 V can be roughly calculated, ignoring the impact of base currents with the formula:

$$A_{DIFF} = \frac{\Delta V_{OUT+}}{\Delta V_{DIFF}} = -I_{E0} \times \frac{R_C}{2 \times V_T}$$

For the simulation examples: I_{E0} = 0.5 mA, R_C = 10 kΩ

The thermal voltage VT is about 26 mV. Then the formula delivers A_{DIFF} = 5 V/52 mV ~ 96.

The simulation results show an amplification factor which is a little smaller because of the assumption in the formula that base currents can be ignored. In practice this deviation can be compensated for with a slightly higher value for R_C.

Below, a more complex application example is shown in Figure 10, where the current source for a differential amplifier is realized with an NPN current mirror and where the collector resistors are replaced by another current mirror realized with two PNP transistors. The emitter currents for the differential amplifier BJTs Q1 and Q2 are provided by the current source built by Q7 and Q8. The resistors R5 and R1 define the control current for this current mirror. R5 was added to tune the current source to 500 µA almost exactly using E12 series resistor values. The input on the right side of the differential amplifier is connected to a fixed bias voltage realized with a simple resistor divider. The base of Q2 is connected to about 1 V with the divider. In the circuit example a single supply voltage of 10 V is shown, not a symmetrical supply.

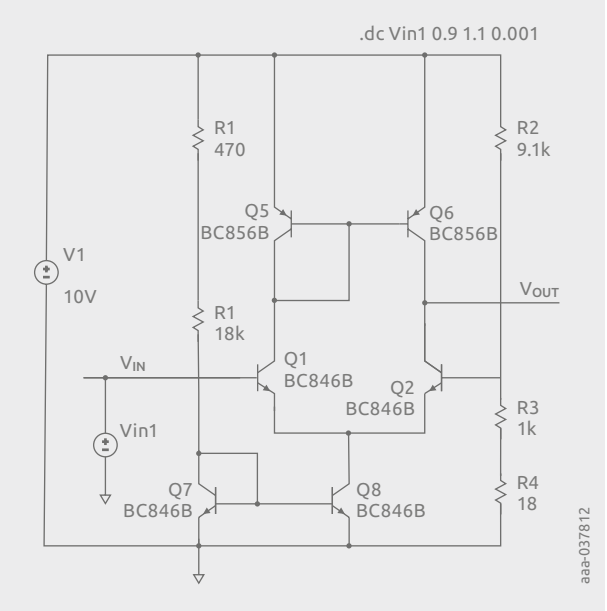


Figure 10 | Spice simulation of an asymmetrical differential amplifier realized with two additional current mirrors – one used as current source for the emitters of Q1 and Q2 and a second one replacing the collector resistors

The curve for V_{OUT} is shown in Figure 11. The differential amplification is about 800, as the tangent drawn in red shows.

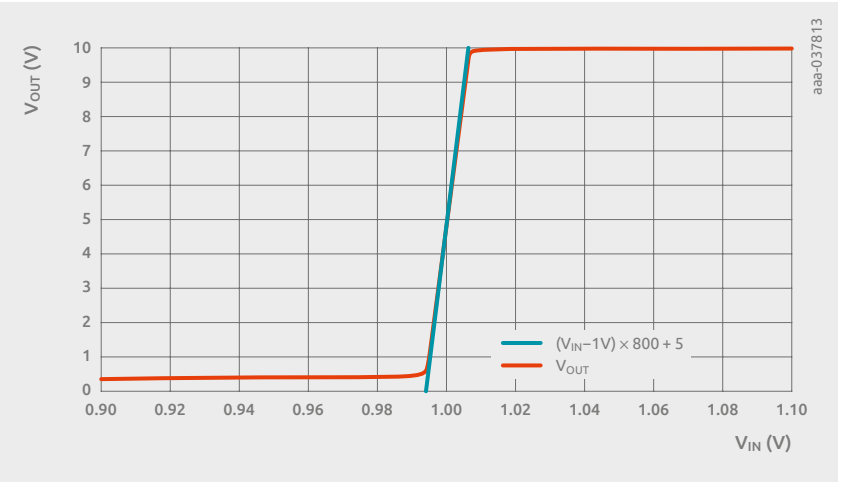


Figure 11 | Spice simulation traces for V_{OUT} vs. V_{IN} for the circuit shown in Figure10 – the light-blue line is a tangent added, centered on the steep rising area of the V_{OUT} curve

The amplification can be reduced by adding current feedback in the emitter path of the BJTs of a differential amplifier. An example of this approach is simulated for the circuit shown in Figure 12. The resistors R3 and R4 are added into the corresponding emitter path of Q1 and Q2. The input signals are ramping from −0.4 V to +0.4 V for V_{IN+} and from +0.4 V down to −0.4 V for V_{IN-}. The output curve shown in Figure 13 shows a significantly reduced steepness, so a reduction of the amplification. The linear part of the input voltages is extended significantly.

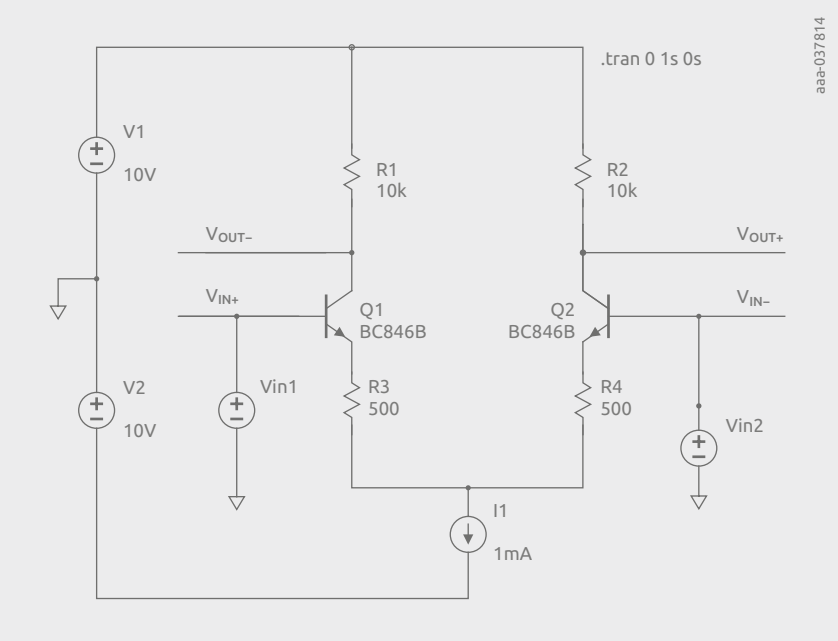


Figure 12 | Spice simulation circuit of a differential amplifier with current feedback resistors R3 and R4

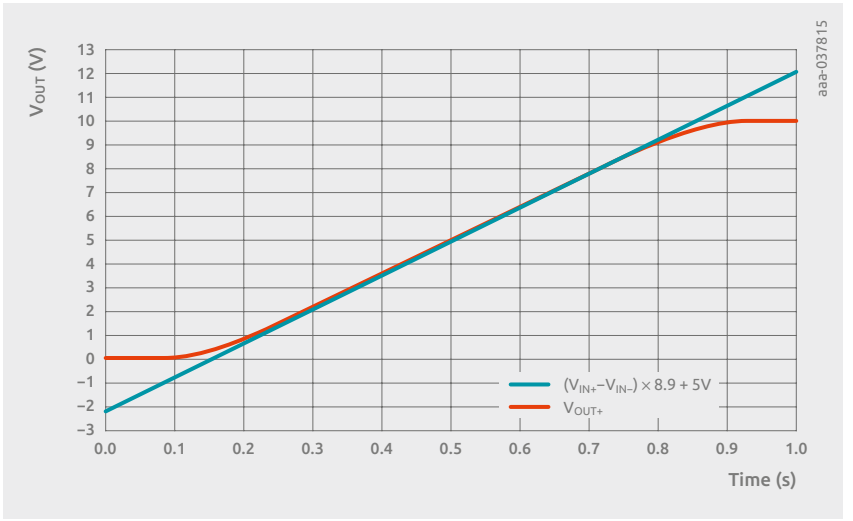


Figure 13 | Spice simulation results – V_{OUT} (blue trace) and a tangent added (green trace)

7.4 Comparators

Comparators are almost identical to differential amplifiers. They have two inputs – a positive and a negative input. The output delivers a digital signal, meaning a low or a high state. The output state is high if the voltage at the positive input is higher than the voltage at the negative input. The low state is obtained if the voltage at the positive input is smaller than at the negative input. For this requirement the transfer curve needs to be steep. It is not desirable to have a wide area where the comparator shows a linear behavior. Therefore, differential amplifiers with a high amplification are suitable as comparators. This means that most of the application examples discussed in Chapter 7.3 can be considered as discrete solutions for a comparator.

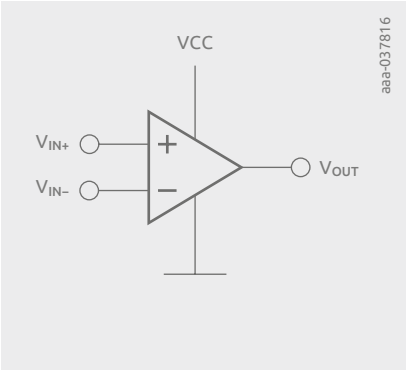


Figure 1 | Simple comparator circuit

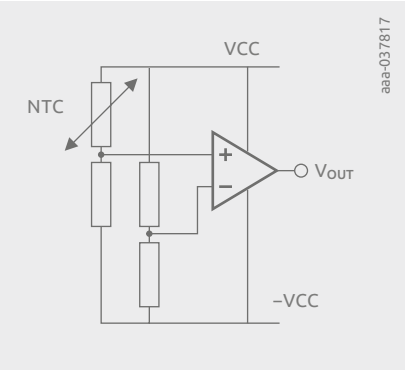


Figure 2 | Thermal switch with NTC sensor and a comparator

Figure 1 shows a simple block symbol for a comparator. Comparators can be used with a single supply as well as with a positive and negative power supply. If the output is called V_{OUT} without a positive or negative indication, a positive output direction is meant. The output switches to high state if V_{IN+} is bigger than V_{IN-}. Integrated differential amplifiers and comparators provide the positive output as a pin connection only normally. In a discrete realization which is in the focus of this handbook, both polarities are present and can be used in an application.

Comparators can be found in many control circuits where an analog sensor delivers a signal. This can be a negative thermal coefficient (NTC) or a positive thermal coefficient (PTC) resistor. One input of the comparator is coupled to a reference voltage with a resistor divider, and the other input is connected to a divider in which a thermal sensor is used. If a potentiometer is added into the reference voltage divider the target temperature can be adjusted to a desired target value. Figure 2 shows an example. As the temperature rises, the resistance of the NTC decreases, so voltage at the positive input increases. Once the voltage at the positive input is higher than the voltage at the negative input, the comparator output voltage switches to logic low level; for example, a heater could be turned off because the target temperature is reached.

For a comparator in practical use, it is recommended to plan for a hysteresis of the switching characteristic if the incoming signal has very smooth rise and fall times, or if it is a kind of DC signal. For thermal signals this is very likely to be the case. Without a hysteresis the comparator will start to oscillate; this means an undesired switching of the output signal if the input voltage is close to the reference voltage of the comparator.

In Figure 3 a discrete bipolar junction transistor (BJT) circuit for a comparator based on a differential amplifier is shown. For the BJT Q2 a fixed base voltage is applied. This means that the negative input of the comparator is connected to a fixed reference voltage. Q1 is connected via 47 kΩ to an input signal, which rises from 0 V to 5 V within a second, then stays at 5 V for 0.1 s and then falls back to 0 V again. A feedback loop from the positive output to the positive input of the comparator is realized via the resistor R5. With an input voltage of 0 V, applied to V_{IN} which is the positive input of the comparator, Q1 is turned off, which means that V_{OUT-} is almost the supply voltage. Q2 conducts because the base voltage from the reference voltage divider built by R2, R3 and R8 provides about 2 V. If the input signal voltage increases, a small current flows from the base node of Q1 to the collector of Q2. This reduces the base drive of Q1, and the BJT switches slightly later in the ramping of the input signal, so at a higher voltage. Once Q1 turns on, Q2 turns off and the feedback loop speeds up the transition, because the collector voltage of Q2, which is the positive output, jumps up to almost the voltage level of V1. The positive direction feedback loop enhances the switching time of the comparator and makes the analog operation area extremely narrow. If the input signal changes in the other direction from 5 V to 0 V, the return to the start condition requires a slightly lower V_{IN}. As a result of the positive feedback loop the comparator has a hysteresis in the switching characteristic.

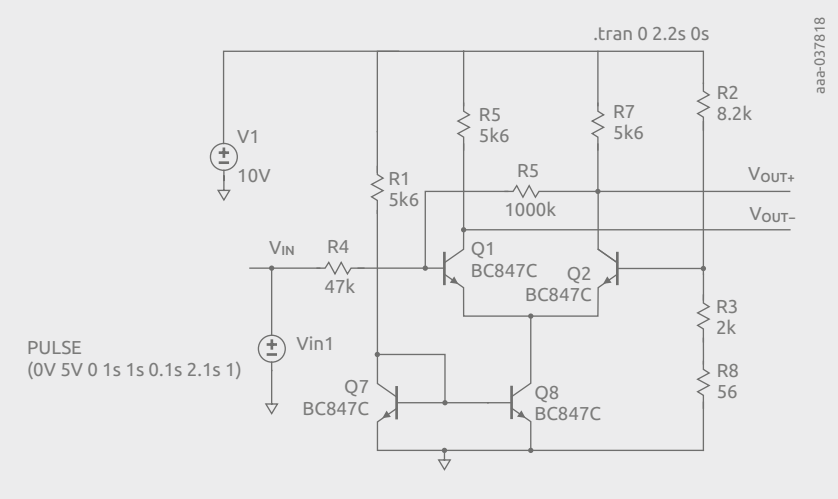


Figure 3 | Example comparator Spice simulation circuit with positive feedback loop

In Figure 4 the simulation results are shown. The red trace is the input signal as described above. The two output signals switch with short transition times. The overlaid cursor window shows the input voltages of the two switching events. At about 1.99 V the positive output changes to a high state, but it switches back to a low state at 1.87 V. So, there is a hysteresis of about 100 mV, which makes the circuit more immune to residual noise in the input signal.

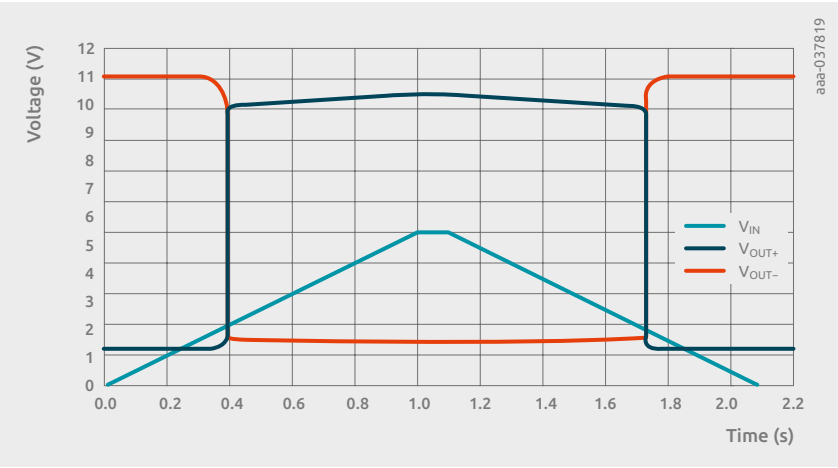


Figure 4 | Spice simulation result for the circuit shown in Figure 3

7.5 Current sensing

In this chapter a suitable application example for current mirrors is discussed. Often a current needs to be sensed at the high side of a load. A current value should be measured with a voltage which is suitable for a microcontroller ADC input, so a rather small voltage relative to GND. Such a requirement could be seen in an electrical vehicle or a mild hybrid car.

In Figure 1 a battery voltage of 48 V is applied as supply. A load is connected via a 50 mΩ current sensing resistor. In the simulation a current source realizes the load. The output current is simulated from 0 A up to 10 A. Maximum current sensing voltage is then 0.5 V.

The sensing circuit uses two current mirrors – a PNP mirror in the upper part and an NPN mirror working on the GND side. The output voltage is derived from the emitter resistor R3 in the NPN current mirror.

The sensing resistor R1 generates the input voltage to the circuit, which is provided as very low ohmic. With increasing current the emitter voltage of Q2 becomes more negative against the 48 V supply. The emitter of Q1, which is the counterpart in the PNP current mirror, shows almost the same voltage. The collector current through Q1 is the input current for Q3 of the NPN current mirror.

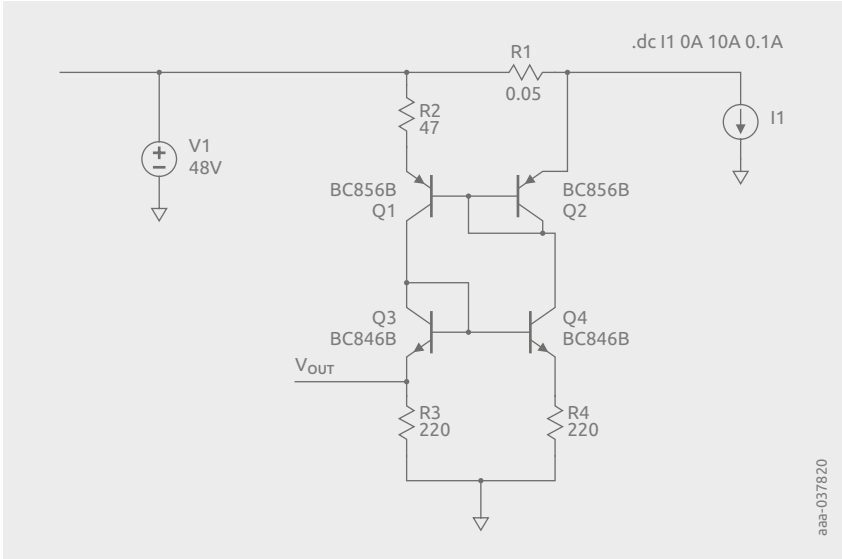


Figure 1 | Current sensing in the high-side path with two current mirrors

In Figure 2 the output voltage V_{OUT} is shown vs. the load current I1. The voltage trace is an almost ideal linear curve. The range of V_{OUT} is 0.1 V to 2.44 V for the simulated example, which is suitable for the ADC input of a microcontroller. The range can be tweaked easily with the value of R2.

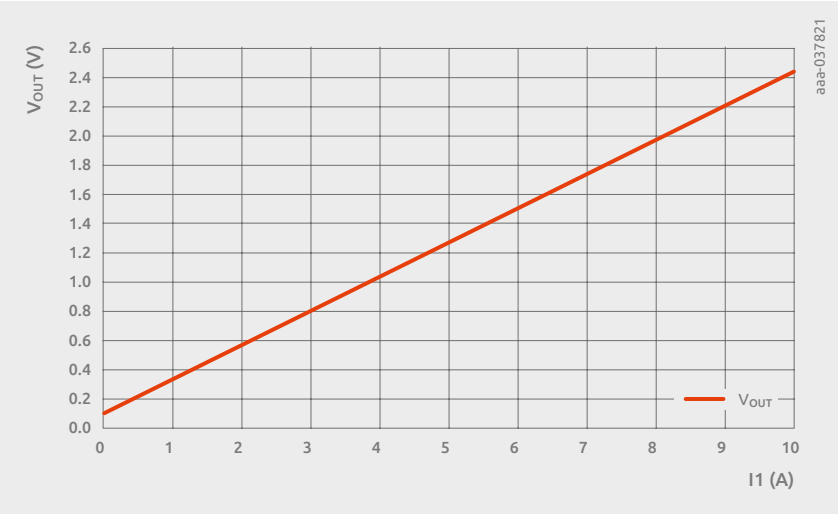


Figure 2 | Output voltage vs. load current I1

7.6 Voltage regulation

Linear regulators are widely used in application fields where noise- and ripple-free constant power supply is required regardless of changing input and output conditions. This particularly includes generating stable input voltage supply for application-specific chips (ASICs), microcontrollers, integrated circuits (ICs), application processors, sensors and many more. This is also the reason why linear regulators are used after switched-mode power supplies (SMPS) and therefore can be found in almost every power supply block.

There are a variety of linear regulator solutions available in the market, including both integrated and discrete solutions with their own advantages and disadvantages. A very well-established and straightforward solution is a linear regulator where a bipolar junction transistor (BJT) is used as a pass element. In this solution, contrary to SMPS, the difference between input and output power is directly dissipated in the pass device. This is also the reason why linear regulators are used when the difference between input and output voltage is rather small, or only small output current needs to be provided. This way power dissipation in the pass element is kept to a minimum. As already mentioned, the major advantage of a linear regulator with external pass element is the easy setup. Figure 1 shows the basic setup of a linear regulator with feedback regulation. The pass device in this case is an NPN-BJT, which is driven by a PNP transistor. The pass device could also be a PNP-BJT, or for very high currents even a Darlington transistor. The minimum voltage drop across the BJT output stage for the example in Figure 1 is equal to the sum of the emitter-collector saturation voltage of the PNP transistor and the voltage drop of the base-emitter junction of the NPN ($V_{DROP}(min) = V_{CE,sat} + V_{BE}$). The output voltage is regulated by an error amplifier which gets the feedback voltage via a resistor divider from the output.

This feedback is compared to a set reference voltage and the base drive of the driving PNP-BJT is adjusted accordingly, which then adjusts the drive of the pass transistor. So, if the feedback voltage is above the reference voltage the error amplifier reduces the base current, and vice versa.

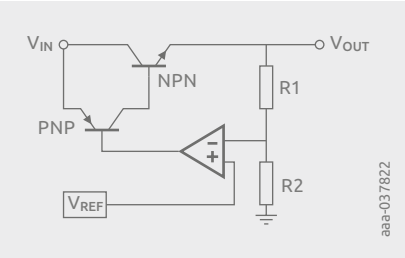


Figure 1 | Example of linear regulator

Within the linear regulator there is a subgroup known as low-dropout regulators (LDOs). While standard linear regulators require headroom between their input and output voltage of $V_{CEsat} + V_{BE}$, which is around 1.2 V, or for a Darlington transistor this would even be higher (~2 V), LDOs require headroom of their V_{CEsat} only – hence the name LDO. Figure 2 shows an example of (a) a LDO using a NPN and (b) a LDO using a PNP. These types of linear regulators are optimal for battery-powered applications because they are highly efficient through the low dropout. Using a high forward gain transistor will further increase the efficiency, because lower driving currents can be used.

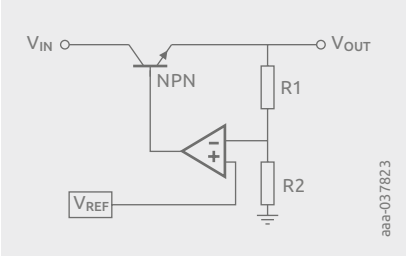


Figure 2 (a) | LDO using NPN-BJT

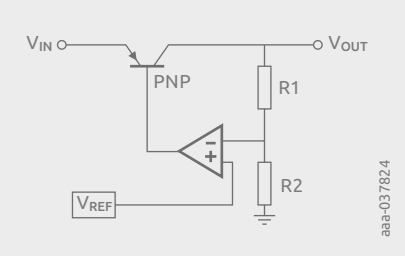


Figure 2 (b) | LDO using PNP-BJT

The choice of whether a NPN or a PNP should be incorporated depends on the requirements of the LDO. In general, NPN-BJTs have a better V_{CEsat} and forward current gain β compared to their PNP counterparts. On the other hand, if a PNP transistor is used it comes with a built-in reverse polarity protection, which the NPN solution does not have. So, in the case of a reverse voltage the NPN transistor would conduct to the input without any current limitations. If a reverse polarity is required a low forward voltage drop (V_F) Schottky needs to be placed in series with the LDO, adding voltage drop to $V_{OUT(min)} = V_{CE,sat} + V_F$.

There is a range of integrated solution for linear regalutaions but also a wide range of linear regulator ICs which only require some input and output capacitors and a pass element, but complete discrete solutions are still very popular in the industry. Below, two straightforward discrete regulator circuits are highlighted and discussed.

For loose linear regulation and output currents in the double-digit mA regime a Zener diode with the right Zener voltage V_Z (larger or equal to the desired output voltage and the maximum base emitter voltage) can be used. In this case there is no feedback loop. To showcase this, the Spice circuit shown in Figure 3, a 5 V linear regulator, can be considered. The nominal input voltage for this linear regulator is assumed to be 12 V. Figure 4 shows the corresponding voltage, current and instantaneous power waveforms.

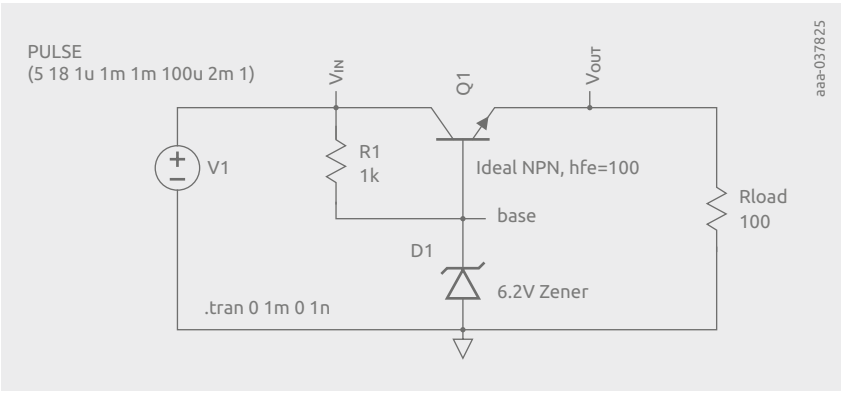


Figure 3 | Linear regulator with Zener diode

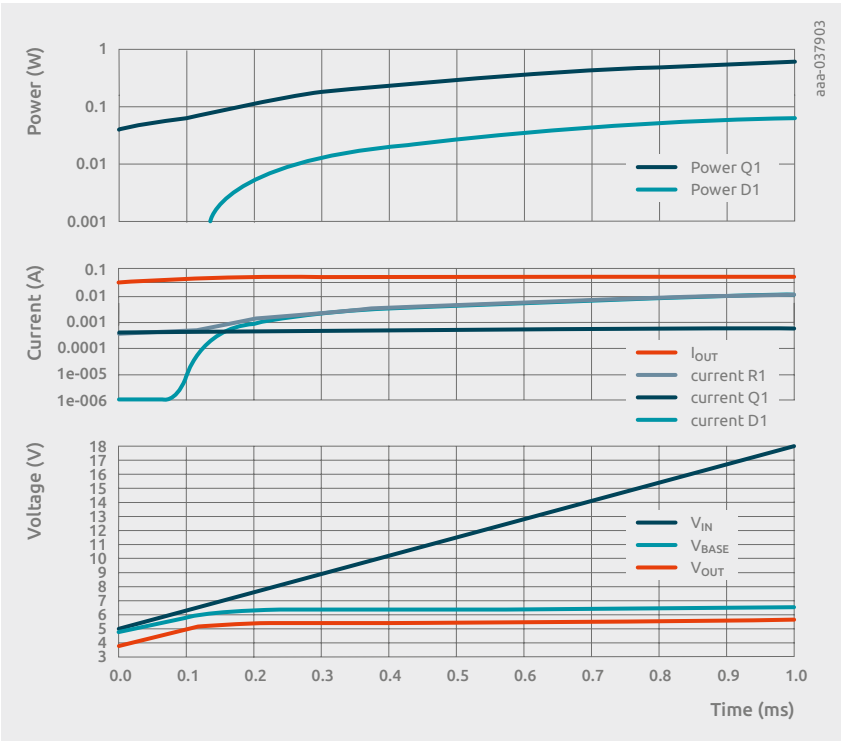


Figure 4 | Voltage, current and instantaneous power waveforms: 5 V/50 mA linear regulator with an input voltage ramp from 5 to 18 V

In the simulation a 6.2 V Zener diode is chosen to achieve an output voltage of around 5 V. The NPN-BJT in the simulation has a forward gain of 100. The output voltage can be calculated by $V_{OUT} = V_Z - V_{BE}$. R1 should be selected so that enough current can be supplied to the Zener diode (more than 0.5 mA). The current $I_{R1} = (V_{IN} - V_Z)/R1$. The base current can be then calculated by $I_B = I_{R1} - I_Z$. To demonstrate the response to input voltage changes V_{IN} is ramped up from 5 to 18 V. As soon as the voltage passes V_Z and the current through D1 is high enough the output voltage is held constant at the targeted (+10%) value regardless of the difference between input and nominal input voltage. The major part which contributes to power dissipation inside the BJT is the difference between input and output voltage.

A more precise and very well-established control method is to regulate and drive the pass element with a shunt regulator, such as the well-known TL431 or TLVH431.

Depending on the reference voltage V_{ref} of the chosen shunt regulator (V_{ref} of TL431 = 2.49 V and V_{ref} of TLVH431 = 1.24 V) the output can be set as low as the sum of $V_{OUT(min)} = V_{ref}$. As an example, the given 1.8 to 1.45 V LDO can be considered. The schematic is depicted in Figure 5 and a 3D visualization is shown in Figure 6. Since the input voltage is smaller than $V_{OUT(min)}$ a separate base drive needs to be provided. The output voltage is set by the equation $V_{OUT} = (1 + R1/R2) \times V_{ref}$. R1 and R2 should be realized as quite high ohmic to avoid unnecessary high ground currents. The resistor in the base path should also be chosen to provide minimum cathode current for the TLVH431, which is 1 mA and still provides enough base current on top. The maximum output for current for the LDO is 3 A.

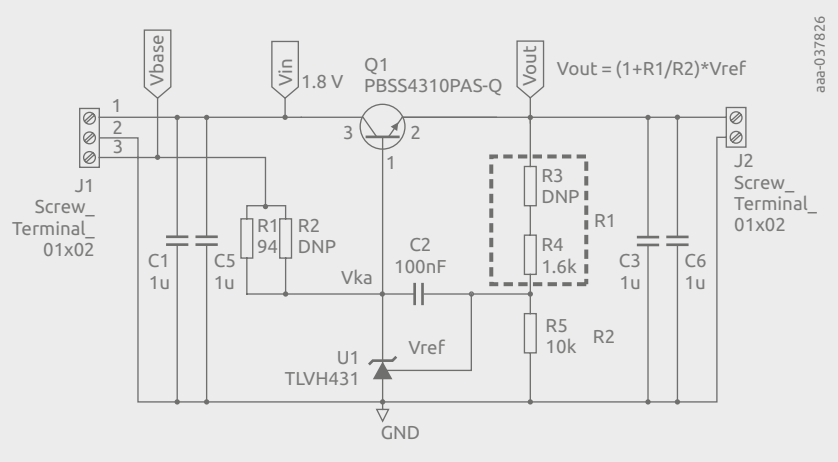


Figure 5 | Schematic 1.8 to 1.45 V, 3 A LDO with low-V_{CEsat} transistor and TLVH431

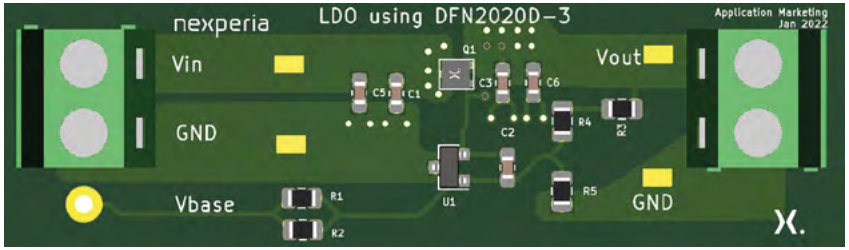


Figure 6 | 3D visualization of an example PCB

Now the most important part for the LDO needs to be chosen – the pass BJT. For this a low V_{CEsat} should be selected. Nexperia has a large portfolio of low-V_{CEsat} type with high forward gain, optimal for LDO applications. The different products PBSS4310PAS, PBSS460PA, PBSS4021NX and PBSS4330X are compared in Table 1.

Table 1: Pass BJT – product comparison

Type	V_{CEsat} (3 A) [V] (max.)	I_C [A]	h_{FE} (2 A) (min.)	V_{BEon} [V] (max.)	V_{CE0}	Package
PBSS4310PAS	0.11	3	275	0.845	10	SOT1061D
PBSS4620PA	0.17	6	260	0.9	20	SOT1061
PBSS4021NX	0.1	7	300	0.85	20	SOT89
PBSS4330X	0.3	3	180	1	30	SOT89

Products which have "PA" in the name come in a modern 2 mm × 2 mm leadless package, while the products with "X" in the name come in a legacy SOT89 package (4.6 mm × 4.25 mm). All products, except the last one in the table, feature a very low V_{CEsat} and a high h_{FE}. To see how the devices perform in the application the products have been tested for load currents between 0.5 and 3 A, while the top case temperature is recorded with an infrared camera. The top case temperature vs. the load current is shown in the graph in Figure 7.

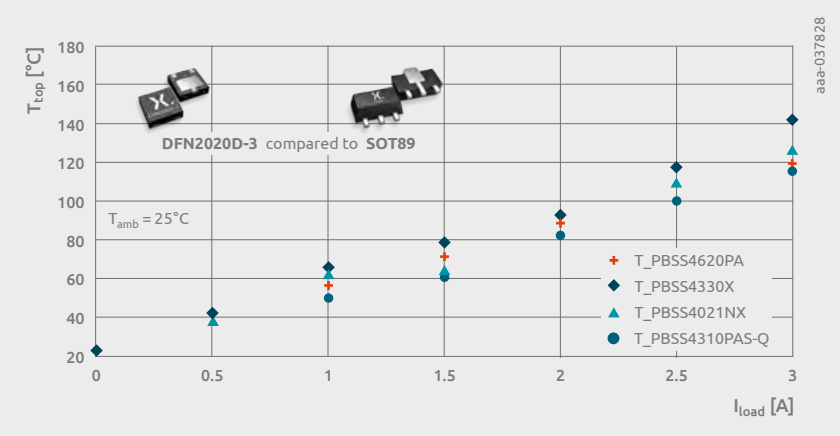


Figure 7 | The graph shows that PBSS4310 shows the best thermal performance compared to the other devices in the group in Table 1, resulting in less power dissipation and higher system efficiency

7.7 Current stabilization

Often it is necessary to generate a stabilized current for loads which cannot be connected to a constant voltage source directly. A classic example of this is an LED or LED string. Because the forward voltage of LEDs depends on temperature with a negative thermal coefficient, current through such a load would increase because of self-heating or an increase in ambient temperature. Eventually thermal runaway could occur, potentially destroying the LEDs.

Figure 1 shows a very simple realization of a current sink. The transistor Q1 gets a bias voltage via a base divider. If the base current is negligible compared to the current through the base resistors R_{B1} and R_{B2} the voltage at the base is $V_{base} = VCC \times R_{B2}/(R_{B1} + R_{B2})$. At the emitter resistor this voltage can be found reduced by the base emitter voltage V_{BE} of the transistor, which is about 0.7 V.

The equation for I_{OUT} is then:

$$I_{OUT} = \frac{VCC \times \frac{R_{B2}}{R_{B1} + R_{B2}} - 0.7\,V}{R_E}$$

The circuit can be changed easily from a constant current sink to a current source if a PNP transistor is used instead of an NPN type, as shown in Figure 2.

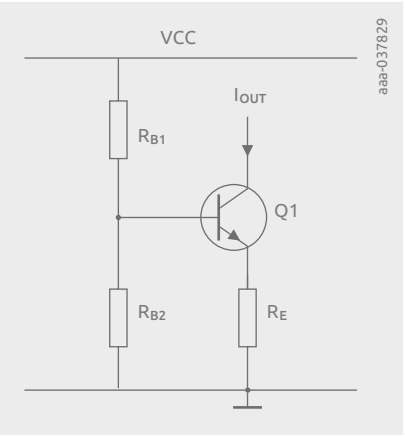


Figure 1 | Simple constant current sink

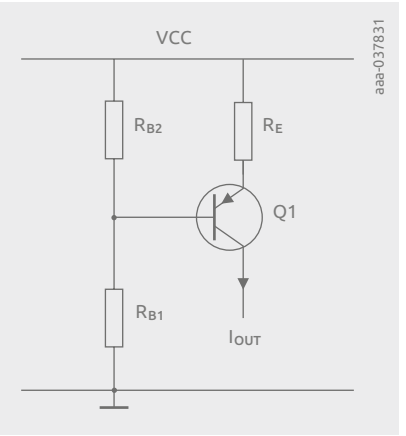


Figure 2 | Simple constant current source

The basic circuits from Figure 1 and Figure 2 have the disadvantage that the output current stability over temperature suffers from the negative temperature coefficient of V_{BE}, which is about −2 mV/K. The output current decreases by about $\Delta I_{OUT}/\Delta T = -2$ mV/RE.

To achieve compensation a p-n diode can be introduced into the base divider, as shown in Figure 3. The diode leads to at least a partial compensation of the thermal drift of the output current. Often a Zener diode is applied in the base divider, as shown in Figure 4. The current I_{OUT} can be calculated roughly with the formula:

$$I_{OUT} \sim \frac{(V_Z - 0.7\,V)}{R_E}$$

The Zener diode has the great benefit that I_{OUT} does not depend on VCC, so there is a better attenuation of voltage changes in the supply and potentially overlaid ripple.

Current mirrors provide a further effective and precise solution for stabilized current sources and sinks. These solutions were discussed in detail in Chapter 7.2.

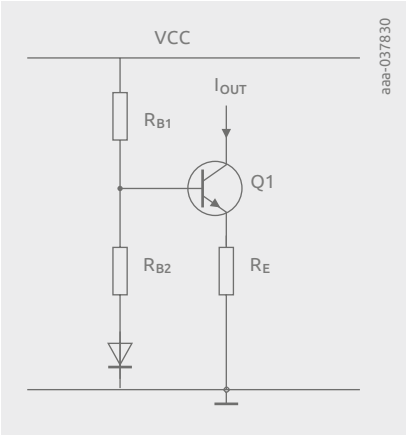


Figure 3 | Constant current sink with enhanced thermal stability

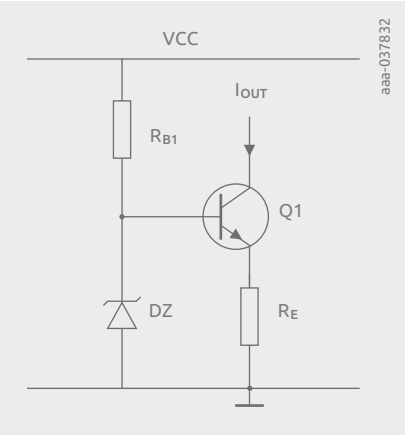


Figure 4 | Constant current sink with Zener diode in base voltage divider

A very precise current stabilization can be achieved if a bipolar junction transistor (BJT) is used as the power stage with support from a base drive controller, which provides an accurate and thermally compensated control loop. A very economical solution is the use of a so-called shunt regulator such as TL431 or TLVH431, as shown in Figure 5. The shunt regulator controls the BJT so that the voltage drop at the sense resistor R_S is the same as the nominal V_{ref} of the controller IC. The output current is then:

$$I_{OUT} = \frac{V_{REF}}{R_S}$$

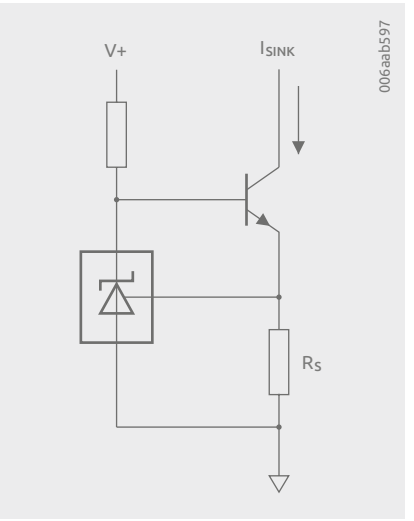


Figure 5 | Constant current sink with TL431 shunt regulator in the base control path of the output current BJT stage

Figure 6 shows a SPICE simulation circuit for this approach. The output at the collector of Q1 is connected to a voltage source V1 that provides the current flowing into the current sink. V1 is modified from 2 V to 20 V. The trace of I_{OUT} shows very good stability of the output current vs. the collector voltage VC of the BJT. The operating point of the current sink has little impact on the output current.

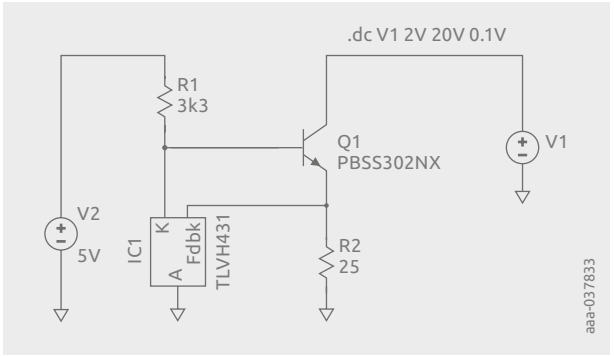


Figure 6 | SPICE simulation of a constant current sink with TLVH431 shunt regulator

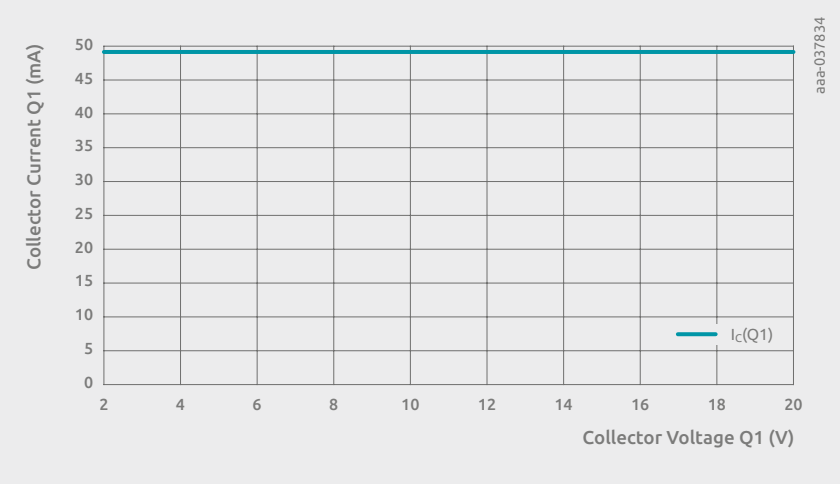


Figure 7 | SPICE simulation result for I_{OUT} (collector current of Q1) vs. V1

Figure 8 shows a current source created with a shunt regulator with an additional output stage realized with a BJT.

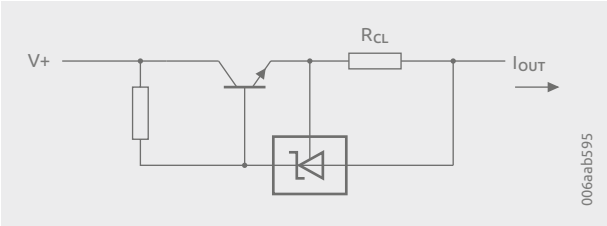


Figure 8 | Constant current source with TL431 shunt regulator in the base control path of the output current BJT stage

7.8 BJT as thermal sensor (ideality parameter)

Temperature has a significant influence on the parameters of bipolar junction transistors (BJTs). This normally undesired effect means it can make sense to use BJTs as thermal sensors. V_{BE} decreases by about 2 mV per Kelvin, so the thermal factor is about –2 mV/K. As a thermal sensor the BJT needs to be run with a constant current, as shown in Figure 1. This simple approach suffers because the spread of V_{BE} over process and the thermal coefficient are both quite large.

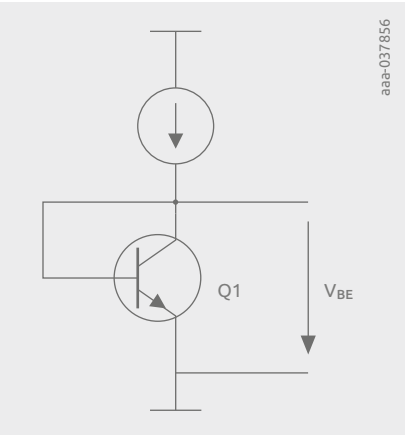


Figure 1 | BJT used as thermal sensor

For a diode characteristic, the so-called Shockley equation is important. It describes the current of the diode ID to voltage VD dependency.

$$I = I_S \times (e^{\frac{V_D}{\eta \times V_T}} - 1)$$

I_S = saturation current, typically in the region of 10-12 A
V_T = kT/q = thermal voltage, ~26 mV for BJTs at room temperature,
with k the Boltzmann constant (1.380649×10^{-16} VAs/K),
T the absolute temperature and
q the elementary charge (1.602×10^{-19} As)
η = ideality factor, for silicon diodes in the range from 1 to 2

The ideality factor η is an important constant for a given device, but this can vary from part to part. This parameter cannot be found in bipolar transistor data sheets. The bipolar transistor PMBT3904 (also named MMBT3904 or 2N3904) is a type which is typically used as a thermal sensor and therefore values for η can easily be found in application notes or data sheets for thermal sensing ICs. The ideality factor for transistors of this type from different vendors is shown in these documents.

The average factor for transistors of PMBT3904 type is about 1.004. Integrated diodes in system chips such as CPUs, GPUs and similar SoCs, which are expected for on-chip temperature sensing, show a similar factor. It would be possible also to use two-pin p-n diodes instead of a three-pin BJT, as shown in Figure 1. However, these diodes have an ideality factor which is much higher. Values range from 1.2 to 1.5. These different factors, deviating significantly from 1.004, would require adapting the calculation formula from the measured diode V_F toward the temperature measured.

If there are more requirements for the accuracy of temperature measurement it is common to measure V_{BE} for two different defined test currents with an exact ratio of 10, for example. In Figure 2 a typical basic topology for a temperature sensing IC using an external BJT sensor is shown. There are two exact current sources which provide current for the sensing BJT. V_{BE} at the transistor is connected to the IC via a high-impedance input stage, and amplification and analog-to-digital conversion is performed. After calculation from V_{BE} to a temperature value, this data is available at a digital interface such as I²C bus.

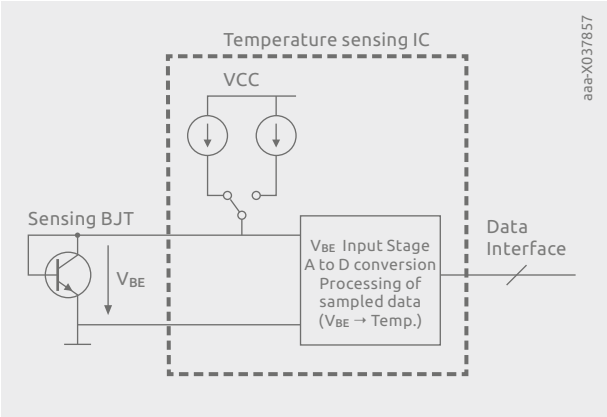


Figure 2 | Two-current temperature measurement approach for a temperature sensing IC

The method of measuring at two operating points leads to the formula below, which is valid for an ideal diode:

$$T = \frac{(V_{BE2} - V_{BE1}) \times q}{\eta k \ln \frac{I_{C2}}{I_{C1}}}$$

7.9 Audio circuits

The role of BJTs in audio circuits

Bipolar junction transistors (BJTs) have been foundational in shaping the landscape of audio circuit design, offering a unique blend of linearity, gain and frequency response. As three-layer semiconductor devices with two p-n junctions, BJTs can operate in active, cutoff and saturation regions, serving predominantly as amplifiers and switches in audio applications. Their ability to provide high gain while preserving the integrity of the audio signal makes them a popular choice, ensuring a high-fidelity reproduction of the original input. Despite the advent of more advanced transistor technologies, the reliability and performance of BJTs have sustained their use in audio circuits.

Understanding amplification classes and the role of BJTs

To grasp the significance of BJTs in audio circuits, it is necessary to explore various amplifier classes and how they employ BJTs.

Class A amplifiers: Known for their exceptional linearity and high fidelity, Class A amplifiers conduct over the entire input cycle. BJTs used in Class A configurations offer excellent linearity but are inherently inefficient, generating substantial heat and requiring significant heatsinking.

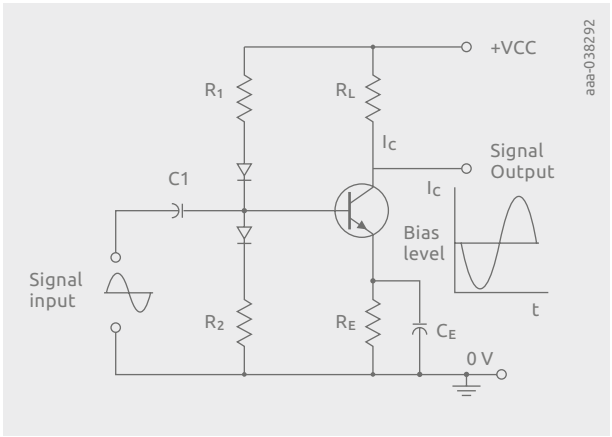


Figure 1 | Class A amplifier

Class AB amplifiers: These amplifiers combine the linearity of Class A with the efficiency of Class B (which conducts over half of the input cycle) to create a more balanced design. Class AB amplifiers utilize two BJTs in a push-pull arrangement, effectively reducing power dissipation. While they offer improved efficiency compared to Class A, there is a potential for crossover distortion at the point where the device switches from one transistor to the other, which necessitates careful biasing of the BJTs.

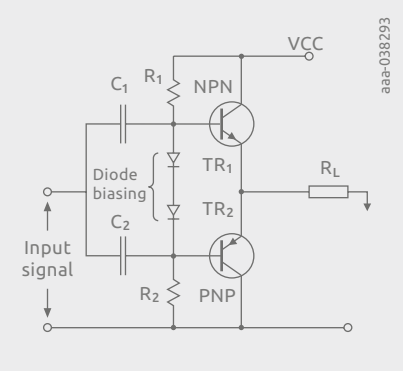


Figure 2 | Class AB amplifier

Class B amplifiers: Offering greater efficiency than Class A, Class B amplifiers can however suffer from crossover distortion. BJTs in Class B configurations can help mitigate this issue, although it may come at the cost of reduced linearity.

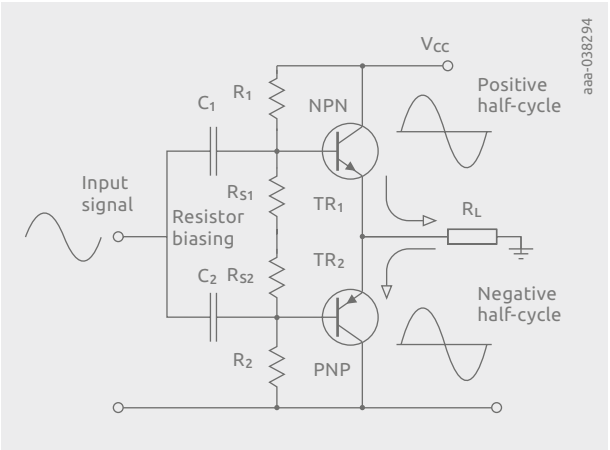


Figure 3 | Class B amplifier

Comparing BJTs with MOSFETs and Class D amplifiers

When considering alternatives to BJTs in audio circuits, MOSFETs and Class D amplifiers are often explored.

MOSFETs: With their high input impedance and swift switching capabilities, MOSFETs present a viable option. They generally require less biasing, resulting in lower power consumption. However, they may introduce distortion, especially at low frequencies and signal levels.

Class D amplifiers: These amplifiers operate by rapidly switching the output transistors on and off to create a pulse-width modulated representation of the input signal. This approach results in exceptional efficiency and minimal heat dissipation. Despite these advantages, potential issues such as electromagnetic interference (EMI) and distortion can arise, particularly if the filtering is not adequately designed.

In contrast, BJTs offer a superior linearity and signal integrity, especially critical in high-fidelity audio applications. They ensure that the output remains a true representation of the input, even if this comes at the cost of efficiency and power consumption. While MOSFETs and Class D amplifiers provide alternatives with their own set of advantages, BJTs hold a unique position in the realm of audio amplification, particularly in Class A and Class AB configurations where audio fidelity is important.

Signal generation and filtering

In the dynamic field of audio circuit design, precision and reliability in signal processing are paramount. This chapter delves into the application of BJTs in various audio circuit components such as signal generators, voltage-controlled oscillators (VCOs), low-frequency oscillators (LFOs) and filters, as well as high-frequency (HF) and intermediate-frequency (IF) generators.

Signal generators are indispensable tools in audio circuits, tasked with producing a variety of waveforms. BJTs are particularly favored in this domain due to their rapid response and ability to generate signals across a broad frequency spectrum. The bipolar nature of BJTs ensures a consistent, linear amplification, crucial for producing stable and precise waveforms. Their low intrinsic noise also contributes to the purity of the generated signals, a vital aspect in audio applications. Designers are advised to optimize biasing conditions to enhance the linearity and efficiency of BJT-based signal generators. Figure 4 shows a circuit to generate a sawtooth with discrete BJTs.

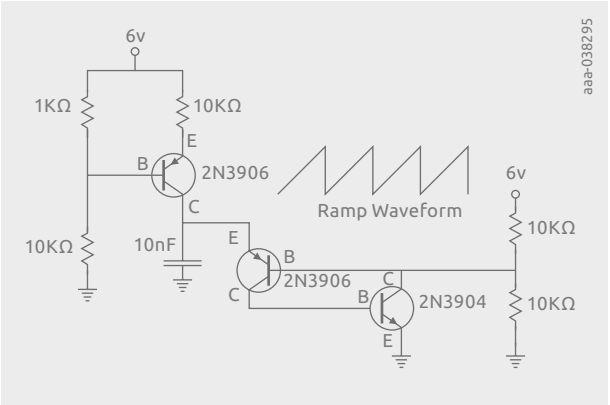


Figure 4 | Sawtooth generator

In VCOs, where the output frequency is modulated by an input voltage, BJTs are renowned for their exemplary performance. They offer a linear control-voltage-to-frequency response, ensuring accurate and consistent frequency modulation. Their high transconductance is beneficial in achieving a faster response time, enhancing the agility of the VCO. Compared to MOSFETs, BJTs exhibit less variance in performance across different operating conditions, providing a more reliable solution for VCO applications in audio circuits. Such circuits include the Hartley and Colpitts inductor-capacitor (LC) oscillators (shown in Figure 5).

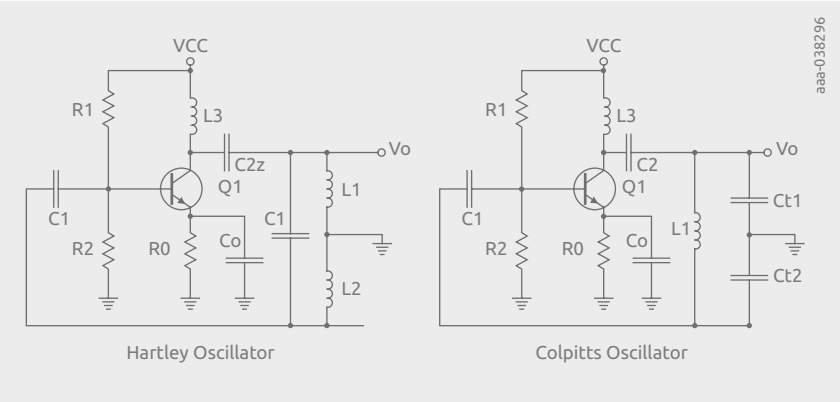


Figure 5 | VCO applications (Hartley and Colpitts oscillators)

Low-frequency oscillators (LFOs) are pivotal in modulating various audio parameters to create diverse sound effects. The utilization of BJTs in LFO circuits guarantees stability and precision at low frequencies. Their high input impedance minimizes loading effects, preserving the integrity of the signal path. Design considerations should include careful selection of passive components to maintain the BJT in its optimal operating region, ensuring a consistent LFO performance. An example is shown in Figure 6, with tunable phase-shift oscillator.

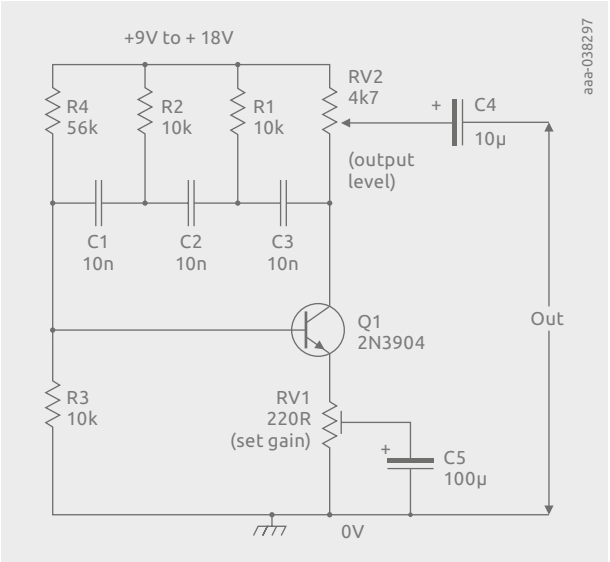


Figure 6 | Low-frequency phase-shift oscillator

Filters play a critical role in shaping the frequency response of audio signals. In active filter configurations, BJTs stand out for their high gain and bandwidth capabilities. They ensure a flat, linear response across the desired frequency range, resulting in accurate signal processing. The low noise characteristics of BJTs also contribute to maintaining the signal's fidelity, particularly in audio applications where signal integrity is crucial. Designers are encouraged to pay attention to the thermal stability of BJTs in filter applications, ensuring consistent performance across various operating conditions. In Figure 7 a bandpass example is shown, using a single transistor.

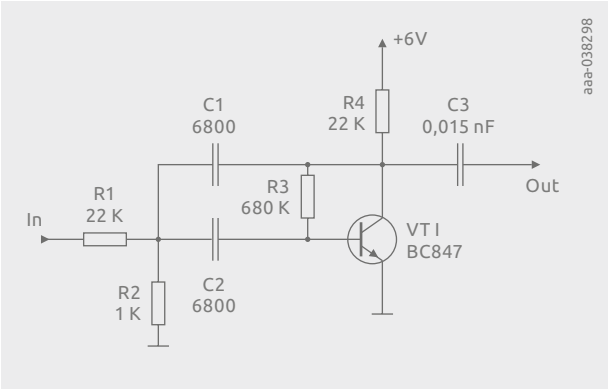


Figure 7 | Single-transistor bandpass

In the realm of HF and IF generation, BJTs are prized for their ability to operate efficiently at high frequencies. Their linearity ensures that the generated signals maintain integrity, which is of utmost importance in communication and RF applications. The thermal stability of BJTs is a significant advantage, especially in environments with fluctuating temperatures, providing a robust solution for HF and IF signal generation.

Considerations when using BJTs in audio circuits

Situations in which the load presents a low impedance, necessitating substantial drive current, pose challenges for operational amplifiers, potentially leading to overheating or triggering current-limiting mechanisms. This scenario is exemplified by audio power amplifiers.

Achieving optimal noise performance is crucial, particularly in applications involving low source resistances of 500 Ω or less. In such contexts, discrete BJTs demonstrate superior performance compared to operational amplifiers. Prevalent applications include moving-coil head amplifiers and microphone preamplifiers, which mostly utilize discrete input devices. The operational amplifiers employed in these configurations, despite potentially modest noise specifications, contribute to open-loop gain (for enhanced linearity) and load-driving capabilities.

Applications demanding the best distortion performance may necessitate considerations beyond operational amplifiers, as these typically possess Class B or AB output stages. Many of these amplifiers exhibit noticeable crossover artifacts in the distortion residual. In contrast, discrete operational amplifiers, with their enhanced power dissipation capabilities, can incorporate Class A output stages, avoiding crossover distortion issues.

Circumstances that necessitate provisioning a low-voltage supply exclusively for one or two operational amplifiers may make the associated costs of additional transformer windings, rectifiers, reservoirs and regulators prohibitive. In these scenarios, the utilization of discrete transistors such as an emitter-follower to drive a power amplifier from a low impedance may present a more economical and spatially efficient solution. The contemporary landscape of automated component insertion further mitigates the cost implications of integrating additional discrete components on the PCB.

From a marketing perspective, strategically positioning products with discrete circuitry may appeal to a niche customer segment skeptical of operational amplifiers, potentially creating a unique market opportunity.

7.10 Discrete logic circuits

Bipolar junction transistors (BJTs) are often used in switching circuits where only two states are required. These would be the on-state and the off-state for a binary logic application. General-purpose BJTs and resistor-equipped transistors (RETs) can be found in this application area. RETs are referred to as "digital BJTs" by some vendors because of this background. They have the important benefit that a base series resistor or a base divider is integrated already, so the component count is reduced.

Discrete logic is used if the switching speed requirements are low. Furthermore, standard logic families are limited in terms of the voltages they can address. The input voltage of a discrete BJT solution can be adapted easily by proper selection of the base divider, and the output voltage is not limited to low voltages but can address a wide range with a suitable VCE rating of the chosen transistors.

In Figure 1, a basic common emitter configuration circuit is used as an inverter stage. When the input voltage is high, the BJT turns on the output, providing a low state. For the opposite scenario of a low-state input signal, the BJT is turned off and the output is pulled up to a high state. The circuit described is an open-collector inverter stage. The high-state output voltage is determined by the supply voltage VCC. The VCE rating needs to be larger than or equal to the desired high level at the output. Discrete logic can provide a requested logic function as well as a voltage level conversion.

Table 1 shows a simple logic Table for an inverter.

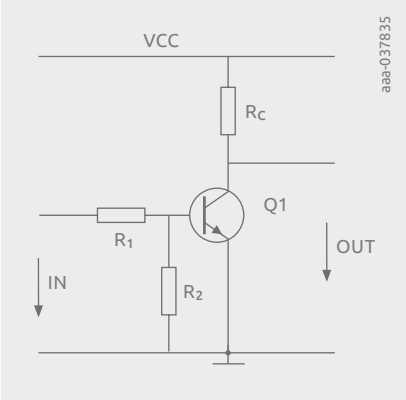


Figure 1 | BJT as logic inverter stage

Table 1: Logic Table for an inverter

Input state	Output state
0	1
1	0

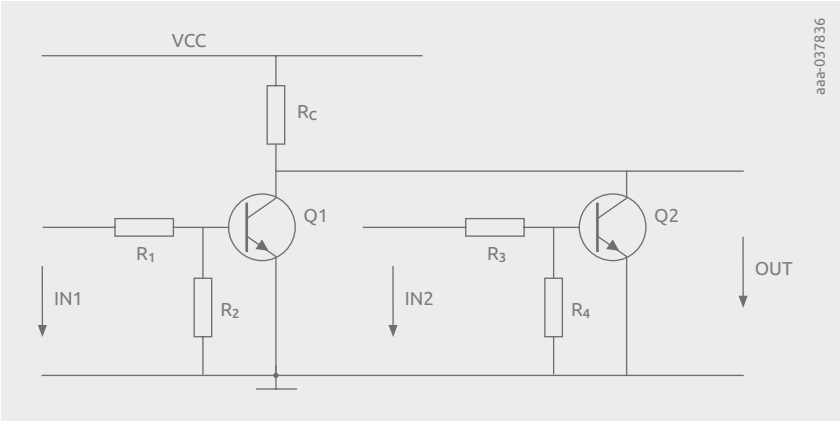


Figure 2 | NOR gate with two inputs

Figure 2 shows how the logic function of a dual-input NOR gate can be realized. Two BJTs are put in parallel and share a common collector resistor. If at least one of the BJTs turns on, the output delivers a low state. The output acquires a high state if both inputs are logic 0. This behavior is shown in Table 2 for all combinations of input states. If the application requires the function of an OR gate an additional inverter stage as shown in Figure 1 can be applied. The number of inputs for the NOR gate can be easily increased with additional BJT stages. Because the BJTs work in parallel, the tendency toward having more inputs does not change the output levels.

Table 2: Logic Table for a two-input NOR gate

IN2	IN1	Output state
0	0	1
0	1	0
1	0	0
1	1	0

If the switching BJTs are put in series instead of a parallel structure, the logic function of a NAND gate is realized; Figure 3 shows this solution. The output provides a low state only if both inputs are high. In all other combinations of input states, the output stays high. The function Table is shown in Table 3. The number of inputs can be increased by putting more BJTs in series. The low level becomes higher because the saturation voltages of the transistors add up. With an inverter behind the NAND gate the logic function of an AND gate can be realized.

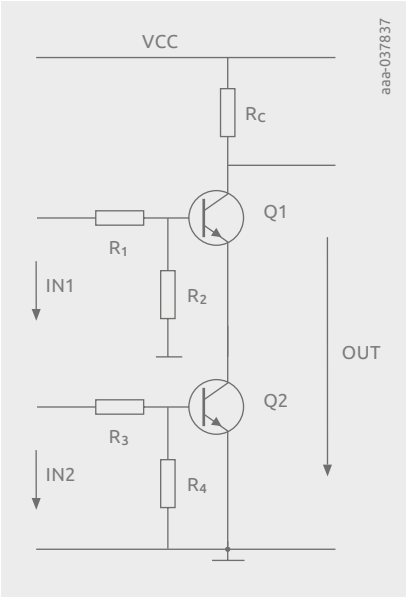


Figure 3 | NAND gate with two inputs

Table 3: Logic Table for a two-input NAND gate

IN2	IN1	Output state
0	0	1
0	1	1
1	0	1
1	1	0

Based on the described basic logic gates, other logic functions can be realized by combining the principles for more sophisticated logic behavior. In all more complex systems, it is required to monitor several signals such as power-good indication signals, signals indicating that the system temperature is in the desired operating area, the status of position switches or similar signals. Such signals need to be tracked and processed with a logic function which delivers a desired output signal for defined conditions of all the inputs evaluated. For example, it can be important as part of power sequencing that several supply voltages are present before an additional supply voltage is started. In automotive applications, variants of the circuits discussed can always be found. Many switching tasks do not require a very short processing delay, or propagation delay (tpd, as it is called in the context of logic devices). Logic gates require a small, stabilized supply voltage. Modern logic families have supply voltages less than or equal to 5 V. To interact with higher-voltage domains, it is necessary to add interfacing stages. The circuits described above easily function for voltage up- and down-conversion between inputs and outputs. Also, input voltages with different levels can be processed; this is achieved by a proper base divider design. Therefore, discrete logic is a cost-efficient solution for control-signal processing where decent speed is required.

In Figure 4 a basic discrete circuit for a flipflop is shown. While one of the transistors is turned on, the other is turned off. If Q1 is in the off-state, the collector has the voltage level of VCC. The base of Q2 gets base drive, then it is turned on and thus keeps Q1 in the off-state. If the base of Q2 is forced to GND for a short time, the logic states of the two BJTs swap. A flipflop is a one-bit storage stage. If we assign the collector of Q2 as output V_{OUT}, Q1 is the inverted logic output of V_{OUT}, or V_{OUTN}.

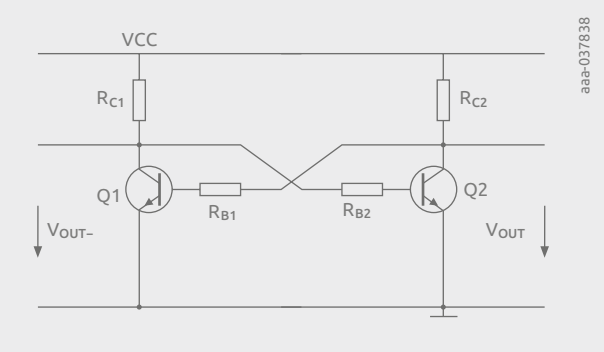


Figure 4 | Flipflop realized with BJTs

The basic flipflop shown in Figure 4 can be extended with two digital inputs to apply set or reset pulses. An NPN transistor is added as a switch between each base of the BJTs Q1 and Q2 to GND to realize this function. Such a circuit is known as R_S flipflop, as shown in Figure 5. The base of Q4 is the set input and the base of Q3 provides the reset input. With a high signal applied to one of the control inputs, the flipflop can be set or reset. It is not useful to apply a set and reset pulse at the same time. In this case both transistors, Q1 and Q2, would be turned off and, after releasing the signals at the same time, the flipflop would acquire a random output stage.

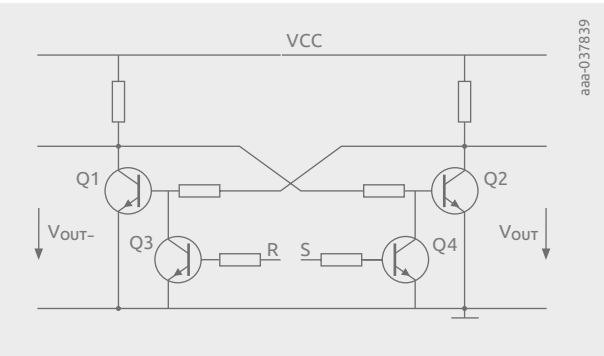


Figure 5 | RS flipflop realized with BJTs

A flipflop can be created with two NOR gates as shown in Figure 6, and alternatively with two NAND gates. In the latter case the set and reset inputs react on low levels, whereas the approach with NOR gates reacts on high pulses. Table 4 is the logic Table for such a flipflop. If both inputs are kept at 0, the flipflop retains the state, meaning it stores the logic state. Applying a high state to either the set input S or the reset input R lets the flipflop jump to the related state at the output Q. If Q is high already, there is no change if a set pulse is applied. The same is true of course if the flipflop is cleared already and a reset pulse is provided. Applying a set and reset pulse at the same time forces both outputs to low state. This condition is not a desired operation, and it is not logical to try to set and reset a one-bit memory at the same time.

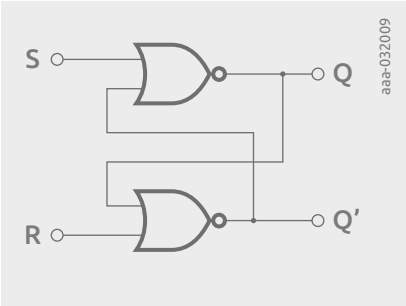


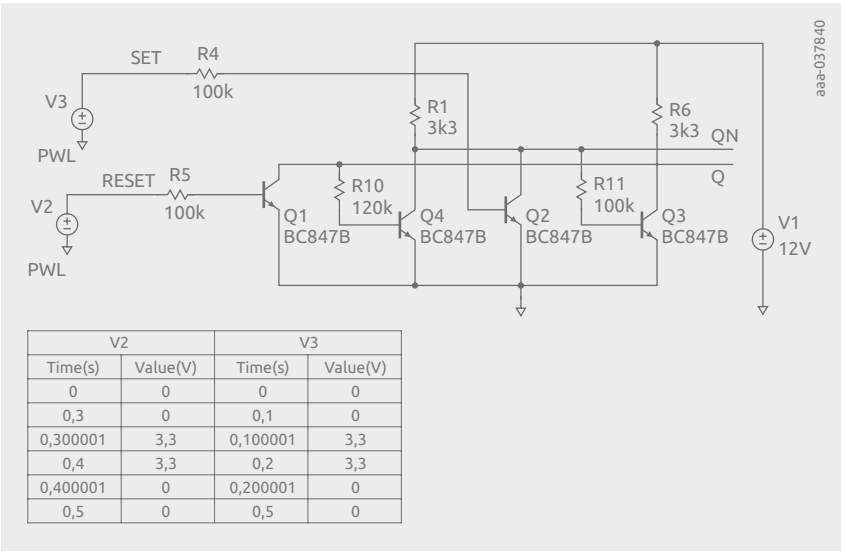
Figure 6 | RS flipflop realized with two NOR gates

Table 4: Logic Table of a flipflop realized with two-input NOR gates

S	R	Q	Q'
0	0	Store	Store
0	1	0	1
1	0	1	0
1	1	0	0

In Figure 6 the NOR gate structure for a flipflop is realized with discrete BJT and is simulated in SPICE. The NOR gate discussed above was shown in Figure 2. The set and reset transistors now switch directly to the Q and QN nodes and not to the base nodes as in Figure 5. The propagation delays for set and reset get shorter with this realization compared to the prior solution. The base resistor for Q1 is chosen slightly higher. This small asymmetry in the design guarantees that the flipflop starts in a cleared and defined condition after power-on.

The simulation result is shown in Figure 8. The flipflop starts in a cleared state, then is set with a set pulse (dark blue trace) and reset afterward with a reset pulse (red trace). The output waveform shows the desired behavior, shown as a light-blue trace.



V2		V3	
Time(s)	Value(V)	Time(s)	Value(V)
0	0	0	0
0,3	0	0,1	0
0,300001	3,3	0,100001	3,3
0,4	3,3	0,2	3,3
0,400001	0	0,200001	0
0,5	0	0,5	0

Figure 7 | RS flipflop realized with two NOR gates based on BJTs in SPICE

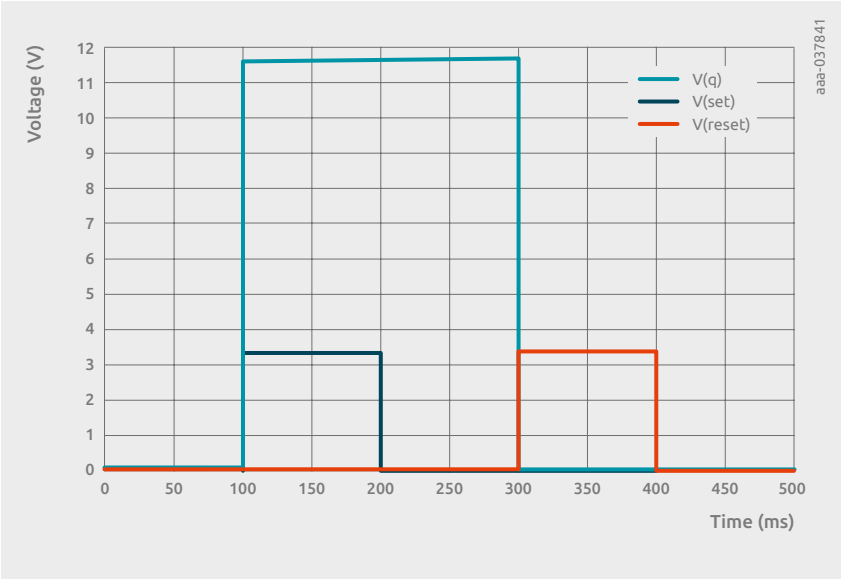


Figure 8 | Simulation results for the RS flipflop

With a small change in the circuit of the basic flipflop, a generator for rectangular signals can be created; a so-called "astable multivibrator". The name was given historically because signals with a rectangular waveform have many harmonics. For an ideal rectangular signal with 50% duty cycle, only odd harmonics to the fundamental waveform exist. The component with 3 × f0 has an amplitude damped by a factor of 3, and the next frequency component at 5 × f0 has an amplitude reduced by a factor of 5 related to f0, so the harmonics follow the equation:

$$f_{(2n+1)} = \frac{f_0}{(2n+1)} \quad for\ (n \geq 1)$$

The circuit diagram is shown as a SPICE diagram in Figure 9. The bases are cross-coupled to the corresponding opposite transistor stage with capacitors and biased to the supply voltage. The result of SPICE simulation shows an output signal with about 1 kHz frequency, as in Figure 10. Oscillation frequency can be calculated with the formula:

$$f \sim \frac{1}{2 \times ln(2) \times R_B \times C} \sim \frac{1}{1.39 \times RC}$$

In the simulated example the equation delivers f = 1.058 kHz, which is close to the outcome of the simulation. If the RC time constants for the two sub-stages are designed differently, the duty cycle changes as T1 ~ ln(2) × R2 × C1 and T2 ~ ln(2) × R3 × C2 need to be considered, and the frequency formula becomes:

$$f \sim \frac{1}{ln(2) \times (R2 \times C1 + R3 \times C2)}$$

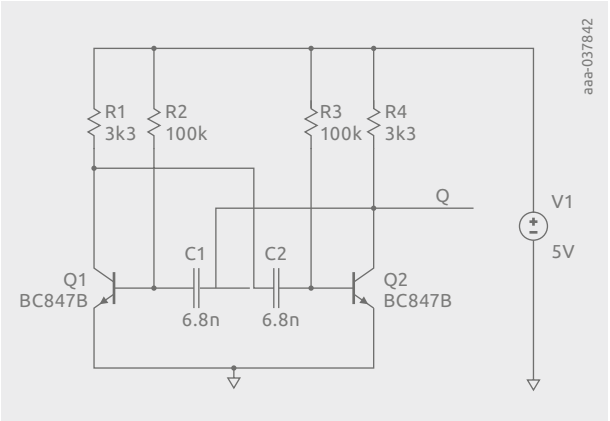


Figure 9 | Astable multivibrator SPICE circuit example

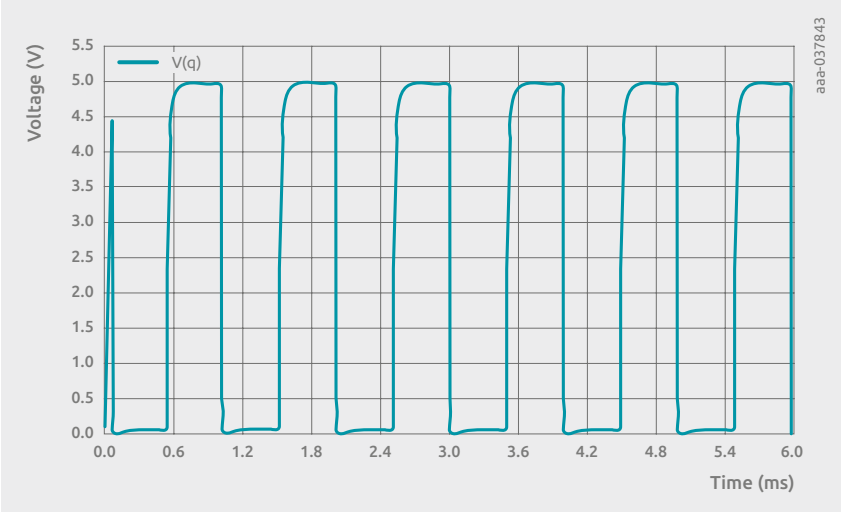


Figure 10 | Astable multivibrator SPICE simulation result

One detail is important to mention for the multivibrator circuits that requires attention from the designer. While Q1 is turned on, for example, there is about 0.7 V at the base and the common node with C1. The other side of the capacitor is connected to the collector of Q2, which is in the off-state. So the capacitor is charged to VCC – 0.7 V. If the state of the multivibrator changes, this charged capacitor is switched with its positive pole to GND, and this means the base of Q1 gets a negative voltage of about –(VCC – 0.7 V). Most BJTs are specified so that VBE0 should not exceed a voltage from 5 V to 7 V depending on the chosen type. For the BC547B in the example 6 V is the limit. This limit must be obeyed with respect to the supply voltage of the circuit.

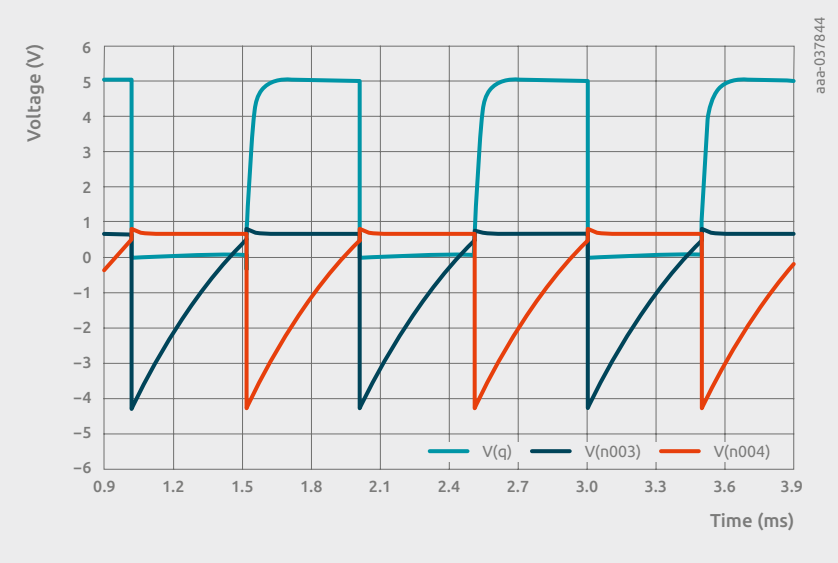


Figure 11 | Astable multivibrator SPICE simulation

Another important variant which looks like a flipflop for one half and like the astable multivibrator for the other half is called a monostable multivibrator, or one-shot multivibrator. The whole circuit is shown in Figure 12. The transistor Q3 is applied as input stage to trigger the circuit. The simulation result in Figure 13 shows how this design works. The circuit creates a high-state output pulse starting with the rising edge of the input pulse. The length of this pulse is roughly $TP \sim \ln(2) \times R2 \times C1$, with quite a good match between theory and simulation.

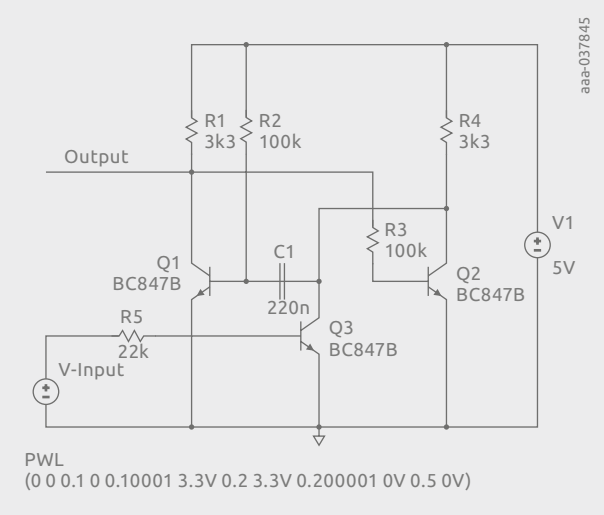


Figure 12 | Monostable multivibrator SPICE circuit example

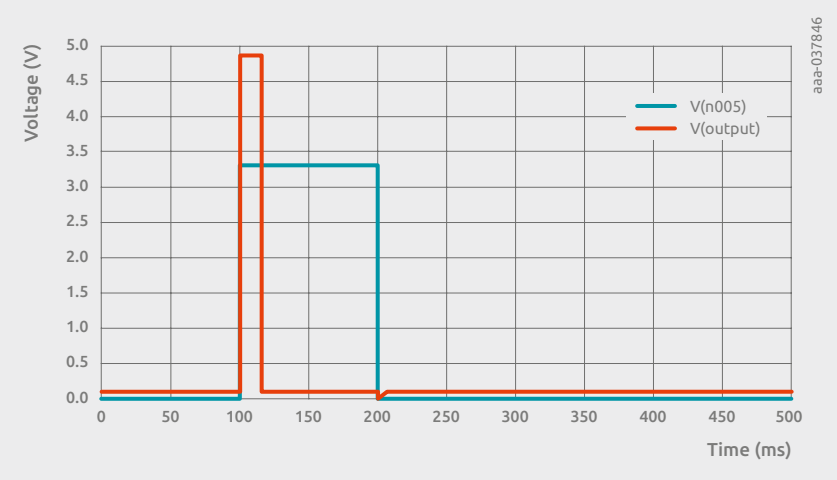


Figure 13 | Monostable multivibrator SPICE simulation result

The monostable retriggerable multivibrator discussed is a nice solution to create pulses with a defined length triggered by the rising edge of a trigger pulse. It also can be used to realize delays or to generate pulses which are delayed to the input pulse. For this, two one-shots are put in series. Such a pulse delay is shown in Figure 14. The one-shot on the left side creates an output pulse with a length that can be adjusted with the time constant of $T1 \sim \ln(2) \times R2 \times C1$. This output pulse gets inverted with the inverter stage realized with Q7. The inverted pulse triggers a second one-shot, which generates a delayed pulse with the length of

T2 ~ ln(2) × R8 × C2. T1 is the delay time between the rising edges of the input pulse and the rising edge of the output pulse from one-shot 2.

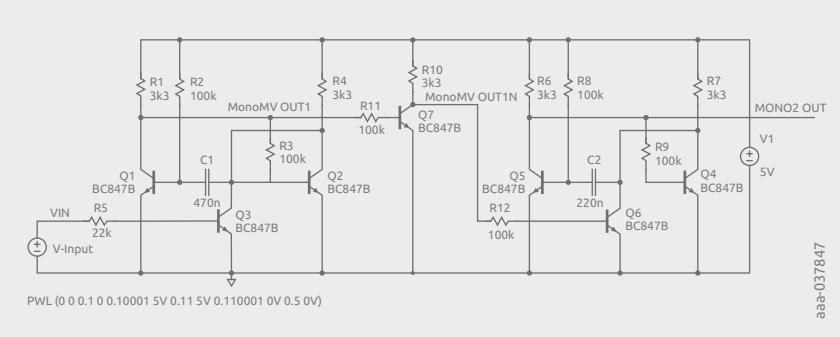


Figure 14 | Pulse delay consisting of two one-shots and an inverter (Q7) in between

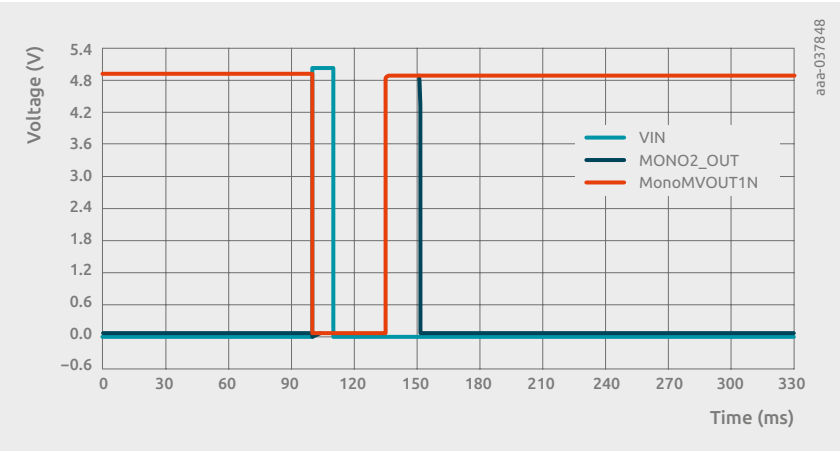


Figure 15 | SPICE simulation result: trigger input pulse in light-blue, inverted output of one-shot 1 in red and the output pulse in dark blue generated by one-shot 2

7.11 Discrete gate-driver with BJTs

Driving power semiconductors

Bipolar junction transistors (BJTs) play a significant role in driving power switches. They offer high flexibility in the design of a gate driver, and due to their high peak power capability, they provide advantages in applications where cost performance plays a significant role.

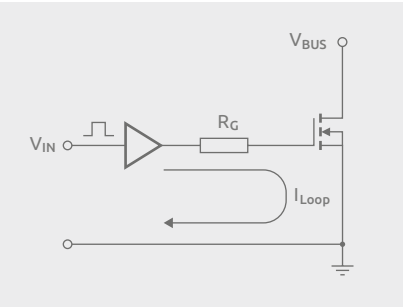


Figure 1 | Driving of a power switch

In applications utilizing active power semiconductor switches like IGBTs, MOSFETs or GaN FETs, the controller does not provide the voltage level or the needed output power to drive the switch. Therefore, an external driving circuit has to be considered, as shown in Figure 1. A carefully designed gate driver that considers the minimization of loop inductances by the PCB layout and the choice of modern package technologies allows a reliable and efficient usage of the power switch. BJTs offer significant current amplification capabilities, making them well-suited for providing the gate charge for the switch. The high current gain of BJTs enables the delivery of substantial base current, facilitating rapid charging or discharging of the gate capacitance and thereby minimizing switching delays. MOS-gated switches commonly possess a gate capacitance that must be effectively managed during switching operations. The inherent ability of BJTs to furnish significant base current ensures that the gate capacitance can be rapidly charged or discharged, thus mitigating any adverse impact on switching performance. Utilizing BJTs in configurations that enable voltage clamping of the switch's gate voltage within the specific limits is paramount for preventing excessive voltage stress. By implementing appropriate clamping mechanisms, engineers can ensure that the power switches operate within their safe operating regions during switching, thereby facilitating faster transitions. Complementary push-pull configurations, such as totem pole drivers employing both npn and pnp BJTs, are instrumental in achieving high-speed switching in applications. By harnessing the complementary characteristics of BJTs, engineers can minimize transition times and enhance overall switching speed. The versatile nature of BJTs allows them to source and sink current efficiently, enabling rapid charging and discharging of the gate capacitance during the turn-on and turn-off phases, respectively. This capability enhances the dynamic performance of the switch in power electronics systems.

Driving circuits examples

A common, cost-effective drive circuit for driving an active switch is a non-inverting bipolar totem pole circuit acting as a booster, as shown in Figure 2. Similar to all external drivers, this circuit manages the current spikes. It minimizes power losses, conditioning the signal for the switch.

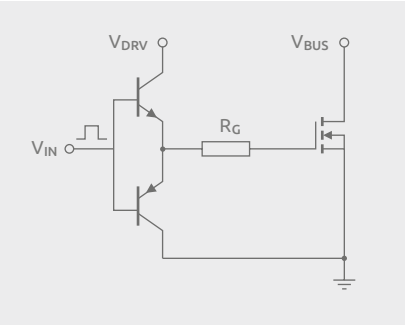


Figure 2 | Bipolar totem pole driver

A single turn-off circuit for achieving rapid turn-off is the pnp turn-off circuit, as illustrated in Figure 3(a) and the npn-version in Figure 3(b). This circuit employs Q_{off} to locally short the gate and source at the active switch terminals during the turn-off process. The inclusion of RG controls the turn-on speed, while D_{on} facilitates the path for the turn-on current. Additionally, D_{on} safeguards the base-emitter junction of Q_{off} against reverse breakdown at the initial stages of the turn-on procedure. The advantage of this approach is that it confines the high peak discharge current of the power switch input capacitance within the smallest possible loop, encompassing the gate, source, and connections of the collector and emitter of the two transistors.

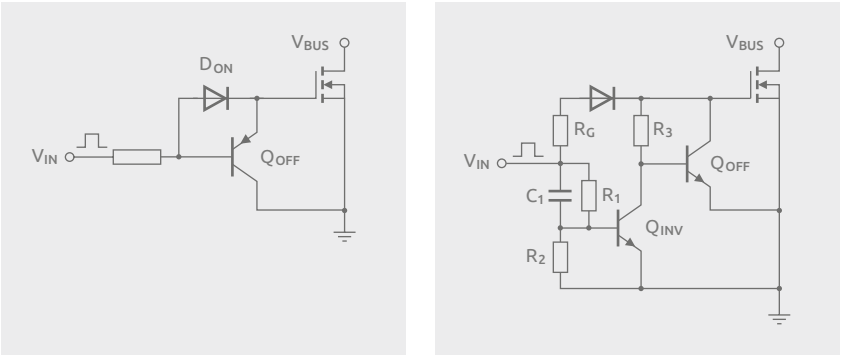


Figure 3 | pnp Turn-off Circuit (a) npn-turn-off circuit (b)

The turn-off current doesn't return to the driver, avoiding any ground bounce issues and significantly reducing the driver's power dissipation. The turn-off transistor bypasses the gate drive loop inductance, the potential current sense resistor, and the driver's output impedance. Additionally, it's noteworthy that Q_{off} never saturates, which is crucial for rapid turn-on and turn-off switching.

Chapter 8

Simulations and software analysis

The importance of simulation in electronics design

This chapter is a comprehensive guide to the simulation and software analysis of bipolar junction transistors (BJTs). It aims to bridge the gap between theoretical knowledge and practical application, providing readers the tools and information necessary to use simulation in their electronic designs.

Electronics design is complex and multifaceted, requiring precision, efficiency and a deep understanding of component behavior under various conditions. In this context, simulation is an indispensable tool, playing a pivotal role in the design and analysis of electronic circuits and systems. The importance of simulation in electronics design cannot be overstated, bringing the engineer a multitude of benefits and capabilities. Essentially, simulation allows for the modeling of electronic circuits and systems in a virtual environment. This provides designers with the ability to scrutinize the behavior of components, such as BJTs, under diverse conditions without the need for physical prototypes. The cost and time savings associated with this are substantial, as physical prototyping can be resource-intensive and time-consuming, particularly in the case of complex or large-scale designs. Additionally, time-consuming analysis of multiple test conditions on a basic circuit or single device can profit greatly from simulation. The precision and control offered by simulation is unparalleled. Engineers can manipulate a wide array of parameters and variables, conducting "what if" analyses to explore the impact of changes in component values, operating conditions or circuit configurations. This enables the identification of optimal component values and configurations, leading to enhanced performance, reliability and efficiency in the final product.

Simulation also plays a critical role in the identification and mitigation of potential issues and failures before they occur in the real world. By simulating various stress conditions and scenarios, designers can pinpoint vulnerabilities and weaknesses in the design, so corrective actions can be taken proactively. This proactive approach to problem-solving not only saves time and resources but also contributes to the creation of more robust and reliable electronic products. Furthermore, simulation fosters innovation and creativity in electronics design. The ability to quickly and easily test out new ideas or unconventional approaches in a virtual environment encourages experimentation and exploration. This can in turn lead to breakthroughs and novel solutions, driving the advancement of technology and design practices.

In the context of learning, developing skills and understanding the device and the circuit, simulation serves as a powerful teaching tool, aiding in the comprehension of complex electronic principles and behaviors. Students and newcomers to electronics design can experiment and learn in a risk-free virtual environment, building their skills and confidence before transitioning to real-world applications.

In conclusion, the importance of simulation in electronics design is manifold, offering cost and time savings, precision, control, proactive problem-solving, innovation and educational benefits. It is an invaluable asset in the modern electronics design toolkit, empowering designers to create more reliable, efficient and innovative electronic products and systems.

Nexperia doesn't just develop efficient products and innovative technologies. It also creates the most advanced tools to provide knowledge, learning and support for design engineers. These include compact device models (SPICE), 3D models (STEPS) and design tools.

Simulation tools and software

This chapter provides an overview of the various simulation tools and software available for BJT analysis. It discusses their features and capabilities, and how to choose the right tool for the situation.

Overview of popular simulation software

This section introduces some of the most widely used BJT simulation software, providing a brief description of each and discussing their respective strengths and weaknesses.

LTspice®
An analog electronic circuit simulation software, produced by semiconductor manufacturer Analog Devices (originally by Linear Technology). It is the most widely distributed and used SPICE software in the industry.

Xyce
Backend simulator that supports parallel simulation; known to be capable of solving extremely large circuits.

Ngspice
Backend simulator for Altium Designer/Eagle/KiCad

PSpice
Cadence Design Systems

SIMetrix
Mixed-signal circuit simulator designed for ease and speed

QSPICE™
Simulator, free software by Qorvo

SPICE
Historically important simulator. Many analog simulators are based on this project, and SPICE-named models are usually compatible with most EDA tools.

Models

There are two main categories of models: device models and subcircuit models. You can verify the syntax by opening the downloaded file using a text editor. Device models pertain to individual components such as BJTs and diodes, and their syntax begins with ".MODEL". On the other hand, subcircuit models encompass configurations involving multiple components like BJTs and diodes. Their syntax starts with ".SUBCKT" and concludes with ".ENDS". Within the subcircuit models category, MOSFET models are referred to as macro models, representing the MOSFETs using equivalent circuits composed of passive and active elements, along with the power supply. Consequently, you will find multiple instances of ".MODEL". For SiC power devices, IGBTs and higher-level models are usually described by behavior models that depict device characteristics through specific numerical expressions.

Simulation methodology

This section provides a comparison of different simulation tools, offering criteria for selecting the most appropriate software based on specific needs and requirements.

Nexperia models are based on SPICE3; the SPICE models are only a representation of the device and may not represent the physical layout of the device and its physical behavior. The same method that is applied to BJTs can also be applied to diodes. For BJTs we will focus on open-source models developed by the University of Berkeley, usually referred to as "Berkeley SPICE models".

The user of the device model can simply open the .lib file downloaded or obtained by using a text editor. The content of the file can be copied as plain text to the schematic itself and also edited within the next to the circuit itself. That avoids the installation in a specific library setup. In complex circuit arrangements, however, a library management tool should be used, and this can be installed within the library structure of the simulation platform.

Below is an example of SPICE model BC847B. The model represents the transistor behavior, and optimization was carried out to improve the quasi-static by adding an additional diode for the reverse operation of the device:


```
************************
************************
******
** BC847B
.SUBCKT BC847B 1 2 3
Q1 1 2 3 MAIN 0.8636
Q2 11 2 3 MAIN 0.1364
RQ 11 1 324.8
D1 2 1 DIODE
*
.MODEL MAIN NPN
+ IS = 1.124E-14
+ NF = 0.9872
+ ISE = 2.566E-15
+ NE = 1.661
+ BF = 280
+ IKF = 0.09455
+ VAF = 36.27
+ NR = 0.9859
+ ISC = 7.015E-18
+ NC = 0.9228
+ BR = 7.047
+ IKR = 0.8167
+ VAR = 16.61
+ RB = 150
+ IRB = 0.0008356
+ RBM = 0.8289
+ RE = 0.804
+ RC = 0.2454
+ XTB = 1.382
+ EG = 1.11
+ XTI = 7.452
+ CJE = 1.264E-11
+ VJE = 0.7056
+ MJE = 0.3401
+ TF = 6.258E-10
+ XTF = 25
+ VTF = 2
+ ITF = 0.277
+ PTF = 0
+ CJC = 3.624E-12
+ VJC = 0.5036
+ MJC = 0.365
+ XCJC = 1
+ TR = 1.55E-07
+ CJS = 0
+ VJS = 0.75
+ MJS = 0.333
+ FC = 0.78
.MODEL DIODE D
+ IS = 1.365E-15
+ N = 0.988
+ BV = 1000
+ IBV = 0.001
+ RS = 2163
+ CJO = 0
+ VJ = 1
+ M = 0.5
+ FC = 0
+ TT = 0
+ EG = 1.11
+ XTI = 3
.ENDS
```

The model parameters are explained in Table 1.

The model is derived from the SPICE Gummel–Poon (SGP) model and represents the equivalent circuit shown in Figure 1.

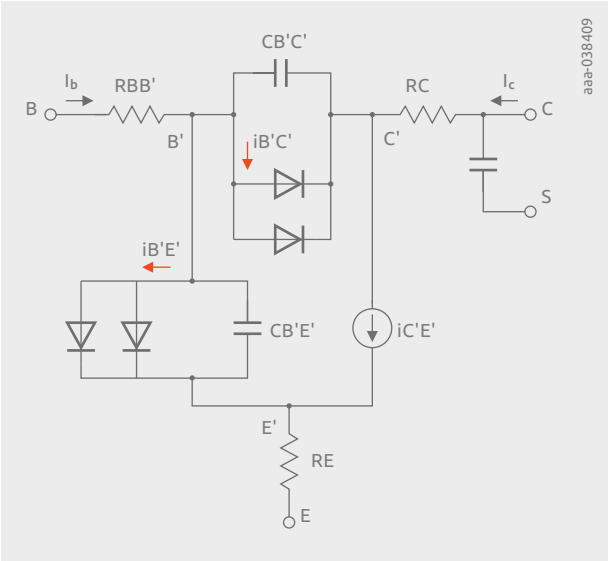


Figure 1 | SGP

Table 1: Model parameter description and code examples.

Name	Property	Unit	Parameter	Code example
IS	Current	A	Transport saturation current	`+ IS = 1.124E-14`
NF	Current	n.a.	Forward-current emission coefficient	`+ NF = 0.9872`
ISE	Current	A	B–E leakage saturation current	`+ NE = 1.661`
BF	Current	n.a.	Ideal maximum forward beta	`+ BF = 280`
IKF	Current	A	Corner for forward-beta high-current roll-off	`+ IKF = 0.09455`
VAF	Current	V	Forward early voltage	`+ VAF = 36.27`
NR	Current	n.a.	Reverse-current emission coefficient	`+ NR = 0.9859`
ISC	Current	A	B–C leakage saturation current	`+ ISC = 7.015E-18`

Name	Property	Unit	Parameter	Code example
NC	Current	n.a.	B–C leakage emission coefficient	`+ NC = 0.9228`
BR	Current	n.a.	Ideal max. reverse beta	`+ BR = 7.047`
IKR	Current	A	Corner for reverse-beta high-current roll-off	`+ IKR = 0.8167`
VAR	Current	V	Reverse early voltage	`+ VAR = 16.61`
RB	Resistance	Ω	Zero-bias base resistance	`+ RB = 150`
IRB	Resistance	A	Current where base resistance falls halfway to its minimum	`+ IRB = 0.0008356`
RBM	Resistance	Ω	Minimum base resistance at high currents	`+ RBM = 0.8289`
RE	Resistance	Ω	Emitter resistance	`+ RE = 0.804`
RC	Resistance	Ω	Collector resistance	`+ RC = 0.2454`
XTB		n.a.	Forward- and reverse-beta temperature exponent	`+ XTB = 1.382`
EG		eV	Energy gap for temperature effect of IS	`+ EG = 1.11`
XTI		n.a.	Temperature exponent for effect of IS	
CJE	Capacitance	F	B–E zero-bias depletion capacitance	
VJE	Capacitance	V	B–E built-in potential	`+ VJE = 0.7056`
MJE	Capacitance	n.a.	B–E junction exponential factor	`+ MJE = 0.3401`
TF	Capacitance	s	Ideal forward transit time	`+ TF = 6.258E-10`
XTF	Capacitance	n.a.	Coefficient for bias dependence of TF	`+ XTF = 25`
VTF	Capacitance	V	Voltage describing V_{BC} dependence of TF	`+ VTF = 2`
ITF	Capacitance	A	High-current parameter for effect on TF	`+ ITF = 0.277`
PTF		°	Excess phase at frequency = 1/(2π TF)	`+ PTF = 0`
CJC	Capacitance	F	B–C zero-bias depletion capacitance	`+ CJC = 3.624E-12`

Name	Property	Unit	Parameter	Code example
VJC	Capacitance	V	B–C built-in potential	+ VJC = 0.5036
MJC	Capacitance	n.a.	B–C junction exponential factor	+ MJC = 0.365
XCJC	Capacitance	n.a.	Fraction of B–C depletion capacitance connected to internal base node	+ XCJC = 1
TR	Capacitance	s	Ideal reverse transit time	+ TR = 1.55E-07
CJS	Capacitance	F	Zero-bias collector–substrate capacitance	+ CJS = 0
VJS	Capacitance	V	Substrate–junction built-in potential	+ VJS = 0.75
MJS	Capacitance	n.a.	Substrate–junction exponential factor	+ MJS = 0.333
FC		n.a.	Coefficient for forward-bias depletion capacitance formula	+ FC = 0.78
TNOM	Temperature	°C	Parameter measurement temperature	+ TNOM = 0.78
NE	Current	n.a.	B–E leakage emission coefficient	+ NE = tbd
KF		n.a.	Flicker-noise coefficient	+ KF = tbd
AF		n.a.	Flicker-noise exponent	+ AF = tbd

Case study and examples

This case study illustrates an LTspice-based simulation for characterizing a BJT circuit in a common base (CB) configuration. In a CB configuration, the base terminal serves as a common terminal for both input and output. It's particularly known for its unique feature of maintaining an almost constant voltage gain.

To simulate CB configuration in LTspice:

Circuit setup: Begin by selecting a BJT from the LTspice component library. Connect the emitter to an AC input source and ground the base. The collector will serve as the output node. Add necessary biasing components, such as resistors and a DC supply, to ensure the transistor operates in its active region.

AC analysis: With the circuit in place, perform an AC analysis. This will yield the frequency response of the transistor in the CB configuration. The result provides insight into the bandwidth and gain of the circuit.

Transient analysis: This analysis will exhibit the time-domain response of the circuit. It's useful for understanding transient behaviors, particularly when the input signal varies.

DC sweep: By sweeping the DC biasing voltage and monitoring the collector current, you can gain insights into the BJT's operation across different regions (cutoff, active, saturation).

Results and interpretation: Post-simulation, LTspice provides detailed waveforms that show the behavior of the BJT in the common base configuration. The software also offers a variety of tools to measure specific parameters such as peak values, RMS values and frequency components.

In Figure 2 a simple SPICE base circuit example is shown. The input voltage V_{IN} varies in the range from −2 V to +0.2 V. In Figure 3 the result of the simulation is depicted. The voltage traces for the base voltage V_B (dark blue trace) and the output voltage V_{OUT} (red trace) are shown as a function of V_{IN}.

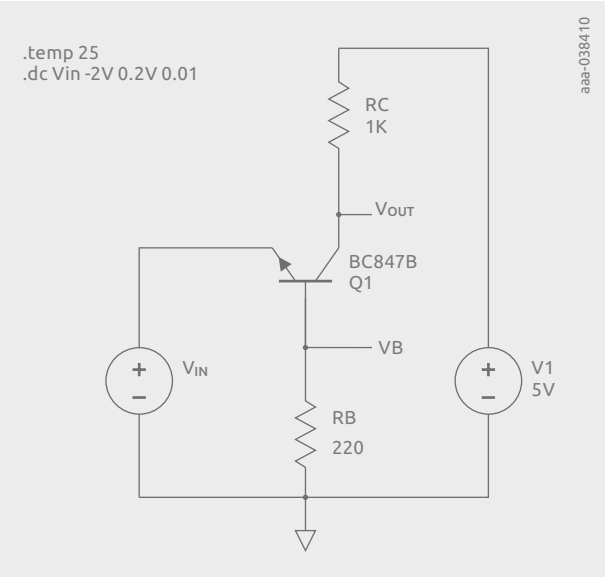


Figure 2 | Simulation in LTSpice: common base configuration circuit

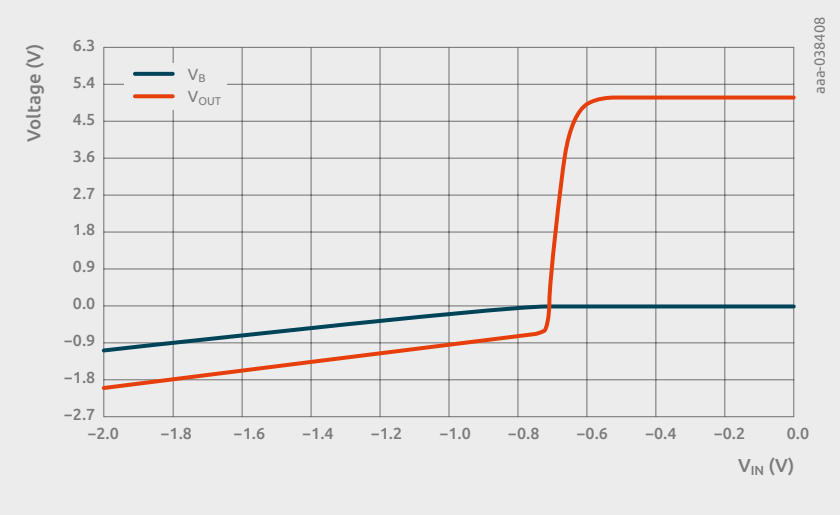


Figure 3 | Simulation results for the base voltage V_B and the output voltage V_{OUT} versus the input voltage V_{IN}

System-based simulations

System-based models are designed to simulate electrical circuits within the broader context of systems and controls. They excel in the modeling of power electronic systems, providing a piecewise linear approximation approach for efficient simulations. This type of simulation model integrates seamlessly with programs like MATLAB/Simulink®, allowing for co-simulation of control algorithms and electrical circuits. This integration is a significant advantage for engineers working on control systems, enabling a holistic approach to system design and analysis used for efficiency testing and loss splits based on conduction and switching losses. While system models may not offer the same level of detailed component models as SPICE, their strength lies in their ability to handle system-level simulations with greater efficiency and speed, and allow dynamic and static analysis for a huge number of switching cycles. Furthermore, they can be incorporated with either data generated from compact models based on SPICE or by the use of digitized data sheets. Popular examples of system simulation platforms are PLECS, PSIM and GeckoCIRCUITS.

Chapter 9

Summary

Invented by William Shockley in 1948, the bipolar junction transistor (BJT) was an innovation which revolutionized the art of linear electronics and completely transformed the field of digital computing. As an ideal replacement for clunky and unreliable vacuum tubes, the BJT enabled the miniaturization of machines and equipment that previously occupied huge volumes of space and consumed vast quantities of power such that only large corporations and academic institutions could afford to own and run them. This allowed them to become more widely available to smaller businesses and eventually also to consumers.

Nexperia has a rich tradition in developing and manufacturing silicon BJTs and through this handbook it has endeavored to capture some of this expertise so that student and professional engineers alike can benefit from its accumulated knowledge and use it to good effect in their applications.

Chapter 1 addressed the fundamentals of BJTs, describing device structures, physical principles of operation and providing an overview of the main process steps in device fabrication. Chapter 2 reviewed various types of BJTs including general-purpose, high-power and matched-pairs, and discussed the features of resistor-equipped transistors (RETs) and their benefits in switching applications before finally considering different types of LED drivers. How to interpret data sheet parameters of BJTs was explained in Chapter 3 before device behavior from a thermal perspective was explored in Chapter 4. Nexperia's diverse range of SMD package options for BJTs – ranging from the legacy SOT23 package to the most modern packages in the industry – were presented in Chapter 5 before important quality and reliability considerations for circuit designers using these devices were covered in Chapter 6. A broad range of BJT application circuits was examined in Chapter 7, including various amplifier topologies, current sensing, voltage regulation and power as well as audio, discrete digital gate circuits and signal generation applications. Finally, modelling and software simulation of BJT devices were examined in Chapter 9.

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Abbreviations

AC	Autoclave
BJT	Bipolar Junction Transistor
β	current gain
C_C	Collector capacitance
C_{CB}	Capacitance from Collector to Base
C_{CE}	Capacitance from Collector to Emitter
C_{EB}	Capacitance from Emitter to Base
CFP	Clip-bonded Flat Power package
δ	duty cycle, t_{period}/t_{on}
EFR	Early Failure Rate
E_F	Fermi Level, energy level
E_C	Energy of the bottom of the conduction band
E_V	Energy of the top of the valence band
η	ideality factor (Greek Eta)
f_T	transition frequency
h_{FE}	DC current gain (I_C/I_B)
HAST	Highly accelerated Stress Test
H3TRB	High Humidity/High Temperature Reverse Bias
I_B	Base Current
I_C	Collector Current
I_{CBO}	Collector-Base cut-off or leakage current, emitter open
I_{CES}	Collector-Emitter cut-off or leakage current, base open
I_{CM}	peak collector current, Maximum Collector current for a defined pulse
I_E	Emitter Current
I_{EBO}	Emitter-Base cut-off or leakage current, collector open
IFR	Intrinsic Failure Rate
IOL	Intermittent operational life
IS	reverse saturation current of the base-emitter diode (~ 10^{-15} A to 10^{-12} A)
k	Boltzmann Constant 1.380649×10^{-16} Vas/K
LED	Light-Emitting Diode
LDO	Low Drop Out (voltage regulator)
L_P	diffusion length
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
μ	Mobility m²/Vs constant
NPN	BJT structure, base is anode of the 2 BJT pn diodes, complementary to PNP
N_A	Acceptor ion concentration
N_D	Donator ion concentration
P_{tot}	total Power dissipation
PNP	BJT structure, base is cathode of the 2 BJT pn diodes, complementary to NPN

q	elementary charge 1.602×10^{-19} As
Q_G	total gate charge (MOSFET)
RET	Resistor Equipped Transistor
RF	Radio Frequency
$R_{th}(j-a)$	Thermal resistance from junction to ambient
$R_{th}(j-c)$	Thermal resistance from junction to case
$R_{th}(j-mb)$	Thermal resistance from junction to mounting base
$R_{th}(j-sp)$	Thermal resistance from junction to solder point
S	Steepness of a BJT, $S = \Delta I_C/\Delta V_{BE}$
SWF	Side Wettable Flanks (for the contacts of a leadless package)
SPICE	Simulation Program with Integrated Circuit Emphasis (Ltspice, Ngspice, Pspice, Qspice,..)
T_J	Junction Temperature
T_{amb}	Ambient Temperature
T_{stg}	Storage Temperature
t_d	(switching) delay time
t_f	fall time
t_{on}	on-time
t_{off}	off-time
t_p	pulse length
t_r	rise time
t_s	storage time
TC	Temperature Cycling
TS	Temperature Shock
τ_t	transit time
τ_p	carrier lieftime
UHAST	Highly accelerated Stress Test
VA	Early Voltage
VBEon	Base-Emitter turn-on Voltage
V_{BEsat}	Base-Emitter saturation Voltage
V_{CBO}	Collector-Base breakdown Voltage with Open emitter
V_{CEO}	Collector-Emitter breakdown Voltage with Open base
V_{CES}	Collector-Emitter breakdown Voltage with base Shorted to the emitter
V_{CEsat}	Collector-Emitter saturation Voltage
V_{CER}	Collector-Emitter breakdown Voltage with a resistor applied from base to emitter
V_{EBO}	Emitter-Base breakdown Voltage with Open collector
V_T	Thermal voltage, ~ 26mV at room temperature
v	velocity
W_{eff}	effective width of the base
$Z_{th(j-amb)}$	Transient thermal impedance from junction to ambient
$Z_{th(j-sp)}$	Transient thermal impedance from junction to solder point

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