Reliability qualification information

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| **Stress** | **Conditions** | **Duration** | **Quantity** | **Rejects** |
| StressPre and Post stress electrical test | Tamb = 25°C | N/A | All parts | See below |
| PCPreconditioning | JESD22-A113Bake Tamb = 125°CSoak Tamb = 85°C, RH = 85%reflow | 24 hours168 hours3 cycles | 924 | 0 |
| HTRBHigh temperature reverse bias | MIL-STD-750-1Tj = Tj max, VDS = 80% of ratedVoltage M1039 Method A | 1000 hours | 231 | 0 |
| HTGBHigh temperature gate bias | JESD22-A108Tj = Tj max, VGS = 20V(SL), 16V (LL) | 1000 hours | 231 | 0 |
| TCTemperature Cycling | JESD22-A104-55°C to 150°C | 500 cycles | 231 | 0 |
| UHASTUnbiased highly accelerated stress test | JESD22-A118Tamb = 130°C, RH = 85%Pressure = +2.27atm | 96 hours | 231 | 0 |
| HAST\*Highly accelerated stress test | JESD22-A110Tamb = 130°C, RH = 85%VDS = 80% of rated voltage | 96 hours | 231 | 0 |
| H3TRB\*Temperature Humidity bias | JESD22-A101Tamb = 85°C, RH = 85%VDS = 80% of rated voltage | 1000 hours |
| IOLIntermittent operating life | MIL-STD-750 method 1037ΔTj = 80°C | 5000 cycles | 231 | 0 |
| RSHResistance to solder heat | JESD22-A111 (SMD)260°C ± 5°C | 10s | 30 | 0 |
| SDSolderability | IPC/ECA J-STD-002Method A dip and lookNo aging, solder Ta = 245°C | 3 sec dip | 66 | 0 |
| IPC/ECA J-STD-002Method B dip and lookNo agingSolder Ta = 245°C>95% lead coverage requiredSteam Aging: condition CSteam Ta = 93°C, 8 hoursSolder Ta = 245°C, 3 sec dip | 8 hours3 sec dip | 66 | 0 |
| Dry Bake:Ta = 150°CSolder Ta = 245°C>95% lead coverage required | 16 hours3 sec dip | 66 | 0 |

\*Either HAST or HT3RB are tested for a set of devices.

Calculation of FIT and MTBF

Test considered for FIT calculation: High Temperature Reverse Bias (HTRB) and High temperature Gate Bias (HTGB). Confidence level 60%, derated to 55°C, activation energy 0.7Ev test time 168 to 1000 hours.

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| **Technology** | **Quantity** | **Failure rate** | **MTBF** |
|  | 462 | 2.6 | 3.83E+8 |