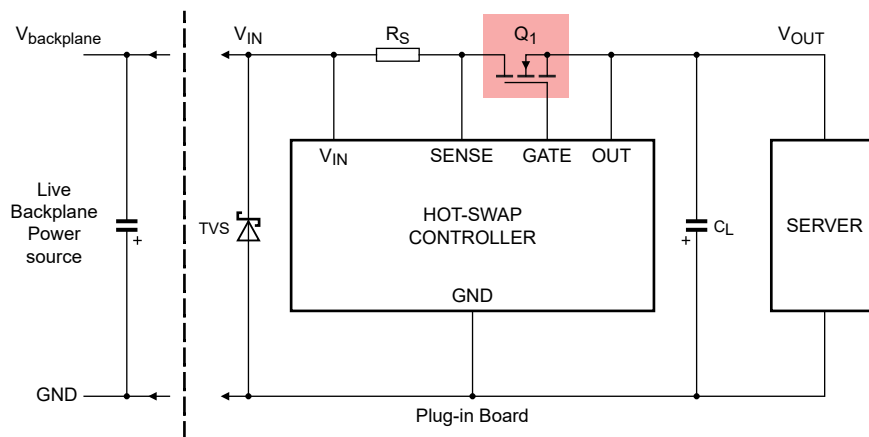


## How to pick a hot-swap MOSFET



**Abstract:** A comprehensive guide on how to select MOSFETs for server applications and how to evaluate their suitability for hot-swap operation. The document provides detailed examples for calculating electrical and thermal parameters, using a practical case study featuring a Nexperia 100 V application-specific MOSFET (ASFET): the hot-swap-optimized PSMN2R3-100SSE in LFPAK88 package.

**Keywords:** Server, AI Datacenter, MOSFET, MOSFET selection, hot-swap application, MOSFET parameters, calculation, paralleling technology, Safe Operating Area (SOA), FAQs.

## 1. Hot-swap Application overview

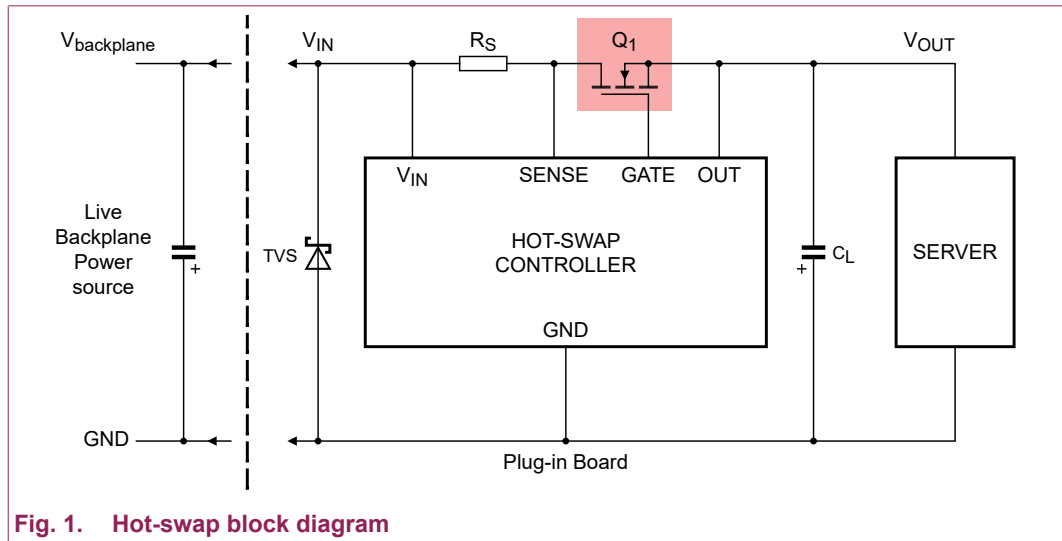


Fig. 1. Hot-swap block diagram

Hot-swap circuits are found in applications where a subsystem can be removed without disturbing or powering down the rest of the system. In the case of computing and data management, such as AI servers; individual trays of GPUs, CPUs, or network switches cannot disturb the rest of the server rack within the data center. This makes AI servers an excellent candidate for hot-swap circuits.

As a result, hot-swap circuits require in-rush current control, fault protection, and controlled turn on-and turn-off functions as they pass power from a centralized source (i.e. 48 V busbar) to a subsystem (i.e. individual server trays). The MOSFET pass element (Q1 in Fig. 1) and controller IC (Hot-swap Controller in Fig. 1) are separated because of high power requirements. As a result, certain MOSFET parameters must be considered.

Maximum drain-to-source voltage ( $V_{DSmax}$ ), drain-to-source on-state resistance ( $R_{DSon}$ ), packaging, paralleling technology, and Safe Operating Area (SOA) will be discussed in detail to simplify the MOSFET selection process. In addition, this will explain why Nexperia's enhanced SOA [hot-swap MOSFETs](#), such as the [PSMN2R3-100SSE](#), excel in the market.

## 2. MOSFET Parameters for Standard Operation

### 2.1. Input voltage ( $V_{IN\_typ}$ ) vs. maximum breakdown voltage ( $V_{DSmax}$ )

For newer and modern data center architectures, the busbar voltage, or input voltage ( $V_{IN\_typ}$ ) to an individual server tray, is within a range of 40 V – 60 V. The typical value of the input voltage will either be 48 V, 50 V, or 54 V. However, transient voltage surges or spikes, in combination with system parasitics (i.e. busbar and wires from the rack to the power distribution board), will induce voltage much higher than the typical range and destroy the MOSFET if the maximum breakdown voltage ( $V_{DSmax}$ ) is exceeded.

As a result, most designers have determined that  $V_{DSmax}$  is 100 V for 54 V systems. More information can be found in the [Calculating  \$V\_{DSmax}\$  of a MOSFET](#) section.

Because  $V_{DSmax}$  determines packaging,  $R_{DSon}$  range, and ultimately price of the MOSFET, it is important to pick the  $V_{DSmax}$  first. In any case, Nexperia offers enhanced SOA hot-swap MOSFETs with  $V_{DSmax}$  at both 80 V and 100 V, such as the [PSMN2R3-100SSE](#).

## 2.2. Input Power and Current vs. MOSFET Power Dissipation ( $R_{DSon}$ )

Input power ( $P_{IN\_typ}$ ) is the wattage requirement determined by the circuits within a subsystem. In the case of server trays, GPUs and CPUs will determine most of the power, which ranges from 1.2 kW – 2.2 kW in current architectures and 2 kW – 4 kW in near-future architectures.

[Equation 1](#) determines the typical input current ( $I_{IN}$ ):

$$I_{IN} = \frac{P_{IN\_typ}}{V_{IN\_typ}} \quad (\text{Equation 1})$$

$$I_{IN} = \frac{(4 \text{ kW})}{(54 \text{ V})}$$

$$I_{IN} = 74 \text{ A}$$

Where:

- $I_{IN}$  is the input current seen by the system [A]
- $P_{IN\_typ}$  is the typical input power seen by the system [W]
- $V_{IN\_typ}$  is the typical input voltage seen by the system [V]

[Equation 1](#) yields a range of 22 A – 74 A, which are typical input currents in modern server architectures. This ultimately leads to power dissipation ( $P_D$ ) in the MOSFET, which is the limiting factor in most MOSFET circuits.

While the maximum junction (or die) temperature rating of Nexperia hot-swap MOSFETs is 175 °C, most designers will have a target junction temperature ( $T_{J\_target}$ ) and other system requirements that they must adhere to.

Typical target junction temperatures can range from 100 °C – 125 °C to allow for transient events, and ambient temperatures can range from 50 °C – 85 °C depending on cooling paths within the server tray. Thermal resistance ( $R_{thJA}$ ) is determined by the MOSFET package and layout, which is discussed in more detail in [MOSFET Packages and Paralleling with Application Specific \(ASFET\) technology](#) section, but an 8x8 mm MOSFET with good layout is used for this example.

In combination with the calculated input current (74 A), 0.328 mΩ is calculated in the [Calculating target  \$R\_{DSon}\$  of a singular MOSFET](#) section. However, there are no 0.328 mΩ MOSFETs available on the market. As a result, designers will place several MOSFETs in parallel to achieve higher current capability.

### 2.2.1. MOSFET Packages and Paralleling with ASFET technology

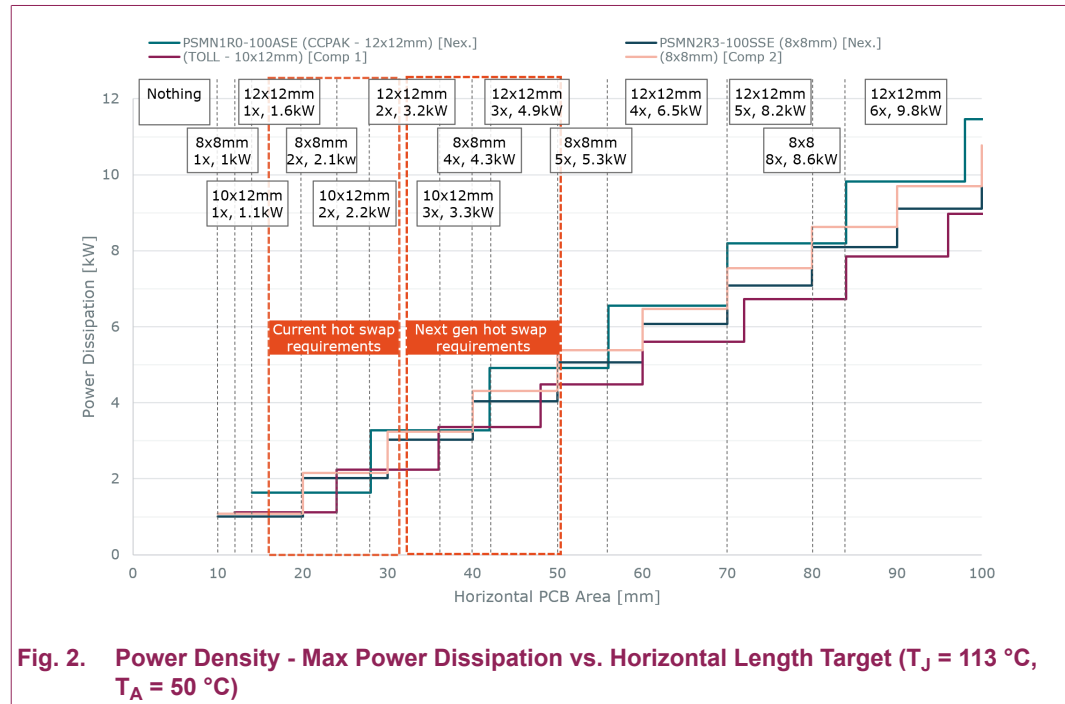


Fig. 2 shows a graph of popular hot-swap MOSFET's, including PSMN2R3-100SSE, maximum server tray power vs. horizontal PCB area. This determines how many MOSFETs in parallel are needed for a system's target power.

To achieve the target input current of 74 A (or 4 kW), Fig. 2 indicates that several parallel MOSFETs (e.g. 4) can be used. This is determined by Equation 2:

$$R_{DSon_{max@temp}} = \frac{T_{J\_target} - T_{amb}}{\left(\frac{I_{IN}}{n_{parallel}}\right) \cdot R_{thJA}} \quad (\text{Equation 2})$$

$$R_{DSon_{max@temp}} = \frac{(113\text{ }^\circ\text{C}) - (50\text{ }^\circ\text{C})}{\left(\frac{(74\text{ A})}{(4)}\right)^2 \cdot (35\text{ }^\circ\text{C/W})}$$

$$R_{DSon_{max@temp}} = 5.259\text{ m}\Omega$$

Where:

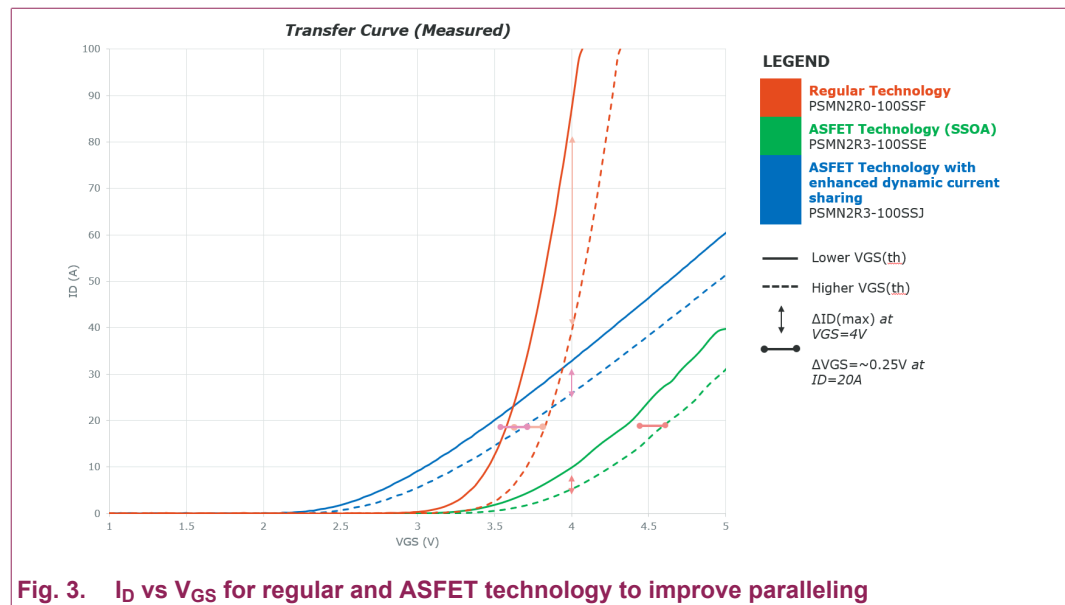
- $T_{J\_target}$  is the target junction or die temperature [ $^\circ\text{C}$ ]
- $R_{thJA}$  is the thermal resistance from junction to ambient, which usually consists of PCB and MOSFET package thermal resistance [ $^\circ\text{C/W}$  or  $\text{K/W}$ ]
- $T_{amb}$  is ambient temperature of the system [ $^\circ\text{C}$ ]
- $I_{IN}$  is the input current seen by the system [A]
- $R_{DSon@temp}$  is the maximum  $R_{DSon}$  adjusted from  $25\text{ }^\circ\text{C}$  to the target temperature using the data sheet [ $\Omega$ ]
- $n_{parallel}$  is the number of MOSFETs in parallel

As discussed in “[LPAK MOSFET thermal design guide](#)” application note, package construction and dimensions play a large role in determining thermal impedance or thermal capability of a MOSFET. Both the PSMN2R3-100SSE (LPAK88, SOT1235, 8x8mm) and PSMN1R0-100ASE (CCPAK, SOT8000A, 12x12mm), benefit from copper clip technology for the best thermal performance, as opposed to bond wires used in TOLL (e.g. PG-HSOF-8-1, 10x12mm). This performance improvement will be reflected in a MOSFET’s Safe Operating Area (SOA) graph, and thermal package impedance graph located in the data sheet.

While packaging is important, PCB layout is a main contributor to the thermal path (i.e. 0.44 °C/W for the thermal impedance of package vs. approximately 35 °C/W for the thermal impedance of the PCB). Ideal and realistic PCB thermal resistances ( $R_{thJA}$ ), such as 35 °C/W for LPAK88, can be found in the “[Thermal boundary condition study on MOSFET packages and PCB substrates](#)” application note.

The PSMN2R3-100SSE’s maximum  $R_{DSon}$  at 175 °C is 5.2 mΩ, which is a great choice for this application requirement of 5.259 mΩ calculated by [Equation 2](#). This difference adds margin when comparing the actual junction temperature to the target.

Note that [Fig. 2](#) shows that the PSMN1R0-100ASE has the best power density (i.e. largest slope) out of any device in the market. The PSMN1R0-100ASE is a 1 mΩ, 12x12 mm, Enhanced SOA MOSFET using the CCPAK package. This device has a clear advantage and gives the best performance, or most margin, at higher power (i.e. >5 kW designs under the same assumptions).



**Fig. 3.**  $I_D$  vs  $V_{GS}$  for regular and ASFET technology to improve paralleling

As discussed in “[Paralleling power MOSFETs in high power applications](#)” application note, mismatch in gate-source threshold voltage ( $V_{GS(th)}$ ), sometimes called the MOSFET “on” voltage, will lead to uneven current sharing between MOSFETs that would result in higher input current ( $I_{IN}$ ) for a singular MOSFET as shown in [Fig. 4](#).

[Fig. 3](#) shows 3 types of MOSFET technology: Regular technology (PSMN2R0-100SSF), Application Specific MOSFET (ASFET) technology with enhanced SOA (PSMN2R3-100SSE), and ASFET technology with enhanced current sharing (PSMN2R3-100SSJ). Choosing enhanced SOA ASFET family will result in 2 to 4 times better current sharing for worst case  $V_{GS(th)}$  separation compared to Regular technology. This is also demonstrated in the waveforms shown in [Fig. 4](#).

As a result, choosing a MOSFET in the enhanced SOA ASFET family, such as PSMN2R3-100SSE, will benefit from the enhanced current sharing.

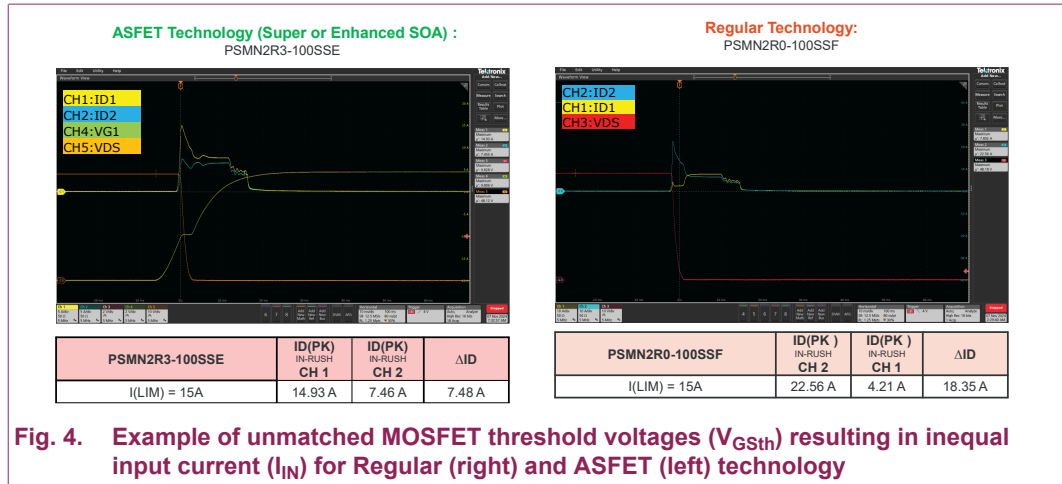


Fig. 4. Example of unmatched MOSFET threshold voltages ( $V_{GStH}$ ) resulting in unequal input current ( $I_{IN}$ ) for Regular (right) and ASFET (left) technology

### 3. MOSFET Parameters during Hot-swap operation

#### 3.1. Hot-swap Operation

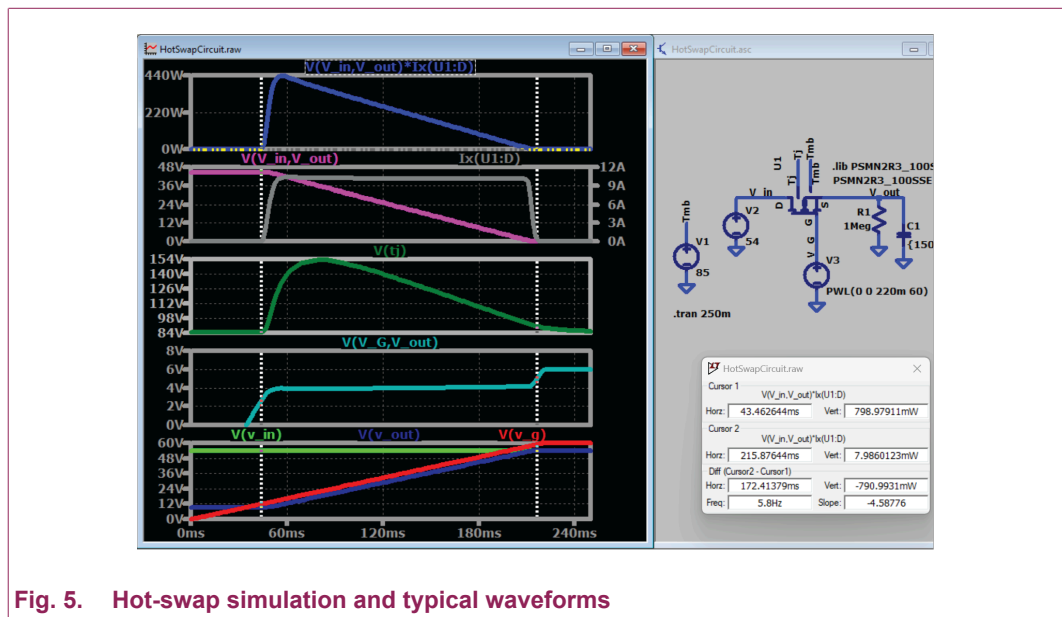


Fig. 5. Hot-swap simulation and typical waveforms

As seen in Fig. 5, typical hot-swap controllers will linearly and constantly charge the gate of the MOSFET to facilitate a controlled turn-on. This operation puts the MOSFET into current source mode, sometimes called linear mode, which constantly charges the bulk capacitance ( $V_{out}$ ). The MOSFET current source mode is extensively discussed in the [“Power MOSFETs in linear mode”](#) application note, and one of the most stressful modes a MOSFET can operate in.

As a result, there are 4 important aspects for linear mode operation:

1. Voltage at the input to be transferred to the output ( $V_{IN}$  or  $V_D$ )
2. In-rush current needed to charge the bulk capacitance ( $I_{inRush}$ )
3. The amount of time taken to charge the bulk capacitance ( $t_{pulse}$ )
4. Pulse Shapes of current and voltage or energy (triangular or rectangular)

Input voltage ( $V_{IN}$ ) is the same as the system’s input voltage, so 54 V is used.

The  $V_{DS}$  voltage pulse shape is triangular, and the current pulse is rectangular, which results in a triangular power pulse shape as shown in [Fig. 5](#). This effectively doubles the SOA performance of the MOSFET as discussed in “[Power MOSFETs in linear mode](#)” application note.

The amount of time ( $t_{pulse}$ ) and the in-rush current ( $I_{inRush}$ ) depend on bulk capacitance, the input voltage ( $V_{IN}$ ), the hot-swap controller’s gate voltage slew rate or source current, and fault conditions. For most hot-swap server applications, this time is between 800  $\mu s$  – 500 ms. In modern architecture, 10 ms or 100 ms are the typical benchmarks.

Ultimately, these values are compared against the MOSFET’s Safe Operating Area (SOA) graph in the data sheet, as shown in the [Safe Operating Area \(SOA\) of a MOSFET and ASFET technology](#) section.

Due to the complex interaction between MOSFET, Hot-swap Controller, and bulk capacitance; simulation is the recommended way to establish a baseline before the prototyping phase. Refer to [Fig. 5](#) and “[Nexperia Precision Electrothermal models in SPICE and VHDL-AMS for Power MOSFETs](#)” application note. Otherwise, the [Imprecise calculation of hot-swap pulse time](#) section will help for generic calculations.

### 3.1.1. Safe Operating Area (SOA) of a MOSFET and ASFET technology

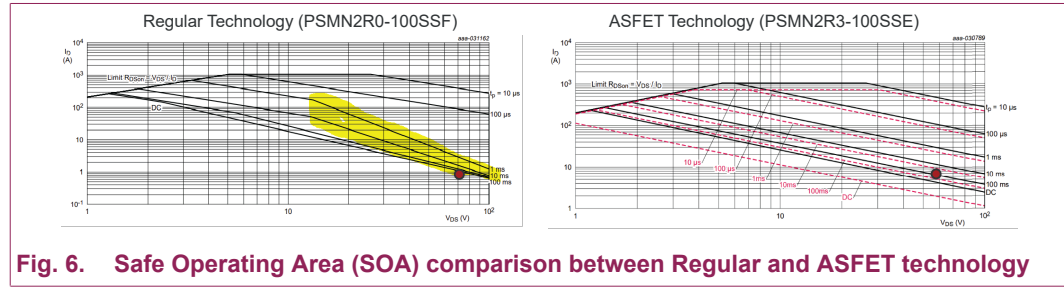


Fig. 6. Safe Operating Area (SOA) comparison between Regular and ASFET technology

Safe Operating Area (SOA), as shown in Fig. 6, illustrates the range of voltage, current, and pulse length where operating below the lines will indicate safe operation.

For power MOSFETs in linear mode there is a significant reduction in performance, which can be reviewed in the Definition of Safe Operating Area (SOA) regions and Spirito effect section. This phenomenon is known as the Spirito effect, and MOSFETs with Enhanced SOA ASFET technology eliminate the Spirito effect which increases SOA performance and margin as shown in Fig. 6.

Comparing the example in Fig. 6 where  $V_{IN}$  is 54 V, the pulse shape is triangular,  $t_{pulse}$  is 100 ms, and the MOSFET is the PSMN2R3-100SSE; the SOA current results in 14 A (or 2 multiplied by 7) at  $T_J = 25^\circ\text{C}$  for, which is approximately 4 times better performance compared to the PSMN2R0-100SSF, non-enhanced SOA MOSFET (3.5 A or 2 multiplied 1.75).

As shown in the Imprecise calculation of hot-swap pulse time section example, the regulated in-rush current is around 8 A and 54 V, for 120 mF and approximately 100ms, which is below the 14 A limit at 100 ms for the PSMN2R3-100SSE.

Recalculating SOA performance for different  $t_{pulses}$ , shapes, and temperatures is discussed in “Power MOSFETs in linear mode” application note and Example of re-rating SOA graph for temperature section.

### 3.2. Fault conditions such as Start up into Short Circuit

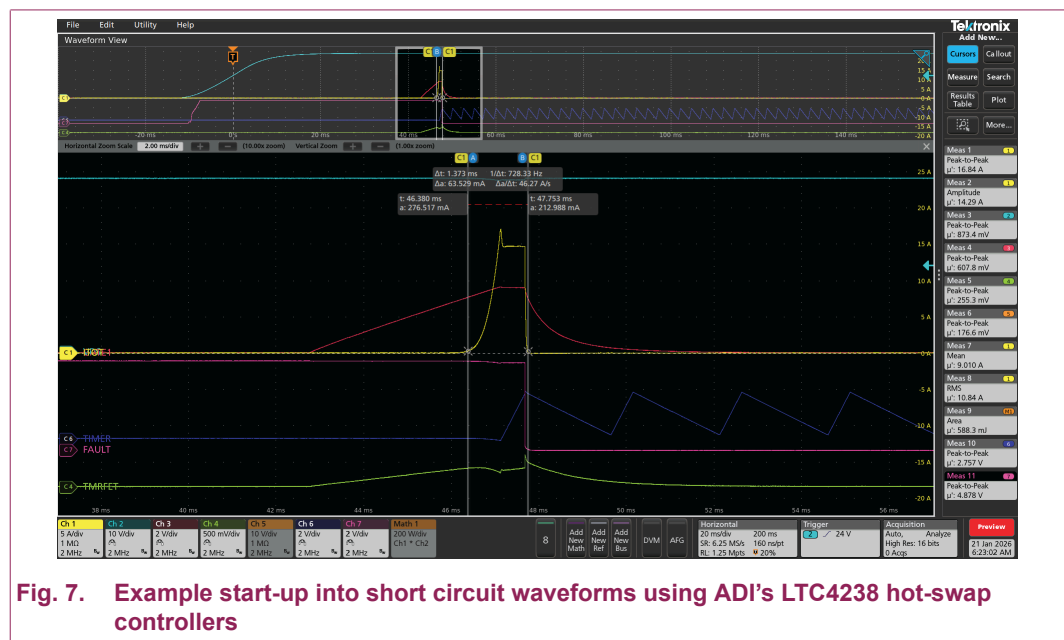


Fig. 7. Example start-up into short circuit waveforms using ADI's LTC4238 hot-swap controllers

There are many fault conditions that can occur to a MOSFET in a hot-swap application. The most demanding fault is start-up into short circuit as shown in Fig. 7.

Start-up into short circuit shows that the  $V_{DS}$  and current are both large which result in a larger instantaneous power compared to a running short-circuit, where  $V_{DS}$  is small but current is large. This is shown on the right side of Fig. 8. In some cases, this energy is more than the energy seen during a normal hot-swap operation to charge the bulk capacitors.

As a result, it is important to compare the  $V_{IN}$ ,  $I_{inRush}$ ,  $t_{pulse}$ , and shape during this fault condition to the SOA graph in data sheet.

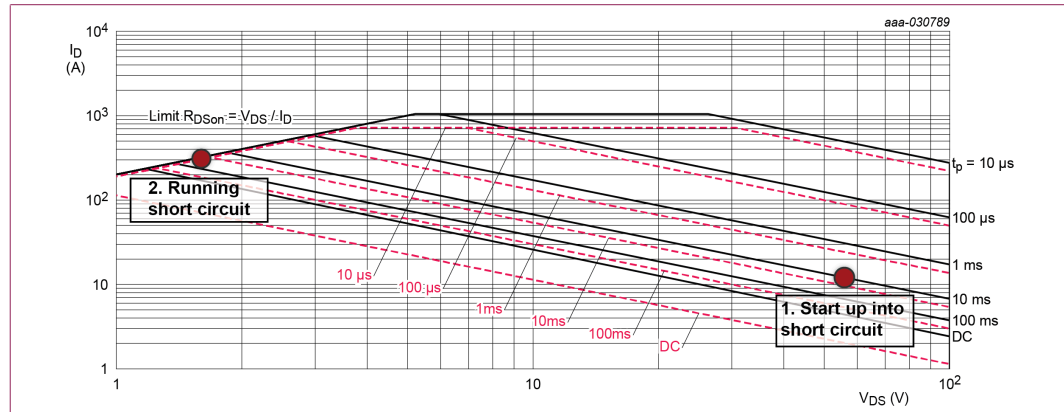


Fig. 8. Common hot-swap faults in context of Safe Operating Area (SOA)

### 3.2.1. The role of hot-swap controllers during fault conditions

Ultimately, the resulting waveform during a fault condition is the combination of parasitics in the system and the hot-swap controller’s reaction. If a MOSFET passes every use-case except a fault, changing the MOSFET might not be the solution or an option without a redesign.

Luckily, the best hot-swap controllers, such as Texas Instrument’s LM506x series and Analog Devices LTC42xx series, are configurable using software which can help reduce stress on the MOSFET without redesigning.

For example, the current is detected through the shunt resistor and the sensing pins of the hot-swap controller as shown in Fig. 1. Fault detection time and deglitch filters of the hot-swap controller will determine when the fault triggers, which should help determine worst case  $t_{pulse}$ . Both LM506x and LTC42xx can adjust or shorten these fault timers.

As a result, always consider the role of the hot-swap controller and how it can reduce energy exposed to the MOSFET.

## 4. Conclusion

Hot-swap circuits are found in AI server applications because of the relationship between the rack's busbar and the server tray. Hot-swap circuits require features, such as in-rush current control, fault protection, and controlled turn on and turn off that will stress the MOSFET. Key parameters such as maximum drain-to-source voltage ( $V_{DSmax}$ ), drain-to-source on-state resistance ( $R_{DSon}$ ), packaging, paralleling technology, and Safe Operating Area (SOA) must be considered in the MOSFET selection process. Notably, Nexperia's enhanced SOA [hot-swap ASFET MOSFETs](#), such as the [PSMN2R3-100SSE](#), are perfect for modern and near future server hot-swap designs.

### 4.1. References

1. Understanding power MOSFET data sheet parameters  
<https://assets.nexperia.com/documents/application-note/AN11158.pdf>
2. Paralleling power MOSFETs in high power application  
<https://assets.nexperia.com/documents/application-note/AN50005.pdf>
3. Power MOSFETs in linear mode  
<https://assets.nexperia.com/documents/application-note/AN50006.pdf>
4. Thermal boundary condition study on MOSFET packages and PCB substrates  
<https://assets.nexperia.com/documents/application-note/AN50019.pdf>
5. LFPK MOSFET thermal design guide  
<https://assets.nexperia.com/documents/application-note/AN90003.pdf>
6. Nexperia Precision Electrothermal models in SPICE and VHDL-AMS for Power MOSFETs  
<https://assets.nexperia.com/documents/application-note/AN90034.pdf>

## 5. Appendix

### 5.1. Frequently Asked Questions (FAQs)

#### 5.1.1. Calculating $V_{DSmax}$ of a MOSFET

The following [equations](#) for determining  $V_{DSmax}$  are for a typical input voltage.

$$V_{DSmax} = 2 \cdot V_{IN\_typ} \quad (\text{Equation 3})$$

$$V_{DSmax} = 2 \cdot (54 \text{ V})$$

$$V_{DSmax} = 108 \text{ V} \approx 100 \text{ V}$$

$$V_{DSmax} = \frac{3}{2} \cdot V_{IN\_typ} \quad (\text{Equation 4})$$

$$V_{DSmax} = \frac{3}{2} \cdot (54 \text{ V})$$

$$V_{DSmax} = 81 \text{ V} \approx 80 \text{ V}$$

Where:

- $V_{DSmax}$  is maximum drain to source blocking or withstand voltage of a MOSFET [V]
- $V_{IN\_typ}$  is the typical input voltage seen by the system [V]

Note, [Equation 4](#) to determine  $V_{DSmax}$  is reserved for regulated outputs (such as OR-ing circuits). The server rack busbar or back-plane is regarded as an unregulated output. As a result, modern data centers have shown that  $V_{DSmax} = 100 \text{ V}$  is preferred and provides enough margin.

### 5.1.2. Calculating target $R_{DSon}$ of a singular MOSFET

$$T_{J\_target} = P_D \cdot R_{thJA} + T_{amb} \quad (\text{Equation 5})$$

$$T_{J\_target} = (I_{IN}^2 \cdot R_{DSon@temp}) \cdot R_{thJA} + T_{amb}$$

$$R_{DSon@temp} = \frac{T_{J\_target} + T_{amb}}{(I_{IN}^2 \cdot R_{thJA})}$$

$$R_{DSon@temp} = \frac{(113 \text{ }^\circ\text{C}) + (50 \text{ }^\circ\text{C})}{((74 \text{ A})^2 \cdot (35 \text{ K/W}))}$$

$$R_{DSon@temp} = 0.328 \text{ m}\Omega$$

Where:

- $T_{J\_target}$  is the target junction or die temperature [ $^\circ\text{C}$ ]
- $P_D$  is power dissipation of the MOSFET [W]
- $R_{thJA}$  is the thermal resistance from junction to ambient, which usually consists of PCB and MOSFET package thermal resistance [ $^\circ\text{C/W}$  or  $\text{K/W}$ ]
- $T_{amb}$  is ambient temperature of the system [ $^\circ\text{C}$ ]
- $I_{IN}$  is the input current seen by the system [A]
- $R_{DSon@temp}$  is the maximum  $R_{DSon}$  at 25  $^\circ\text{C}$  value adjusted to the target temperature using the data sheet [ $\Omega$ ]

### 5.1.3. Imprecise calculation of hot-swap pulse time

The energy of total bulk or output capacitance will help determine the in-rush current pulse time applied to the MOSFET. Note, that this is not the same as  $P_{IN\_typ}$  as input power assumes the entire system's energy, which is more than the energy required by the output capacitance.

$$E_{C\_Load} = \frac{1}{2} C_{Load} \cdot V_{IN\_typ} \quad (\text{Equation 6})$$

Where:

- $E_{C\_Load}$  contained with output capacitance [J]
- $C_{Load}$  is the total of all output capacitance [F]
- $V_{IN\_typ}$  is the typical or average input voltage seen by the system [V]

Because of the relationship between energy and power, time is calculated assuming each MOSFET in parallel experiences the same power dissipation.

$$E_{C\_Load} = P_{D\_all} \cdot t_{pulse} \quad (\text{Equation 7})$$

$$t_{pulse} = \frac{E_{C\_Load}}{(n_{parallel} \cdot P_{D\_inrush})}$$

$$t_{pulse} = \frac{C_{LOAD} \cdot V_{IN\_typ}^2}{(2 \cdot n_{parallel} \cdot P_{D\_inrush})}$$

Where:

- $E_{C\_Load}$  contained with output capacitance [J]
- $P_{D\_all}$  is power dissipation of all MOSFETs in parallel [W]
- $P_{D\_inrush}$  is power dissipation of a singular MOSFET [W]
- $n_{parallel}$  is the number of MOSFETs in parallel
- $C_{Load}$  is the total of all output capacitance [F]
- $V_{IN\_typ}$  is the typical or average input voltage seen by the system [V]

Lastly, most hot-swap controllers used in these applications will have constant and configurable current limits detected through shunt-resistors ( $R_S$  in [Fig. 1](#)) and ADC inputs. This means the power dissipation of each MOSFET can be easily calculated if the exact in-rush current ( $I_{inRush}$ ) is not known. Otherwise,  $I_{inRush}$  can be used directly.

$$t_{pulse} = \frac{C_{Load} \cdot V_{IN\_typ}^2}{2 \cdot n_{parallel} \cdot (I_{InRush} \cdot V_{IN\_typ})} \quad (\text{Equation 8})$$

$$t_{pulse} = \frac{C_{Load} \cdot V_{IN\_typ}}{2 \cdot n_{parallel} \cdot (I_{InRush})}$$

$$t_{pulse} = \frac{C_{Load} \cdot V_{IN\_typ}}{2 \cdot n_{parallel} \cdot \left(\frac{V_{ADC\_limit}}{R_{sense}}\right)}$$

$$t_{pulse} = \frac{(120 \text{ mF}) \cdot (54 \text{ V})}{\left(2 \cdot (4) \cdot \left(\frac{(4 \text{ mV})}{(0.5 \text{ m}\Omega)}\right)\right)}$$

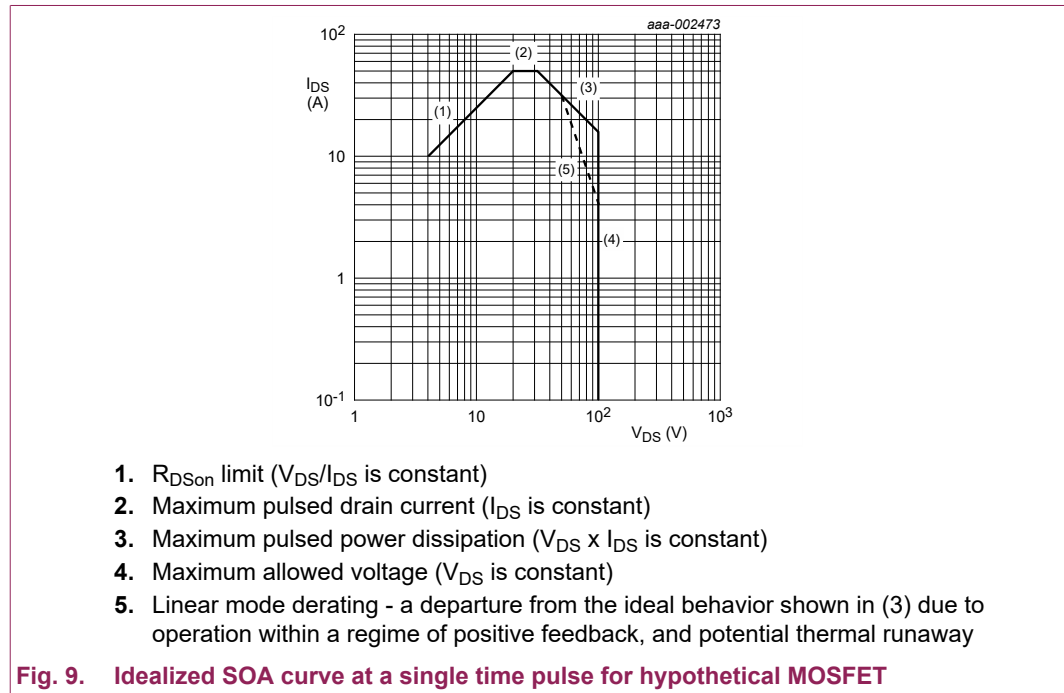
$$t_{pulse} = 101.25 \text{ ms} \approx 100 \text{ ms}$$

Where:

- $n_{parallel}$  is the number of MOSFETs in parallel
- $C_{Load}$  is the total output or system capacitance [F]
- $V_{IN\_typ}$  is the typical or average input voltage seen by the system [V]
- $V_{ADC\_limit}$  is the hot-swap controller's voltage limit sensed across the sense resistor [V]
- $R_{sense}$  is the shunt resistor used to sense current and voltage of the hot-swap circuit [ $\Omega$ ]
- $I_{InRush}$  = In-rush current per MOSFET needed to charge the bulk capacitance [A]

Note that the features of hot-swap controllers are varied and in-rush current is difficult to predict if not regulated. Combined with shunt resistor variance over temperature and the large tolerance of bulk capacitance, simulation is the recommended way to establish a baseline before the prototyping phase. This calculation is meant as a demonstration rather than a worked example.

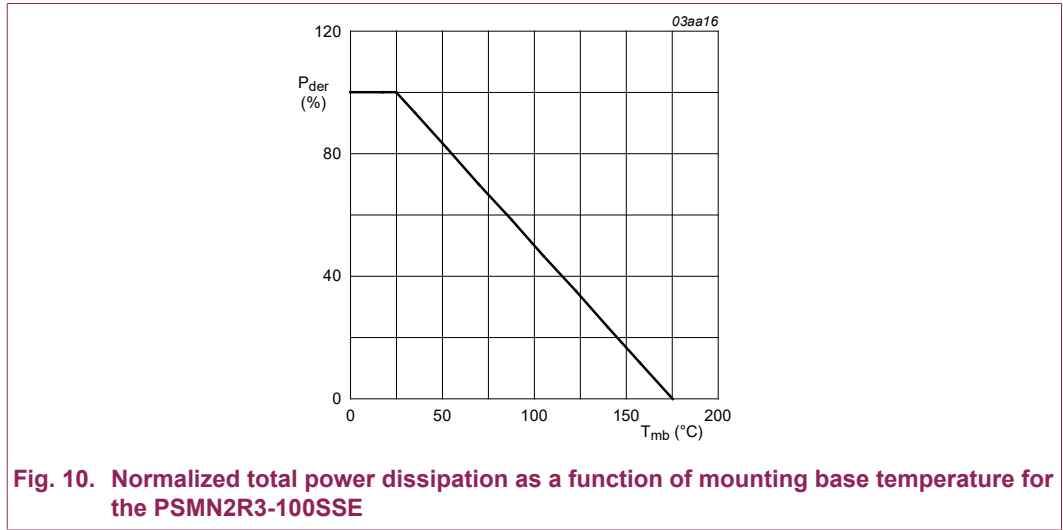
### 5.1.4. Definition of Safe Operating Area (SOA) regions and Spirito effect



Each area of the Safe Operating Area graph represents a specific stress, specification, or mode that the MOSFET operates in. As shown in Fig. 9,  $R_{DS(on)}$  maximum at temperature, maximum drain current, maximum power dissipation, and maximum  $V_{DS}$  are outlined. For example, the  $R_{DS(on)}$  limit (1. in Fig. 9) can be calculated by multiplying  $I_{DS}$  and  $V_{DS}$  along the line.

In the context of the [Safe Operating Area \(SOA\) of a MOSFET and ASFET technology](#) section, area 5 illustrates the derating when the device is in linear mode which is caused the Spirito effect. The Spirito effect is caused by the uneven distribution of current across the MOSFET die and discussed extensively in the "[Power MOSFETs in linear mode](#)" and "[Understanding power MOSFET data sheet parameters](#)" application notes.

5.1.5. Example of re-rating SOA graph for temperature



The re-rating of SOA for different temperatures is based on the normalized power dissipation versus temperature graph as shown in Fig. 10. In summary, this graph helps find a coefficient that is used to scale the specification relative to 25 °C.

Equation 9 illustrates a very similar technique to scale the current shown on the SOA graph.

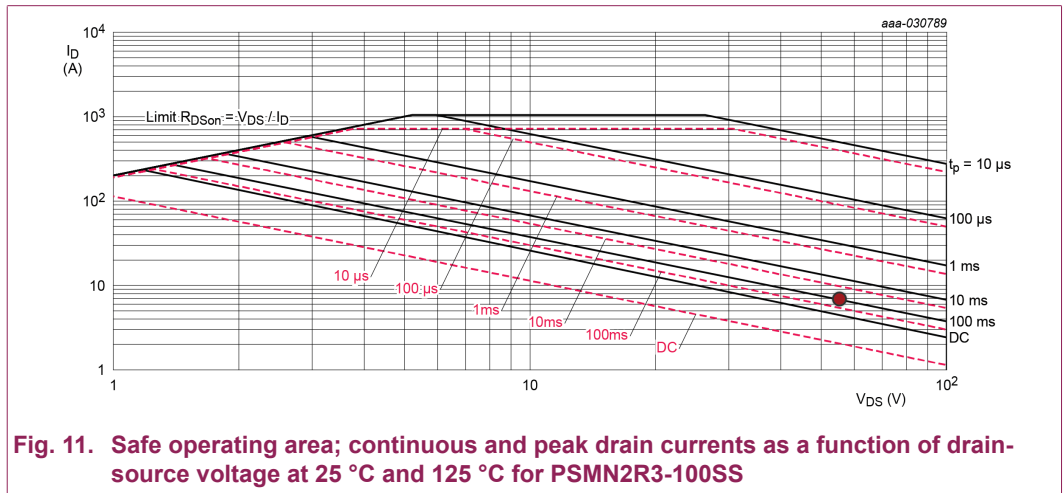


Fig. 11. Safe operating area; continuous and peak drain currents as a function of drain-source voltage at 25 °C and 125 °C for PSMN2R3-100SS

$$I_{D_{SOA}@temp} = \frac{I_{D_{SOA}@25^{\circ}C} (T_{Jmax} - T_{mb\_target})}{(T_{Jmax} - T_{mb@25^{\circ}C})} \quad \text{(Equation 9)}$$

$$I_{D_{SOA}@temp} = \frac{(7 A)((175^{\circ}C) - (110^{\circ}C))}{((175^{\circ}C) - (25^{\circ}C))}$$

$$I_{D_{SOA}@temp} = 3.03 A$$

Where:

- $I_{D\_SOA@temp}$  is the re-rated value of drain current on the SOA graph [A]
- $I_{D\_SOA@25C}$  is the actual value of drain current shown on the SOA graph [A]
- $T_{Jmax}$  is the maximum junction temperature for the MOSFET [C]
- $T_{mb\_Target}$  is the target mounting base temperature used to re-rate
- $T_{mb\_25C}$  is the nominal mounting base temperature of 25 °C

For example, [Equation 9](#) assumes that the SOA graph should be re-rated for  $T_{mb} = 110^{\circ}C$  when  $V_{DS}$  is 54 V, the  $t_{pulse}$  is 100 ms, and the shape of power dissipation is rectangular.

Note that MOSFETs with Enhanced SOA have measured  $I_{D\_SOA}$  values when  $T_{mb} = 125^{\circ}C$  as shown by the red line in [Fig. 11](#). Comparing the measured value at 125 °C (i.e. approximately 5.5 A) and the result of the re-rate calculation at 110 °C (i.e. 3.03 A) shows that this method over-compensates and does not match the measured values on the SOA graph.

## 6. Revision history

Table 1. Revision history

Revision number	Date	Description
1.0	2026-03-20	Initial release

## 7. Legal information

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