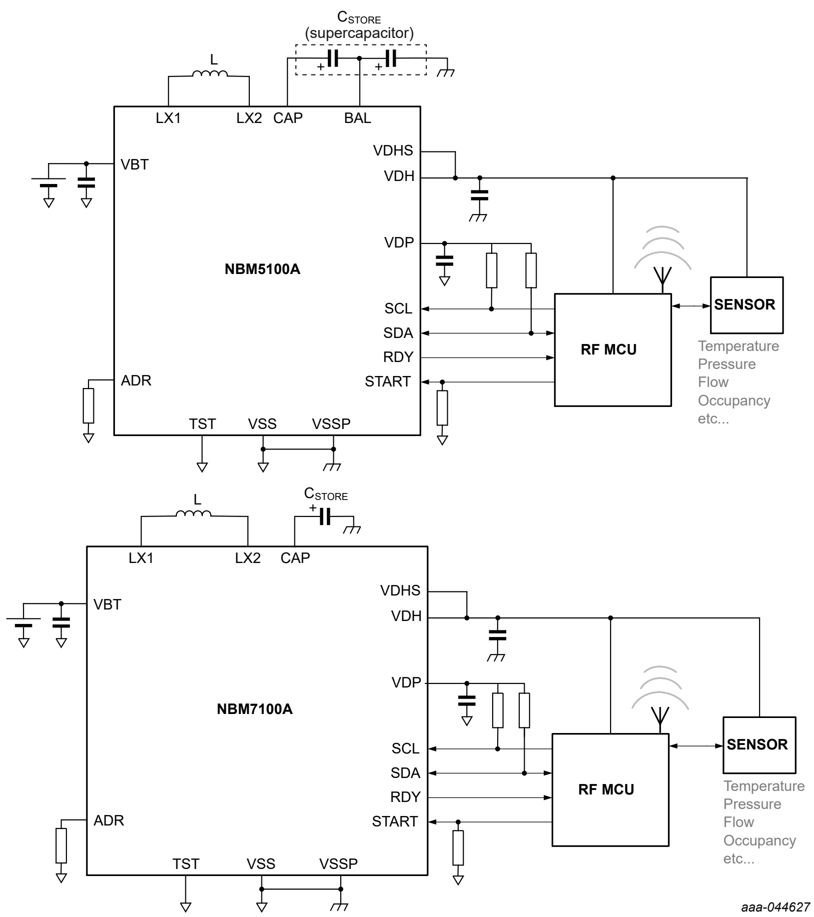
Most frequently asked questions about Nexperia NBM5100x/7100x



Abstract: This application note summarizes the most frequently asked questions from users in the field. The short answers are intended to further clarify the device features and help users in their efforts to implement the device.

Keywords: Battery management ICs, coin cell powered IoT devices

1. Introduction

The battery lifetime-booster NBM5100X/7100X (BB) is a state-of-the-art PMIC with a built-in digital power management system, monitoring and controlling coin-cell power conversion through an I2C/SPI serial communication interface.

This innovative design understandably attracts the attention of numerous wireless IoT users with applications ranging from wireless agricultural sensors to the state-of-the-art UWB key fobs and industrial IoT sensor nodes.

The following pages describe some of the questions collected from the field.

2. Questions and answers

Q1. Can the BB be used with other batteries than CR2032?

Yes, AA or AAA size alkaline batteries can be used with the BB. There is no difference in the BB performance, the battery lifetime extension is feasible and comparable with the performance when coin-cell batteries'performance are used.

Q2. What is the main difference between NBM7100 and NBM5100 apart from the different types of storage capacitors?

NBM5100 is designed to operate with supercapacitors. The maximum breakdown voltage of the supercapacitors is around 5 V, and that is why the max V_{FIX} for NBM5100 is 5.5 V. For more information, refer to *Table 38* in NBM5100x data sheet.

In order to store more energy with lower V_{FIX} and still have a reasonable size storage capacitor, the second stage of the DC-DC conversation in NBM5100 is a **buck/boost** converter. This means that we can have $V_{CSTORE} < V_{SET}$ and still maintain a constant V_{SET} constant in **boost** mode.

Q3. Can we use supercapacitors with NBM7100 if we use only one supercapacitor without the need for balancing?

Supercapacitors can be used with NBM7100 provided the V_{FIX} is **never** set higher than the max breakdown voltage of the supercapacitor. That also means that supercapacitors cannot be used with NBM7100 in auto mode as the default value for V_{FIX} is 9.9 V, which is much higher than the usual max supercapacitor breakdown voltage of 5.5 V.

Q4. How many modes of operation does the BB have and why?

Continuous mode (CM): for applications where we want C_{STORE} to stay charged continuously because we have frequent load pulses.

On-demand mode (OD): for applications with rare, infrequent load pulses or pulses with long idle time, when we wait for the load pulse to arrive and quickly charge C_{STORE} in advance. In OD we do not keep C_{STORE} charged continuously, we charge C_{STORE} only when it is needed, for the rest of the time the device is in sleep (standby) state.

Both CM and OD are intiated by serial I^2C bus commands.

Auto mode: this is OD mode triggered by a hardware pulse on the START pin, not by *eod* bit set by I²C bus command (a special case of OD). The charging is initiated by the rising edge on the START pin and when V_{CAP} reaches V_{FIX} ($V_{CAP(max)}$), the active state starts autonomously, RDY goes high to show that VDH is regulating to VSET and ready to deliver full power.

Q5. How does the device enter an active state in On-demand operating mode? How does the device start a new charging cycle in On-demand operating mode?

Start: setting *eod* bit to 1 (through I²C bus command).

When V_{CAP} reaches V_{FIX} ($V_{CAP(max)}$), ***act* bit is set to 1 autonomously**. RDY goes high, and the load pulse should have arrived already and is applied to $V_{VDH} = V_{SET}$ in active state.

When V_{CAP} is discharged, both *act* and *eod* bits are reset to zero.

The new charging cycle **does not start autonomously,** we have to trigger new charge state by setting *eod* bit to 1, see Fig. 1.

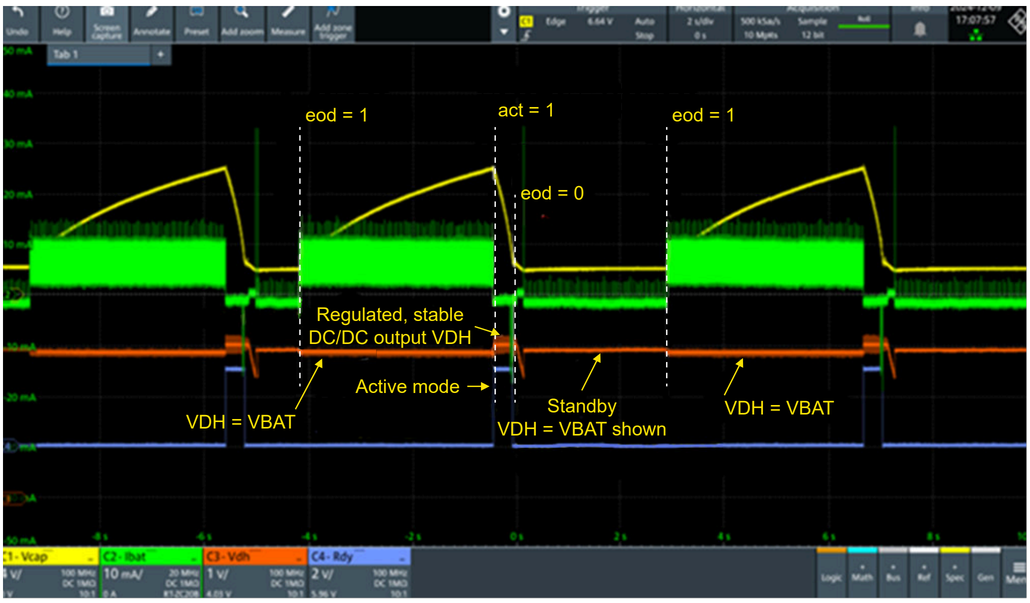


Fig. 1. Setting *eod* bit to 1

Q6. How does the device enter an active state in Continuous operating mode? How does the device starts a new charging cycle in Continuous operating mode? What does “refreshing” mean in Continuous mode of operation?

Start: *ecm* bit set to 1 (through I²C command).

When V_{CAP} reaches V_{FIX} ($V_{CAP(max)}$) – RDY goes high. If there is no load current pulse coming, we are waiting for the load pulse in order to set active state. **Active state is not set autonomously, we have to trigger this state.**

While waiting for the load pulse arrival, DC-DC gets in refreshing mode, to refresh V_{CAP} against the leakage discharge, by pulse enabling. VDH is still connected to VBT, the device is in a “quasi-charge state”.

When load is detected, **we set *act* bit high**, and VDH connects as VSET (disconnect from VBT) and the load is applied in active state.

When V_{CAP} is discharged, RDY goes low and the **DC-DC gets in new charge state autonomously**, *ecm* bit is set to 1, only *act* bit is reset to zero autonomously, see Fig. 2.

Fig. 2 also shows the benefits of using Hi-Z configuration on VDH, see Q11.

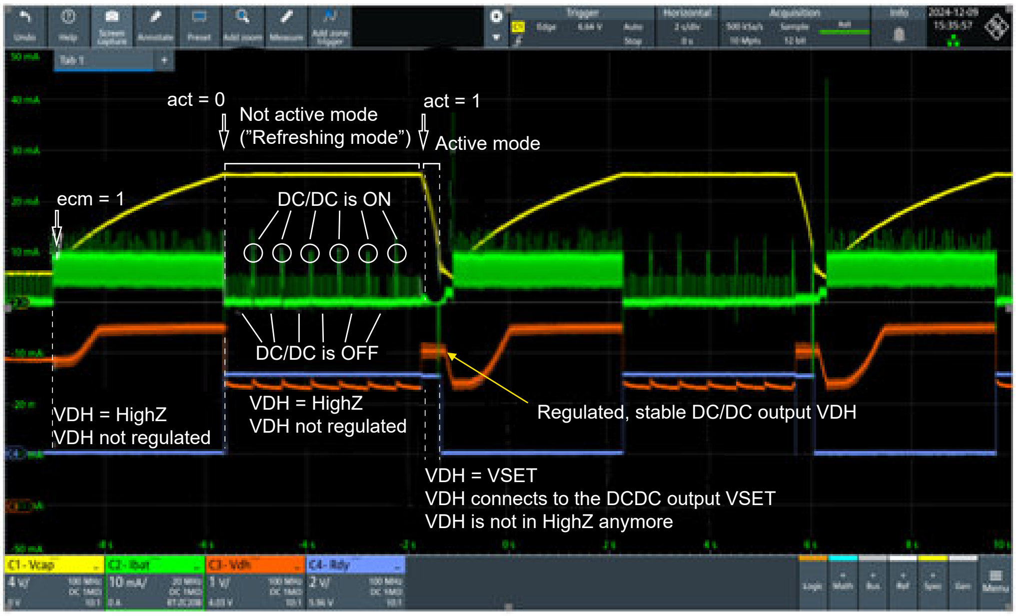


Fig. 2. Setting *ecm* bit to 1

Q7. How does the BB Auto mode end the active state?

Auto mode utilizes the START pin to set and reset the *eod* bit without the serial bus. There are two ways to define the end of the active state:

- Short pulse on START pin method: *act* bit goes zero, when VDH load current goes low, zero (no load applied anymore). The active state is not ended by the short pulse on the START pin, it ends when no load current is detected.
- Long pulse on START pin method: rising edge starts OD charging cycle, when V_{CAP} reaches V_{FIX} ($V_{CAP(max)}$), the device autonomously enters active state. Then the active state ends when the START voltage pulse goes low. So, when long START pulse is initiated, the START pin should be maintained high until the load pulse on VDH is concluded.

Q8. What is the relation of VBT to VDP and VDH?

VDH remains internally connected to VBT in all states of operation except the active state.

In other words, VDH is always connected to VBT in Standby and Charge State, and VBT pin is charging C_{STORE} internally (this charging does not show on VDH, instead VDH shows the VBT, the battery voltage). In active state VDH connects to DC-DC regulated V_{SET}, the V_{CSTORE} supplies the DC-DC regulated V_{SET}. VDH shows this regulated V_{SET} and does not show VBT anymore as the battery is disconnected.

VDP follows VDH.

Q9. What is the minimum voltage on VBT input?

The absolute minimum for VBT is 2.4 V. At battery voltages < 2.4 V, the BB cannot start switching and cannot initiate charge/discharging cycles.

The coin-cell battery can be used down only to 2.4 V. As the BB is extending the battery lifetime, there is no need to use the battery down to the last drop of charge (EoL = 2 V).

Q10. What happens to V_{VDP} and V_{VDH} when V_{VBT} falls below the minimum allowed voltage?

V_{VDH} and V_{VDP} will go to VBAT level. However, under heavy loading, V_{VDH} (VBAT) might collapse to 0 V as V_{VDH} is not regulated, it comes directly from the battery and is not regulated.

When VBAT < 2.4 V, the device is not switching, you cannot start new charge/discharge cycles with the C_{STORE}, therefore you cannot use V_{VDH} as regulated output in active state.

Q11. What is High Z state of VDH and how is this state used?

The High Z impedance state is set through the I²C bus register command – bit 4 of 0x0A reg is set to 1.

When in Hi-Z, VDH remains internally connected to VBT in all states of operation except the active state but shows as High-Z impedance output, it does not show the battery voltage V_{VBT}. VBT is charging C_{STORE} internally (this charging does not show on VDH, VDH does not show VBT, it shows as High Z impedance output).

In active state, VDH connects to DC-DC regulated V_{SET}, the V_{CSTORE} supplies the DC-DC regulated V_{SET}. VDH shows this regulated V_{SET} and does not show any more as High-Z impedance output. VBT is disconnected, the V_{CSTORE} supplies the DC-DC regulated V_{SET}.

This Hi-Z configuration is particularly useful when we want to isolate the load from VDH and the load capacitance is detached from the BB. In this way, no differential voltage can occur between VDH and VBT causing some battery current spikes.

Q12. Does the storage capacitor discharge to 0 V at the end of charging/ discharging cycle?

In both NBM7100x and NBM5100x, the storage capacitor never discharges completely to zero. As a result, there is always a residual voltage of 1.6 - 2 V at the end of the active state. There is no register to program a discharge level.

The residual storage capacitor can be higher than 2 V. For example, during an accidental random disconnection of VBT, this level can be any value between 2 V and $V_{CAP(max)}$.

The NBM5100x uses supercapacitors as storage element:

- At V_{CAP} max = 5 V, the stored energy can be quite high.
- Even at the residual voltage level of 2 V, relatively high energy is still stored which requires external discharging of the supercapacitors.

Users should be made aware of this residual storage capacitor charge and be advised to implement external discharging measures.

Q13. What is the BB Automotive Grade?

It is Automotive Grade 3: -40 °C to 80 °C. The BB can find automotive applications only in this temperature range.

Q14. Is there NVM space allocated in BB?

The BB does not have NVM space and must rely on the external MCU flash memory.

To fully implement all the BB features in CM and in OD modes, the BB must work with an external MCU with flash memory.

Q15. In what situations can the communication between external MCU and the BB be lost?

The VCC rail of the MCU must correspond to the BB VDP level for proper serial communication.

If this is not possible, level translators (shifters) must be used for the SDA/SDO, RDY, START/SDI and SCL/SCL signals (see *Table 11* in NBM5100x and NBM7100x data sheets).

Q16. When RDY is connected to MCU GPIO, is RDY an edge-triggering signal?

Yes, it is preferable that the MCU GPIO to be programmed to monitor the rising edge (or falling edge) of RDY to indicate when the RDY state is updated.

Q17. What is the purpose of the capacitor pre-charge switch in the DC/DC converter?

As shown in the sections about the DC-DC converter of the NBM5100X and NBM7100X datasheets, this switch connects VBT to VCAP. The purpose of the capacitor pre-charge switch is to linearly charge the initially fully-discharged storage capacitor so SW4 can get proper biasing. When the storage capacitor reaches 1.6 V, then the switches of the DC-DC converter (including SW4) can operate properly. The DC-DC coverter starts switching in boost mode and C_{STORE} is getting switch-mode charged. The delay caused by the necessity of this initial pre-charge is insignificant.

Q18. What is the purpose of C_{bypass}, the capacitor parallel to the coin-cell battery?

We are drawing DC current from the battery, which is the average (DC) of the boost converter input current. It is called “charging” current because it takes place only during the Charge state of the charging/discharging cycle.

The purpose of $C_{byspass}$ is to bypass (shunt) the switching ripple of this boost input current so only the DC term to be drawn from the battery (programmable 2mA, 4mA, 8mA, 16mA or 50mA), the average (DC) battery current.

The DC current drawn from the battery is the main advantage of NBM5100X/7100X compared to the competitor’s similar devices as they draw pulsing currents from the coin-cell battery which quickly destroys the battery chemistry.

3. Summary

The BB theory of operation as described the NBM5100x and NBM7100x datasheets is an excellent starting point for the users to understand the BB characteristics and technical parameters.

Undoubtedly, when this interesting chip started getting implemented in the field, more information was needed for successful applications. Having the answers to some of the more frequent field questions presented in this application note, should further help the users in their design efforts.

4. Revision history

Table 1. Revision history

Document ID	Release date	Description
AN90076 v. 1	20251124	Initial version

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