AN90064

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Application note

Pin FMEA for NXF6505 family

Abstract: This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of Nexperia's NXF6505 family under typical failure situations.

Keywords: Failure Modes and Effects Analysis (FMEA), 1.2 A transformer driver

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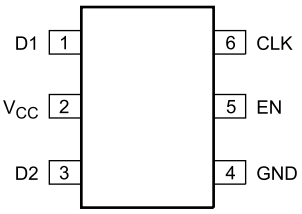
1. Introduction

The NXF6505A/B-Q100 is a specialized push-pull transformer driver that is designed for isolated power supplies in small form factors. This driver is capable of driving low-profile, center-tapped transformers from a 2.25V to 5.5V DC power supply.

The NXF6505A/B-Q100 features internal protection features such as current limiting, undervoltage lockout, thermal shutdown, and break-before-make circuitry, ensuring the device operates within safe limits. The device also includes a soft-start feature that prevents high inrush current during power-up with large load.

DA package
SOT8061-1 (TSOT23-6)



2. NXF6505 family overview

- Specified from -55 °C to +125 °C
- Push-pull driver for transformers, optimized for low EMI:
  - Slew-rate control output
  - Spread Spectrum Clocking (SSC)
- Internal switching frequency:
  - for NXF6505A-Q100: 160 kHz
  - for NXF6505B-Q100: 440 kHz
- Synchronization of multiple devices with external clock input
- Wide input voltage range: 2.25 V to 5.5 V
- High output drive: 1.2 A at 5 V supply
- 2.2A current limit at 5 V
- Thermal shutdown protection
- Small6 pin SOT8061-1 (SC-74; TSOP-6) package
- ESD protection:
  - HBM:ANSI/ESDA/JEDEC JS-001 class 3A exceeds 6000 V
  - CDM:ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1500 V

3. Pin FMEA

This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of Nexperia's NXF6505 family under typical failure situations such as a short-circuit to V_{CC} or GND or to a neighboring pin, or if a pin is left open.

A failure is classified according to its effect on the NXF6505 device and the functionality of the application; see Table 1.

Table 1. Classification of failure effects

Class	Failure effect
A	damage to device
	affects application functionality
B	no damage to device
	may affect application functionality
C	no damage to device
	no affect to application functionality

Table 2. FMEA matrix for pins short-circuited to GND

Pin	Pin No	Class	Remarks
D1	1	A	Short circuit path between Vcc and ground through transformer winding and D1, causing high current to flow and possible damage to transformer. Output voltage out of designed spec.
Vcc	2	B	No isolated output voltage due to the absent of power.
D2	3	A	Short circuit path between Vcc and ground through transformer winding and D2, causing high current to flow and possible damage to transformer. Output voltage out of designed spec.
GND	4	C	Normal operation.
EN	5	B	Device disabled. Transformer is not actively driven.
CLK	6	B	No external clock, internal clock is driving the power MOSFETs.

Table 3. FMEA matrix for pins left open

Pin	Pin No	Class	Remarks
D1	1	B	One of the primary transformer windings does not store energy with D1 open. Secondary output supply is out of intended set-point.
Vcc	2	B	No switching action of D1/D2. Isolated output voltage does not build up.
D2	3	B	One of the primary transformer winding does not store energy with D2 open. Secondary output supply is out of intended set-point.
GND	4	B	No switching action of D1/D2. Isolated output voltage does not build up.
EN	5	B	Device disabled.
CLK	6	B	No external clock, internal clock is driving the power MOSFETs.

Table 4. FMEA matrix for pins short-circuited to supply

Pin	Pin No	Class	Remarks
D1	1	A	Potential difference between one of the transformer winding is zero caused by D1 stuck high. When D1 FET switches on, high current flows from supply to ground. Secondary output supply out of intended set-point.
Vcc	2	C	Normal operation
D2	3	A	Potential difference between one of the transformer winding is zero caused by D2 stuck high. When D2 FET switches on, high current flows from supply to ground. Secondary output supply out of intended set-point.
GND	4	B	No switching action of D1/D2. Secondary output voltage does not build up.
EN	5	B	Functionality to disable the device lost.
CLK	6	B	No external clock, internal clock is driving the power MOSFETs.

Table 5. FMEA matrix for pins short-circuited to adjacent pin

Pin	Pin No	Shorted to	Class	Remarks
D1	1	Vcc	A	Potential difference between one of the transformer winding is zero caused by D1 stuck high. When D1 FET switches on, high current flows from supply to ground. Secondary output supply out of intended set-point.
Vcc	2	D2	A	Potential difference between one of the transformer winding is zero caused by D2 stuck high. When D2 FET switches on, high current flows from supply to ground. Secondary output supply out of intended set-point.
D2	3	GND	C	Not considered. Corner pin.
GND	4	EN	B	Device disabled.
EN	5	CLK	B	If EN is tied high on PCB, external clock synchronization functionality is lost. If CLK is tied low on PCB, Device disabled.
CLK	6	D1	C	Not considered. Corner pin.

4. Revision history

Table 6. Revision history

Rev	Date	Description
AN90064 v.1	20250219	AN90064 initial version

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For sales office addresses, please send an email to: salesaddresses@nexperia.com
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