AN90059

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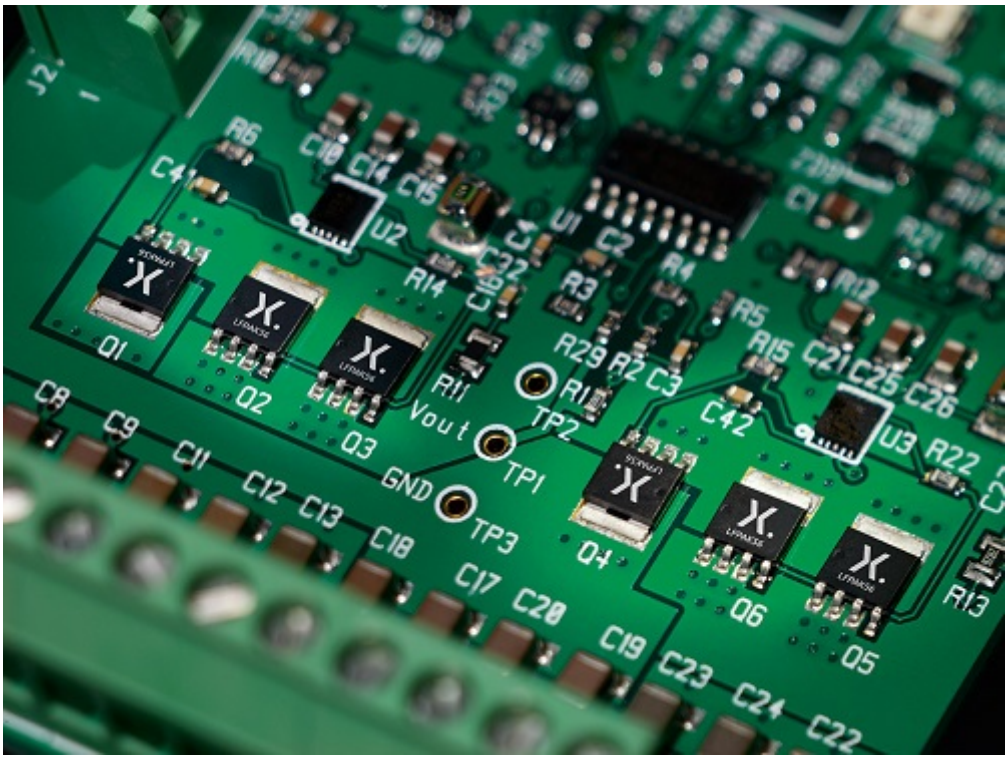
Power MOSFET gate driver fundamentals



Abstract: This application note describes the switching process of a MOSFET, introduces the fundamentals of power MOSFET gate drive circuits and demonstrates the most useful and widely used topologies. A focus is made towards using discrete components rather than gate driver ICs to help build an understanding of the fundamentals of gate driver circuits.

Keywords: MOSFET, gate charge, input capacitance, gate drive, high side, low side, isolated, transformer, optocoupler, photocoupler, bootstrap, charge pump, discrete, totem pole, push pull, level shift, switching

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1. Introduction

The power MOSFET can be regarded as a voltage-controlled switch. Applying a voltage between the gate and source terminals (V_{GS}) turns the MOSFET on, allowing current to flow through the channel from the drain to the source.

When fully enhanced, a power MOSFET operates close to its rated on-state resistance ($R_{DS(on)}$). Increasing the gate voltage beyond the full enhancement level results in only a minor reduction in $R_{DS(on)}$.

This application note primarily focuses on the following aspects:

- The detailed process of turning on a MOSFET
- The requirements for the gate drive circuit
- Some of the most practical and widely used gate drive circuit topologies

Unless otherwise specified, this application note refers exclusively to n-channel enhancement-mode (normally off) MOSFETs. However, the methods described can also be applied to driving IGBTs and SiC MOSFETs.

2. MOSFET characteristics

2.1. Capacitance

All MOSFETs have inherent capacitance (see Fig. 1). These are not external capacitors but are intrinsic to the MOSFET and result from its structure.

The capacitances are:

- C_{GD}: the capacitance between the gate and drain of the MOSFET, sometimes referred to as the Miller capacitance.
- C_{GS}: the capacitance between the gate and source of the MOSFET. The gate-source capacitance must be charged to the threshold voltage of the MOSFET before current begins to flow through the drain.
- C_{DS}: the capacitance between the drain and source of the MOSFET.

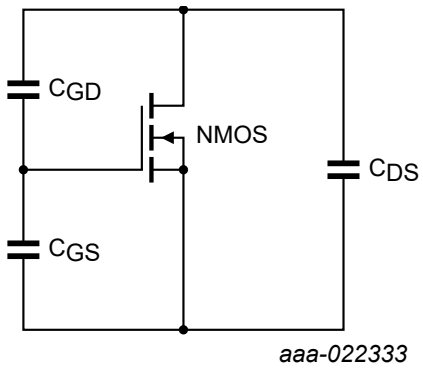


Fig. 1. MOSFET capacitance parameters

The intrinsic capacitance of a MOSFET can also be characterized as follows:

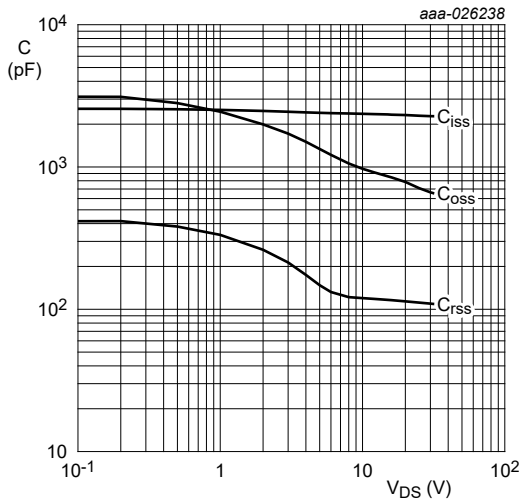
- C_{iss}: input capacitance
- C_{oss}: output capacitance
- C_{rss}: reverse transfer (or feedback) capacitance

C_{iss}, C_{oss}, and C_{rss} can be measured at the device pins.

The relationship between the inherent capacitance and the intrinsic capacitance is as follows:

- $C_{iss} = C_{GS} + C_{GD}$
- $C_{oss} = C_{DS} + C_{GD}$
- $C_{rss} = C_{GD}$

The gate-source capacitance C_{GS} remains relatively constant under all operating conditions. However, C_{DS} is a function of the drain-source voltage (V_{DS}), and C_{GD} is a function of both V_{DS} and V_{GD} (gate-drain voltage). Excluding C_{GS}, the relationship between capacitance and voltage is non-linear (see Fig. 2).



- V_{GS} = 0 V
- f = 1 MHz

Fig. 2. Capacitance as a function of drain source voltage

The input capacitance C_{iss} is an important parameter when evaluating switching performance. To turn the MOSFET on, the input capacitance must be charged sufficiently.

Due to capacitance variation with voltage, it is more useful to refer to the gate charge data rather than the capacitance data when determining switching performance.

2.2. Gate charge

Total gate charge ($Q_{G(tot)}$), gate-source charge (Q_{GS}), and gate-drain charge (Q_{GD}) describe the amount of gate charge required for the MOSFET to switch. This is particularly important in high-frequency switching applications, for example, above 100kHz, since much of the power loss occurs during switching, when there are simultaneous significant changes in voltage and current between the drain, gate, and source. The higher the gate charge, the longer the switching times are, and this results in more losses. In the blocking state, there are significant voltages but negligible leakage currents. In the full-on state, there are significant currents and low voltages.

The gate charge curve describes what happens to a MOSFET during the turn-on event (refer to Fig. 3). The turn-off event is approximately the inverse of the turn-on, except that turn-off is usually slower than turn-on, see 1. The test circuit supplies the drain of the MOSFET with either a constant voltage or a constant current as would typically be seen in a half-bridge application switching an inductive load. In the initial stage of the switching event, the gate charge begins to build up, and consequently, V_{GS} rises from zero. The MOSFET only starts to conduct once the V_{GS} reaches the threshold voltage ($V_{GS(th)}$).

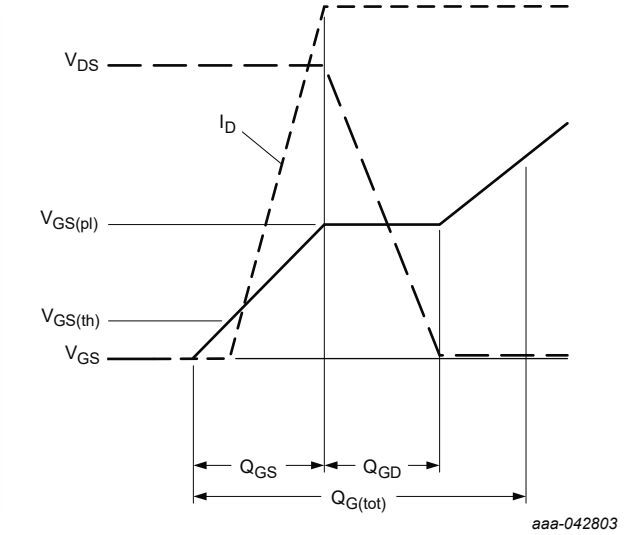


Fig. 3. Gate charge curve showing V_{GS}, V_{DS} and I_D

The gate-source voltage continues to rise until it reaches a plateau, $V_{GS(pl)}$. The plateau (also known as the Miller plateau) is associated with C_{GD} and the gate-drain charge (Q_{GD}). During this miller effect period, the Miller capacitance increases while V_{DS} is decreases. V_{GS} stays constant because the drain current has reached its operating point. The gate current charges C_{GD}. Therefore, the gate-drain voltage (V_{GD}) rises which leads to V_{DS} falling, since V_{GS} is fixed. Since the Miller capacitance has increased, most of the current flows through C_{GD} and not C_{GS} (Q_{GD} builds up but Q_{GS} does not).

Once V_{DS} has fallen almost completely, we reach the end of the plateau. At this point, the Miller capacitance stops increasing and any further increases in gate charge increase the gate-source voltage until it reaches the gate drive voltage. After the miller plateau, V_{DS} still continues to drop slightly as the drain-source resistance gets lower with an increase in V_{GS}. The higher the voltage on the gate the higher the charge applied ($Q = C \times V$), further reducing the R_{DSon}.

Throughout the switching process, there are significant currents and voltages concurrently between the drain and source, so Q_{GD} and Q_{GS} are important when considering switching losses.

Once the end of the Miller plateau is reached, the gate-source voltage increases again, but with a larger capacitance than before Q_{GS} has been reached. The gradient of the gate charge curve is less above the Miller plateau.

Power MOSFETs (of the same technology) with lower R_{DSon} have a larger die and consequently larger intrinsic capacitance. This means that a larger amount of gate charge is required to switch the device (and thus will have slower switching). More advanced technologies generally have lower gate charges for a given R_{DSon} compared to less advanced technologies.

The gate-charge parameters are highly dependent on the measurement conditions. Different suppliers often quote their gate-charge parameters for different conditions, demanding care when comparing gate charge parameters from different sources.

Higher I_D leads to higher values of Q_{GS} because the plateau voltage is also higher. This relates to the transfer characteristic which shows the dependency of drain current on gate-source voltage.

Higher V_{DS} leads to higher values of Q_{GD} and $Q_{G(tot)}$, as the plateau duration increases (see Fig. 4).

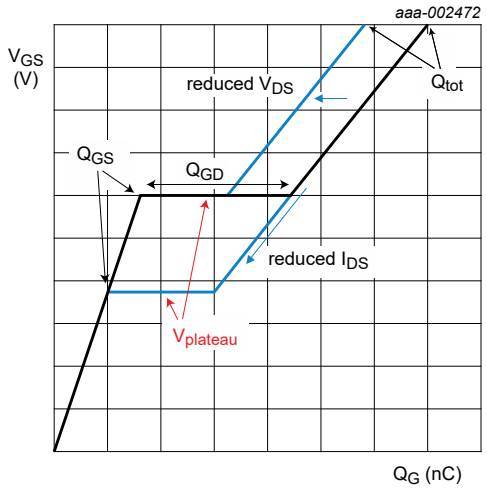


Fig. 4. Features of gate charge curve

2.3. Gate charge test circuit

The test circuit for determining gate charge is shown in Fig. 5. The MOSFET is supplied with a constant drain current which is clamped to a set V_{DS}. The gate is supplied with a constant current. The diode is used to clamp the drain-source voltage to the voltage supply.

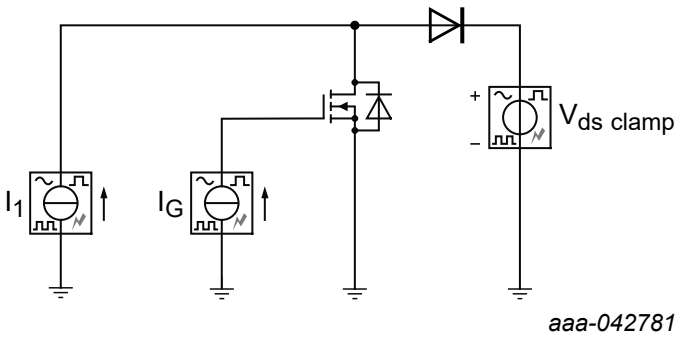
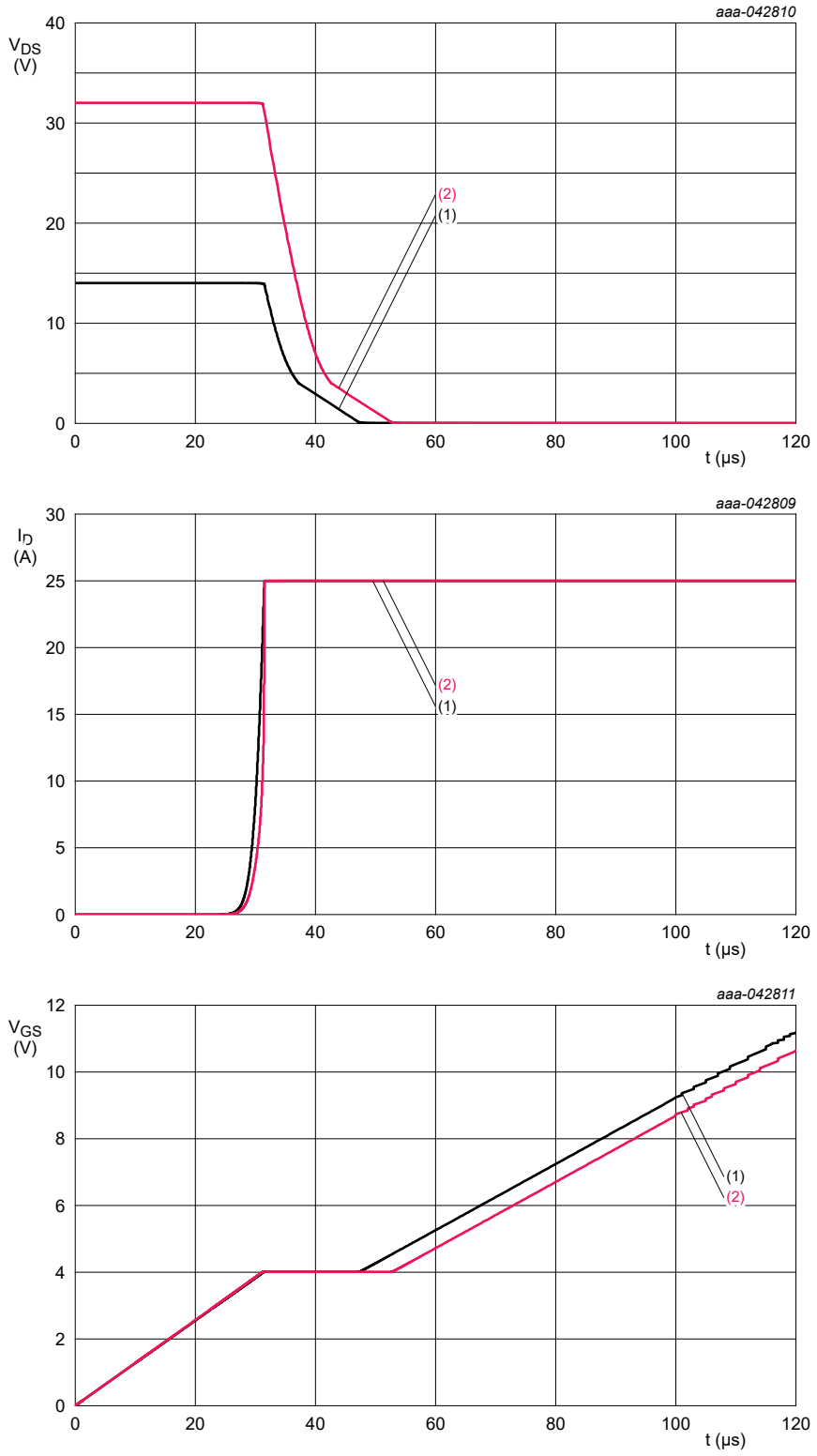


Fig. 5. Gate charge test circuit

Fig. 6 shows the resulting simulation waveform. The circuit is simulated at two V_{DS} values: 32 V and 14 V. Time is shown on the x-axis but is essentially the same as the V_{GS} vs Q_G graph from Fig. 4 since the gate is driven with a constant current, which is 1 mA in this case. By multiplying the x-axis by 1 mA, the result is gate charge in nC.



- (1) V_{DS} = 14 V
- (2) V_{DS} = 32 V

Fig. 6. Gate charge test circuit simulated waveform

3. Gate driver circuit requirements

3.1. Gate drive voltage

The gate driver circuit needs to supply a voltage high enough to fully turn on the MOSFET. For turning off, the gate drive voltage must be low enough so that the MOSFET can be completely off, for example, $V_{GS} < V_{GS(th)}$.

The voltage levels coming from most MCUs are 5 V or 3.3 V. While logic level MOSFETs are designed to be driven with a 5 V gate voltage, standard level MOSFETs require at least 10 V V_{GS} to be fully turned on. Sometimes it is desired to obtain as high a V_{GS} as possible, within the datasheet limits, to minimize the R_{DSon}. This is one reason why we need dedicated gate driver circuits.

In some applications, the supply voltage for the gate drive circuit may be subjected to severe variation, for example, cold crank or load dump condition in automotive, and this may have some influence in the V_{GS} supply range. Therefore, some headroom may need to be designed in to account for worst case conditions.

If the gate voltage is too low, the MOSFET might not turn on fully and it will have a high R_{DSon}, which can cause significant power loss and heating. If the gate voltage is too high, the MOSFET could get damaged (by exceeding its maximum rating $V_{GS(max)}$).

Along with checking the $V_{GS(th)}$ and $V_{GS(max)}$ in order to find the right voltage level MOSFET, it is important also to check the R_{DSon} of the MOSFET against the gate drive voltage.

Consider an example where a MOSFET is driven by a 3.3 V gate drive. The following specifications apply to the BUK6D16-30E MOSFET:

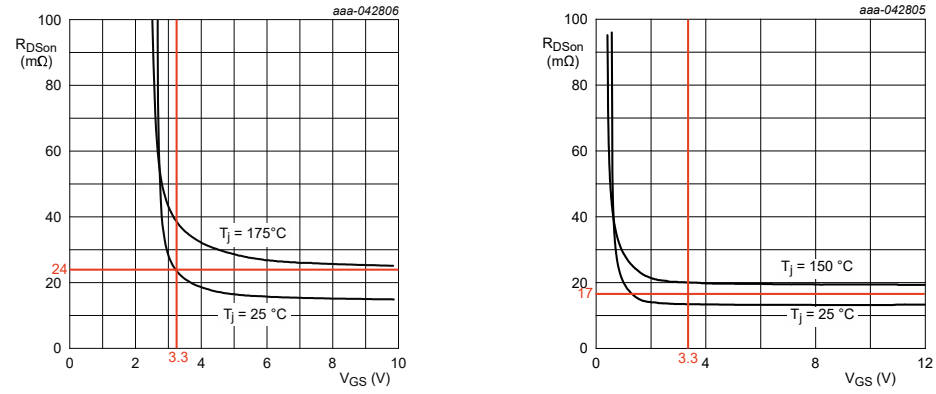
- $V_{GS(th)}$ = 1 V (min) to 2.5 V (max)
- R_{DSon} = 13.4 mΩ @ V_{GS} = 10 V or 17 mΩ @ V_{GS} = 4.5 V
- $V_{GS(max)}$ = 20 V

This means that this MOSFET starts conducting at around 2 V V_{GS}, but it still has a high drain-source resistance at 3.3 V V_{GS} (see (a) of Fig. 7) and hence high power loss.

Alternatively, users can look for a MOSFET that has a lower $V_{GS(th)}$ and lower R_{DSon} at 3.3 V V_{GS}, such as the PMPB20XNEA (see (b) of Fig. 7), which has the following specifications:

- $V_{GS(th)}$ = 0.75 V (min) to 1.25 V (max)
- R_{DSon} = 16 mΩ @ V_{GS} = 4.5 V or 24 mΩ @ V_{GS} = 2.5 V
- $V_{GS(max)}$ = 12 V

This MOSFET can be almost fully turned on by a 3.3 V gate drive and has a lower drain-source resistance at this V_{GS}, hence less power loss. Furthermore, PMPB20XNEA has a larger V_{GS} margin from where the R_{DSon} increases dramatically (as shown by the vertical asymptote in Fig. 7). It is important to have some headroom here to ensure the device performance even with part-to-part variation. Part-to-part variation is accounted for once the design considers the minimum and maximum values stated on the datasheet.



(a) BUK6D16-30E (b) PMPB20XNEA

Fig. 7. On-state resistance as a function of gate-source voltage

3.2. Gate current

It is a requirement of the gate driver circuit to charge and discharge the input capacitance of the MOSFET. Thus, the gate driver needs to source a current during the turn-on of the MOSFET, and it needs to sink a current during turn-off. When the MOSFET is not switching, the gate current is often negligible.

The higher the gate current, the less time it will take to fully charge or discharge the gate of the MOSFET. Thus, higher gate current results in faster switching.

The following formula can be used to calculate the gate current during the plateau period:

$$I_{G\_pl} = (V_{drive} - V_{pl}) / R_{G(tot)} \quad (1)$$

Where I_{G_pl} is gate current during the plateau, V_{drive} is the applied gate voltage, V_{pl} is the plateau voltage, $R_{G(tot)}$ is the resistance between the MOSFET gate and the gate input voltage.

$R_{G(tot)}$ consists of the internal gate resistance of the MOSFET $R_{G(int)}$, the external gate resistance $R_{G(ext)}$ and the output resistance from the gate driver circuit $R_{out(driver)}$. $R_{G(int)}$ is usually in the order of a few ohms or less.

$$R_{G(tot)} = R_{G(int)} + R_{G(ext)} + R_{out(driver)} \quad (2)$$

Consider the following example:

Calculate the gate current during the plateau when switching power MOSFET BUK7S1R0-40H on and off, where V_{drive} is switching between 10 V and 0 V and $R_{G(tot)}$ is 10 Ω. In this scenario, the drain current is 25 A and the ambient temperature is 25 °C. From the datasheet of the MOSFET, the plateau voltage is around 4.2 V for these conditions. Using Formula 1,

$I_{G\_pl(on)} = (10 - 4.2) / 10 = 0.58$ A

$I_{G\_pl(off)} = (0 - 4.2) / 10 = -0.42$ A

The current during turn-off is usually lower than during turn-on and as a result, turn-off is typically slower than turn-on.

To calculate the peak I_G during the switching event, V_{pl} can be set to 0 V in Formula 1. Taking the same BUK7S1R0-40H example as before,

$I_{G(pk)} = (10 - 0) / 10 = 1$ A

As shown in the calculations above, the gate driver is required to source or sink significant current during the switching event (when fast switching is required). If the gate driver circuit is driving multiple MOSFETs in parallel, then the current requirement is even more demanding. Refer to 2 for detailed information on paralleling MOSFETs.

3.3. Gate resistance

$R_{G(tot)}$ is the resistance on the path that the gate current flows. As was mentioned in Section 3.2, a larger I_G results in faster switching time. Formula 1 indicates that a larger $R_{G(tot)}$ results in a lower I_G, and thus, reduces the switching speed.

Selecting $R_{G(ext)}$ provides a method of controlling the speed of switching the MOSFET. However, it is important to remember that $R_{G(int)}$ and $R_{out(driver)}$ also impact the maximum attainable I_G.

The selection of $R_{G(ext)}$ is important, and it is a balancing act since both slowing and speeding up the switching speed come with their own set of advantages (see 3).

Advantages of lower-speed switching:

- Reduce reverse recovery current (since it is a function of dI/dt)
- Reduce spiking and ringing caused by parasitic inductance and capacitance in the circuit. Reducing voltage spikes reduces the likelihood of the MOSFET going into avalanche mode. The gate resistance dampens the oscillations in the gate loop.
- Reduce risk of gate bounce, refer to 3, 4, and 5 for details.
- Improve EMC by reducing EMI emissions

Advantages of higher-speed switching:

- Lower switching losses
- Lower power losses mean less heat being generated by the MOSFET, which allows designers to choose smaller and more cost-effective MOSFETs and PCB solutions.
- Improve efficiency which reduces energy waste

The higher the switching frequency, the more significant the switching losses are (see Formula 3). Therefore, minimizing switching losses is most important when operating at higher switching frequencies.

$$P_{sw} = E_{sw} * f_{sw} \quad (3)$$

The remaining sections of this document describe further methods on how to speed up the switching of the MOSFET by reducing the impedance on the gate current path, thus, increasing the gate drive source or sink current.

3.4. Circuit parasitic elements

It is important to consider parasitic inductance in the gate driver circuit, especially when fast switching is required. Parasitic inductance in the gate-source loop can cause voltage and current spikes and oscillations as the parasitic inductance and the MOSFET's capacitance can form an LC resonant circuit. The oscillations on V_{DS} and V_{GS} can cause or exacerbate EMI issues, affecting the system's EMC. Refer to 3 for detail.

The main contributor to parasitic inductance is the wires or the PCB track. It is important to keep the area coverage by the gate-source loop as small as possible to minimize loop inductance. For example, place components close together and use good layout practice, see 6. Adding gate resistance dampens the oscillations. There is some package parasitic inductance and resistance within the MOSFET that is based on the design of the package and is not something the circuit designer can control.

To demonstrate this, the circuit shown in Fig. 8 is simulated while varying L_G and R_G. In this case, R_G corresponds to the external gate resistance only.

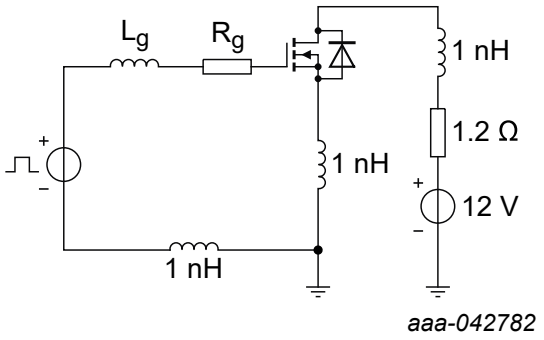
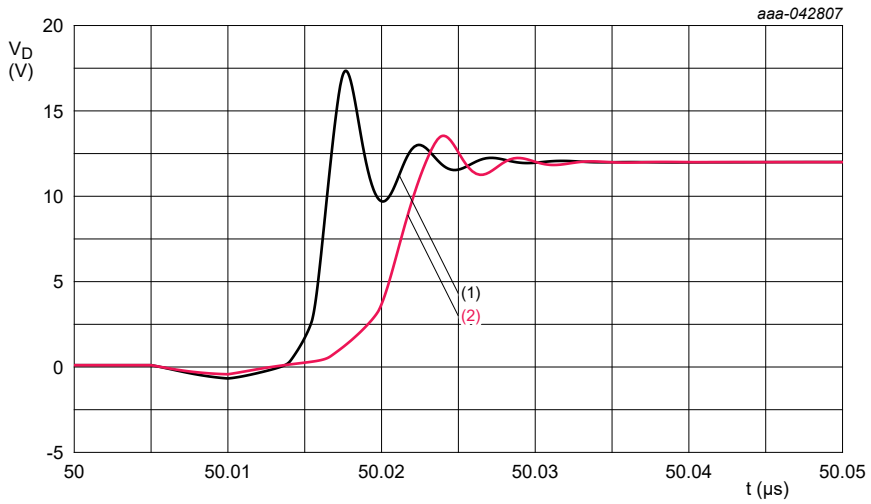


Fig. 8. Circuit with parasitic inductance included

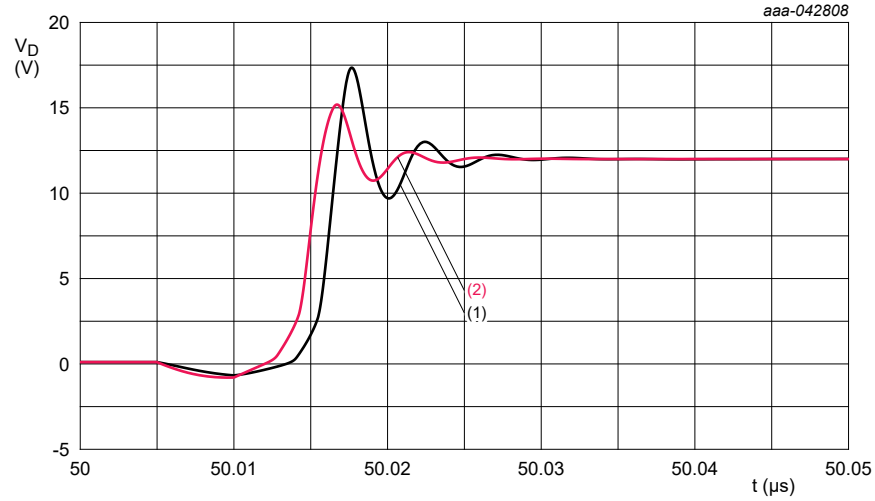
Fig. 9 shows the drain voltage for two different gate resistances. The voltage spikes and oscillations are greatly reduced by the larger gate resistance. Although the spiking and ringing have been reduced, the additional gate resistance has slowed down the switching speed. Slowing the switching speed has doubled the switching loss in this case.



- (1) R_G = 0.1 Ω
- (2) R_G = 2 Ω

Fig. 9. Simulated drain voltage showing the effect of gate resistance.

The same circuit from Fig. 8 is simulated again but the gate inductance is changed. The resulting drain voltage is shown in Fig. 10. The spiking and ringing are more severe for the larger inductance, while rising time and settling time is similar for both.



- (1) L_G = 5nH
- (2) L_G = 1nH

Fig. 10. Simulated drain voltage showing the effect of gate inductance

3.5. Gate driver power consumption

It is important to have low power consumption in the gate drive circuit to achieve high efficiency. This is particularly important in cases where the gate drive supply has limited capacity, for example, bootstrap or charge pump.

The total power dissipation in the gate driver circuit is dependent on the circuit topology, selection of components, duty cycle, and frequency. For example, in the gate driver shown in Fig. 16, the value of resistance chosen in the level shift stage impacts how much power is dissipated in the gate drive circuit.

However, the required energy and average power to switch the MOSFET for any topology can be changed using Formula 4 and 5 respectively. In this way, the energy losses for turn-on and turn-off can be calculated.

$$E_G=Q_{G(tot)}*V_{GS} \quad (4)$$

$$P_G=Q_{G(tot)}*V_{GS}*f_{sw} \quad (5)$$

For example, the average power required from the gate driver to switch BUK7S1R0-40H with 10V V_{GS} at a switching frequency of 100kHz can be calculated as follow:

P_G = 98nC*10V*100kHz = 98mW

Additionally, the MOSFET gate energy to turn on is dissipated in the gate driver or in the gate resistance during turn-off.

Since $Q_{G(tot)}=C_{iss}V_{GS}$, Formula 4 can be re-written as:

$E_G=C_{iss}V_{GS}^{\ 2}$

During turn-on, there is an energy loss of $C_{iss}V_{GS}^{\ 2}/2$ in the gate resistance and $C_{iss}V_{GS}^{\ 2}/2$ is the energy that is stored in the input capacitance.

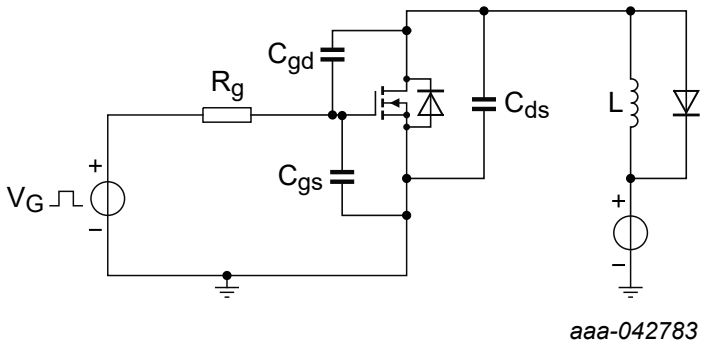
During turn-off, the energy stored in C_{iss} is dissipated in the gate resistance. Due to the non-linear relationship between C_{iss} and V_{DS}, it is better to use $Q_{G(tot)}$ to calculate losses, as in Formula 4 and 5.

3.6. Switching time calculations

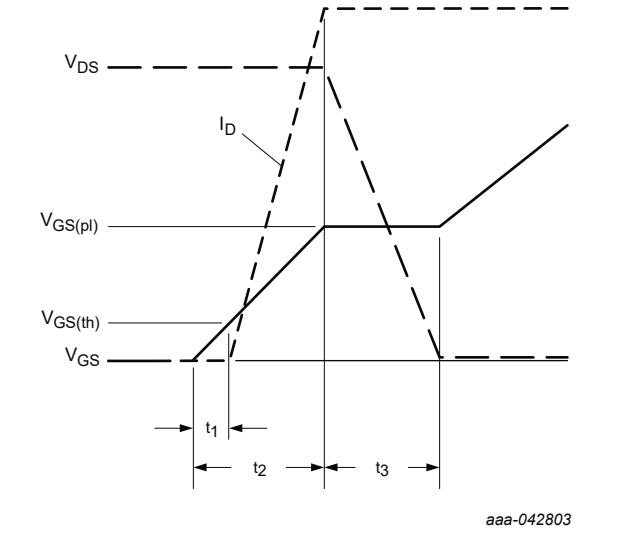
In general, switching time of a MOSFET mentioned in the data sheet are turn-on delay, turn-off delay, rise and fall times. These are measured with resistive load, making them unsuitable for inductive loads.

However, here in this section analytical solutions for the turn-on and turn-off time periods of the MOSFET are analyzed with an inductive load show in Fig. 11.

Note: Gate charge in Section 2.2 is for Inductive switching which can be applied here.



(a) Block diagram



(b) Waveform

Fig. 11. Gate charge circuit with inductive load

Fig. 12 explains the equivalent circuit of the MOSFET gate with internal gate resistance (R_g) and input capacitance C_{gs} and C_{gd}.

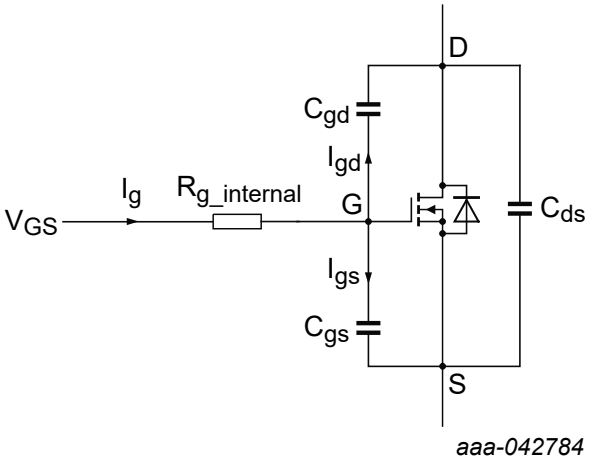


Fig. 12. MOSFET equivalent circuit

The turn-on event of MOSFET explained in Section 2.2 and Fig. 11, during which the period t_1, the gate drive charges the gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} via the gate series resistor R_g until V_{GS} reaches to threshold voltage $V_{GS(th)}$. Hence, the gate current I_g flows through the parallel capacitors C_{gs} and C_{gd} and is given as

$$I_g = I_{gs} + I_{gd} \tag{6}$$

$$I_g = C_{gs}\frac{dV_{GS}}{dt} + C_{gd}\frac{dV_{GS}}{dt} \tag{7}$$

Also,

$$I_g = \frac{V_G - V_{GS}}{R_g} \tag{8}$$

Therefore,

$$\frac{dV_{GS}}{V_G - V_{GS}} = \frac{dt}{R_g \times (C_{gs} + C_{gd})} \tag{9}$$

Solving the above equations results in

$$V_{GS} = V_G\left(1 - e^{\frac{-t}{R_g \times (C_{gs}+C_{gd})}}\right) \tag{10}$$

Where

- $C_{iss} = C_{gs} + C_{gd}$
- $R_g = R_{g\_internal} + R_{g\_external}$

t_1 is the required time to reach threshold voltage $V_{GS(th)}$, Hence, substituting $V_{GS(th)}$ for V_{GS}, at time t_1 is obtained as

$$t_1 = R_g(C_{gs} + C_{gd})\,ln(V_G / (V_G - V_{GS(th)})) \tag{11}$$

Similarly, during the time t_1 to t_2, V_{GS} exceeds $V_{GS(th)}$, and C_{iss} continues to be charged and at t_2, the gate voltage reaches the plateau voltage $V_{GS(pl)}$ and then obtained the following formula for t_2:

$$t_2 = R_g(C_{gs} + C_{gd})\,ln(V_G / (V_G - V_{GS(pl)})) \tag{12}$$

During the period t_3, the gate voltage remains constant at the $V_{GS(pl)}$ voltage, the gate current flows through C_{gd} and not through C_{gs} since V_{GS} is fixed. Therefore, the gate-drain voltage (V_{GD}) rises which leads to V_{DS} falling to almost zero. Calculating time t_3 directly is difficult since C_{gd} changes with V_{ds}. So gate charge should be taken into consideration instead of capacitance to determine the switching time t_3.

Referring to Fig. 3. Q_{GS} is the charge associated with the period t_2, where the V_{GS} starts to rise and reaches $V_{GS(pl)}$. During this period V_{ds} does not change so C_{gd} stays constant. At this time most of the drive current flows through C_{gs} rather than C_{gd}. So the gate charge during t_2 is assumed to be Q_{GS}.

Q_{GD} is associated with the time period t_3 where V_{GS} stays constant, and the drain current has reached its operating point. During this period, the miller capacitance C_{gd} increases as V_{DS} is falling. Since C_{gd} is increased most of the current flows through C_{gd} rather than C_{gs}.

Considering C_{gd}, t_3 is derived as below:

$$t_3 = R_g C_{gd} \times \frac{V_{DS}}{V_G - V_{GS(pl)}} \tag{13}$$

Also, considering the charge stored in C_{gd} during the time period t_3,

$$t_3 = R_g Q_{gd} \times \frac{1}{V_G - V_{GS(pl)}} \tag{14}$$

And after t_3, both C_{gs} and C_{gd} are charged until the gate-source voltage V_{GS} reaches the final gate drive voltage.

Lastly, the definitions of the switching times are given in Fig. 13. The turn-off event is considered as the inverse of the turn-on.

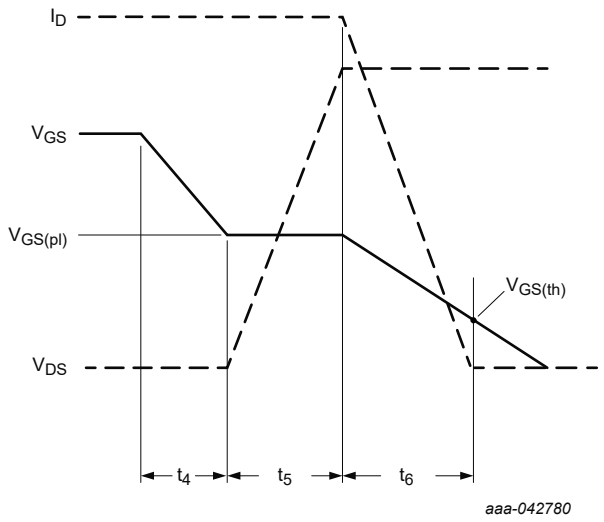


Fig. 13. MOSFET turn-off transient waveform

Based on the turn off sequences explained in Fig. 13,

t_4 is the gate voltage fall time from V_{GS} to $V_{GS(pl)}$, there is no changes to V_{DS} or I_{DS}.

$$t_4 = R_g\left(C_{gs} + C_{gd}\right) \times ln\left(\frac{V_{GS}}{V_{GS(pl)}}\right) \tag{15}$$

t_5 is the turn-off plateau time, where the V_{DS} rises from a low saturated value to V_{DD}. I_D does not change. Also C_{gd} changes as the V_{DS} rises, it is difficult to calculate t_5 with capacitance C_{gd}.

$$t_5 = R_g C_{gd} \times \frac{V_{DS}}{V_{GS(pl)}} \tag{16}$$

Considering Q_{gd} for calculating t_5,

$$t_5 = R_g Q_{gd} \times \frac{1}{V_{GS(pl)}} \tag{17}$$

t_6 is the required time for V_{GS} to fall from plateau $V_{GS(pl)}$ to gate threshold $V_{GS(th)}$, also the current I_D falls to 0 A,

$$t_6 = R_g\left(C_{gs} + C_{gd}\right) \times ln\left(\frac{V_{GS(pl)}}{V_{GS(th)}}\right) \tag{18}$$

Formula 11 to 18 give the approximate method of calculating switching times without considering the second order and additional parasitic in the circuit.

Comparing equations with an example SPICE model simulation

The described method can be verified with simulation example in LT SPICE using BUK7S1R0-40H device and compare with values obtained using the fore-mentioned formulas. A simple switching circuit with inductive load as shown in Fig. 11, for the following circuit conditions:

- V_g = 10 V
- $R_{g\_external}$ = 47 Ω
- L = 30 µH

- V_{DD} = 32 V
- I_D = 20 A

Table 1 presents the comparison between simulated switching times and the calculated from the fore-mentioned formulas.

Table 1. Switching times calculation

Switching times	Calculated values (ns)	Simulation results (ns)	Source
Turn-on switching			
t_1	126	115	Formula 11
t_2	192	166	Formula 12
t_3	140	155	Formula 14
Turn-off switching			
t_4	306	396	Formula 15
t_5	194	209	Formula 17
t_6	119	111	Formula 18

4. MOSFET gate driver circuits

4.1. Low-side driver circuits

4.1.1. MCU direct drive

Most MCU GPIO pins can supply 3.3 V or 5 V as a high output. As discussed in Section 3.1, this can be enough to turn on a low threshold MOSFET – meaning that in some cases, the MOSFET can be driven directly from the MCU (see Fig. 14). A 3.3V gate voltage is suitable for MOSFETs with a typical threshold of around 0.7 V - 1 V. A 5 V gate voltage is suitable for MOSFETs with a typical threshold of around 1.5 V - 2 V. MCU direct drive is one of the simplest ways to drive a MOSFET but has significant drawbacks and limitations.

For example, care must be taken since most micro-controllers can only source or sink a small amount of current (usually no more than 10's of mA). Power dissipation could also be an issue if Q_G or the switching frequency is too large (see Formula 5). In the case of a fault (for example, MOSFET failure), a surge current could flow and the MCU can get damaged. It is important to place a large enough gate resistance to ensure that the current limits are not exceeded. Proper bypassing of the MCU's supply voltage must be ensured by selecting an appropriate value capacitor.

Due to the limited input/output current capability of the controller, it takes a long time to switch the MOSFET. Thus, it is only a viable option in low frequency applications and for driving small MOSFETs with low Q_G. This gate drive method may be suitable for driving small loads such as LEDs.

Another consideration is that the R_{DSon} may be higher than expected due to the gate drive voltage not being high enough. Attention should be given to the V_{GS} vs R_{DSon} graph given in the MOSFET datasheet (see Section 3.1).

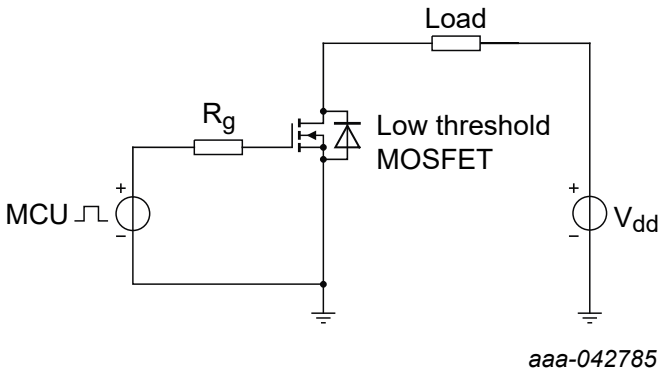


Fig. 14. MCU direct drive circuit

4.1.2. Bipolar totem-pole driver

The bipolar totem-pole driver is commonly used for driving MOSFETs (see Fig. 15). This incorporates an NPN and PNP transistor in a coupled emitter configuration with their bases tied together. It takes advantage of the high current gain properties of the BJT to source and sink large peak currents to or from the gate of the MOSFET, enabling the possibility of high-speed switching (for example, up to 100s of kHz). This NPN and PNP pair is often called a push-pull circuit since it is pushing and pulling current from the MOSFET's gate.

If there is a logic high V_{drive}, the NPN transistor will be switched on and a logic high voltage will be applied to the MOSFET's gate with current being sourced from V_{supply}. If 0 V is applied to the base of the transistors, then the PNP pulls the gate voltage near to ground (about 0.7 V) and the current is pulled from the gate through the PNP transistor.

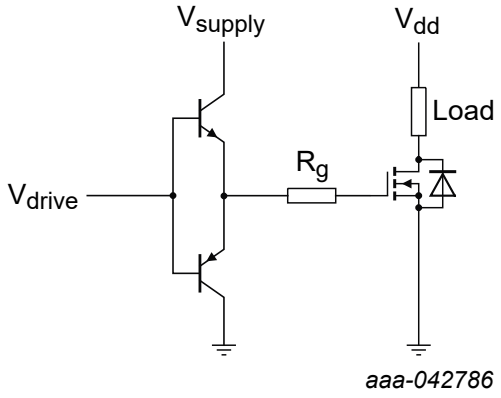


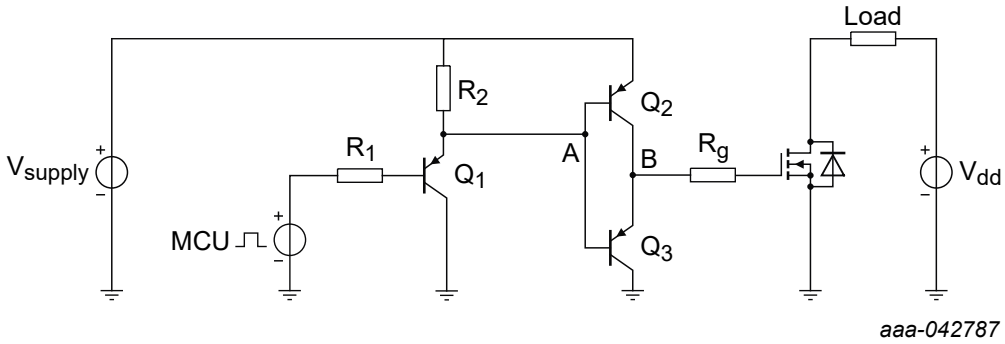
Fig. 15. Bipolar totem-pole driver

When switching the MOSFET on (for example, V_{drive} is logic high), V_{GS} is:

$V_{GS}=V_{drive}-V_{BE(NPN)}$

$V_{BE(NPN)}$ is usually around 0.7 V. Supplying V_{drive} directly from an MCU results in a weak V_{GS} (for example, V_{GS}=5 V - 0.7 V = 4.3 V or V_{GS}= 3.3 V - 0.7 V = 2.6 V). This might be acceptable for driving logic level MOSFETs. To achieve a higher V_{GS} for driving standard level MOSFETs, a few more components are required to provide a voltage level shift. An example is shown in Fig. 16.

When switching the MOSFET on in this circuit, the base of the BJT pair is supplied with 15V from V_{supply} and this allows for a logic high V_{GS} of around 14.3V. NPN Q1 is used to pull the BJT pair base to ground. Resistor R1 is necessary to limit the current drawn from the MCU. It is possible to drive a standard level MOSFET from most MCUs with this circuit and it allows for fast switching. Note that this is an inverting circuit (i.e. a low input from MCU turns on the MOSFET and vice versa).



$R_1 = R_2 = 1000\ \Omega$

Fig. 16. BJT totem pole driver with level shift stage

One useful trait of the BJT totem pole is that there is no risk of shooting through current since it is not possible for both NPN and PNP transistors to be on at the same time. This is clear when we look at the possible voltages between node A and node B:

- $V_{AB} \leq -0.7$ V, only PNP on
- $-0.7\ V < V_{AB} < 0.7$ V, both BJTs off
- $V_{AB} \geq 0.7$ V, only NPN on

A drawback of this circuit is that the V_{GS} range is limited to around 0.7 V to Vsupply-0.7 V. A logic low V_{GS} of 0.7 V might be an issue if the MOSFET has a low minimum threshold or at high temperature where $V_{GS(th)}$ is reduced. The reduced V_{GS} range means that the switching is slightly slower compared to a rail-to-rail driver.

4.1.3. MOSFET totem-pole driver

A MOSFET-based totem pole driver can be implemented as shown in Fig. 17. A high side p-channel MOSFET is connected to a low side n-channel MOSFET in a common drain configuration with their gates tied together. This driver is similar to the BJT totem pole with some important differences. The MOSFET based driver can give full rail-to-rail gate drive voltage and its output stage is inverting. However, the downsides are that MOSFETs are more expensive than BJTs and they come with the risk of shoot through.

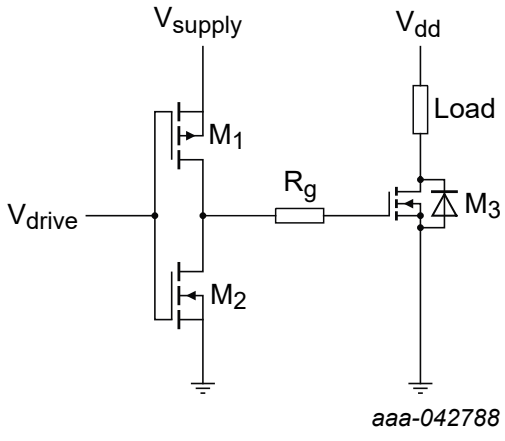


Fig. 17. MOSFET totem-pole driver

It is usually desired for the logic high output of V_{drive} to be equal to that of V_{supply} for switching off M1 (such that $V_{GS(M1)} = 0$ V). Applying 0 V V_{drive} turns M1 on ($V_{GS(M1)} = -V_{supply}$). Consequently, 0 V V_{drive} turns M2 off and V_{drive} logic high turns M2 on. A voltage level shift stage is likely to be required to get a V_{drive} voltage equal to V_{supply} from the control signal of an MCU. The logic states of the MOSFETs are described in Table 2.

Table 2. V_{GS} and logic state of each MOSFET based on V_{drive} as the input voltage

V_{drive}	V_{GS} of totem-pole pmos (M1)	V_{GS} of totem-pole nmos (M2)	V_{GS} of end MOSFET to be driven (M3)
Low = 0 V	-V_{supply} (on)	0 V (off)	V_{supply} (on)
High = V_{supply}	0 V (off)	V_{supply} (on)	0 V (off)

There is a risk of both MOSFETs in the totem pole being on at the same time when V_{drive} is transitioning logic state. This can cause large, undesirable shoot through currents which increase power consumption of the driver circuit and can damage the driver MOSFETs. This major drawback can be avoided by adding delay circuitry to ensure both MOSFETs are not conducting at the same time.

Because of the drawbacks mentioned above, the complementary MOSFET driver is rarely implemented using discrete components.

4.2. High-side driver circuits

4.2.1. P-channel MOSFET drive circuit

N-channel MOSFETs are usually a preferred choice over p-channel MOSFETs for the following reasons:

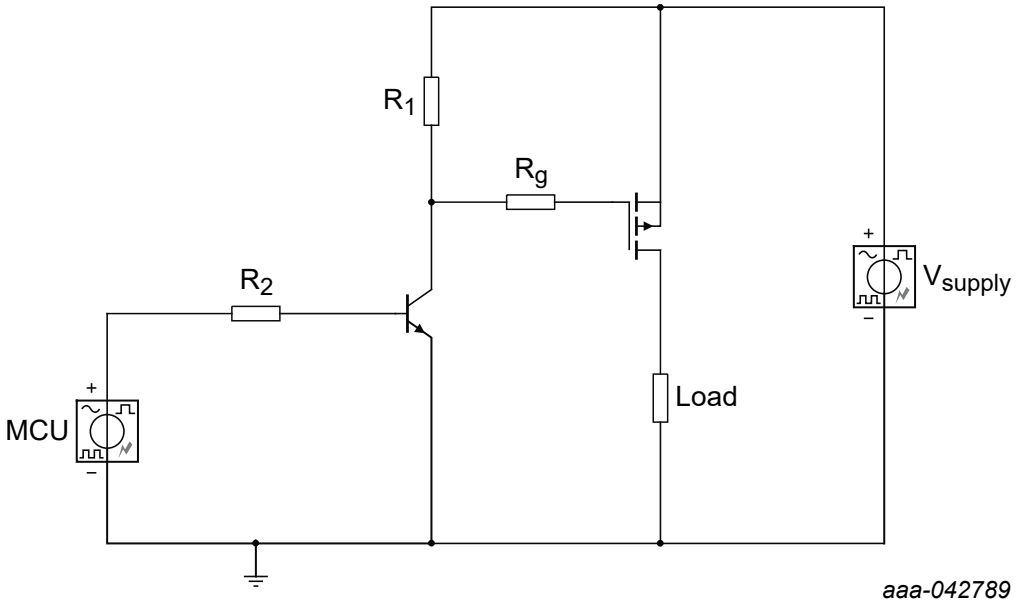
- n-channel MOSFETs are cheaper than equivalent R_{DSon} p-channel devices and can have lower R_{DSon} for the same die size, meaning that they can handle more current at a lower price
- n-channel MOSFETs have lower gate charge for a given R_{DSon} compared to p-channel.

P-channel MOSFET has an advantage over n-channel in terms of being easier to drive as high side device. Thus, p-channel MOSFETs are typically only used as high side switches and in low frequency applications which don't require high current handling.

A simple drive circuit involving a voltage level shift stage is shown in Fig. 18. The MCU output switches the NPN of the level shifter which determines whether the gate of the p-channel is pulled to ground or V_{supply}. If a low value R_G is used, the turn-on of the p-channel is quick since the NPN can sink a lot of current. However, the turn-off gate current is limited by R1, which is usually quite large, meaning the turn-off is slow for this circuit and it is not suitable for high-speed switching.

Note: V_{supply} must be less than the maximum V_{GS} rating of the MOSFET.

While the NPN is on, current flowing through level shifter is $I_{R1} = (V_{supply} - V_{CE})/R1$ and the power dissipated on R1 is $P_{R1} = (V_{supply} - V_{CE})^2/R1$. Thus, reducing R1 increases the turn-off speed of the MOSFET but dramatically increases the power consumption of the driver circuit.

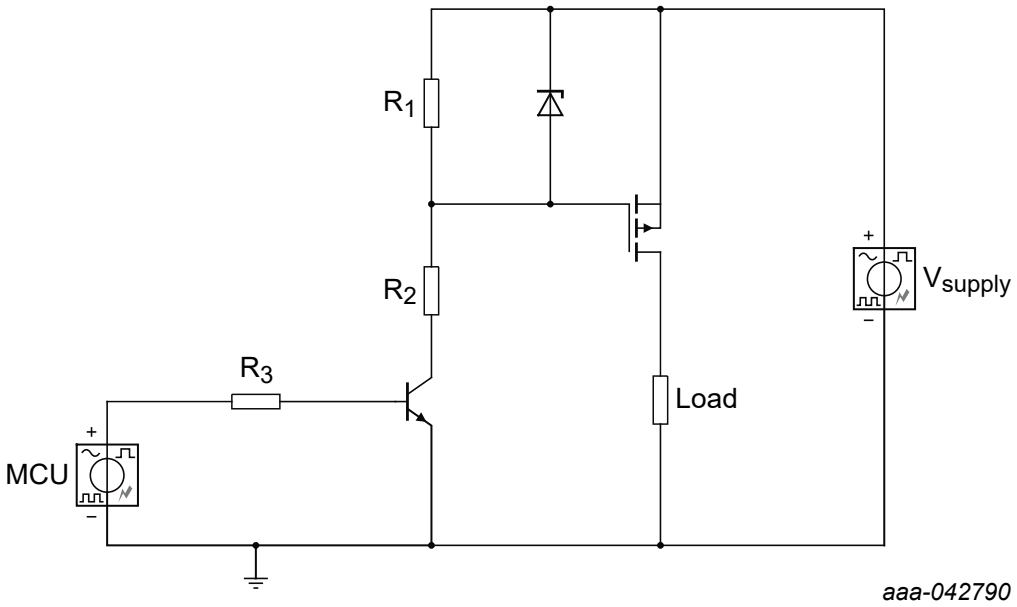


$R_1 = R_2 = 1000\ \Omega$

Fig. 18. Driver circuit for p-channel MOSFET

To improve the switching speed without increasing the power consumption of the driver circuit, a BJT push-pull stage can be implemented to increase the source/sink current. However, it is uncommon for this to be implemented in practice since n-channel MOSFETs are usually chosen over p-channel MOSFETs for switching applications.

To protect the MOSFET from gate-source over-voltages, a Zener diode can be placed between the gate and the source (see Fig. 19). This is necessary if V_{supply} is outside the V_{GS} limits of the MOSFET. Resistor R2 limits the current and power dissipation on the Zener diode. Both resistors will likely be in the kΩ range, meaning that the circuit is only suitable for near DC operation since switching times are slow.



$R_3 = 1000\ \Omega$

Fig. 19. Driver circuit for p-channel MOSFET with V_{GS} protection

4.2.2. Using N-channel MOSFET as a high side device

As mentioned in the previous section, there are some difficulties that come with using an n-channel MOSFET as a high side switch. It can be seen from Fig. 20 that if the MOSFET is on then V_{dd} is observed at the source of the MOSFET. Therefore, to keep the MOSFET on, V_{drive} needs to be larger than V_{dd} (since $V_{GS} = V_{drive} - V_{dd}$). Hence, there are driver circuits designed specifically for driving high side MOSFETs, for example, Section 4.2.3 and Section 4.2.4.

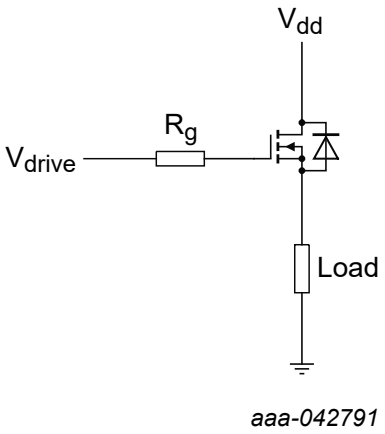


Fig. 20. N-channel MOSFET as a high side switch

4.2.3. Bootstrap

The bootstrap technique is a simple and cost-effective way of driving a high side MOSFET and involves adding two main components: a bootstrap diode and a bootstrap capacitor, see Fig. 21.

When the high side FET is off, current from V_{supply} flows through the diode and capacitor, charging the capacitor to V_{supply} (minus diode V_F). V_{supply} does not need to be larger than V_{dd}. If necessary, a resistor can be placed in series with the capacitor to limit the current during start-up.

As the high side MOSFET switches on, the potential at its source pin rises to V_{dd}. Since the voltage across the capacitor is around V_{supply}, the voltage at the top pin of the capacitor is now around $V_{supply} + V_{dd}$ and the bootstrap diode becomes reverse biased. The bootstrap capacitor acts as a floating voltage supply for the high side driver circuit for the duration that the MOSFET is on.

Since the bootstrap capacitor has limited capacity, it will lose some of its charge and its voltage begins to drop if it does not get re-charged. Hence, it is necessary to switch the MOSFET off regularly. The frequency depends on the value of capacitance, capacitor voltage and how much current is drawn while the MOSFET is on (including leakage current). So, there is a minimum allowed switching frequency and a maximum allowed duty cycle. A larger value capacitor is required when operating at lower switching frequencies or higher duty cycles or both.

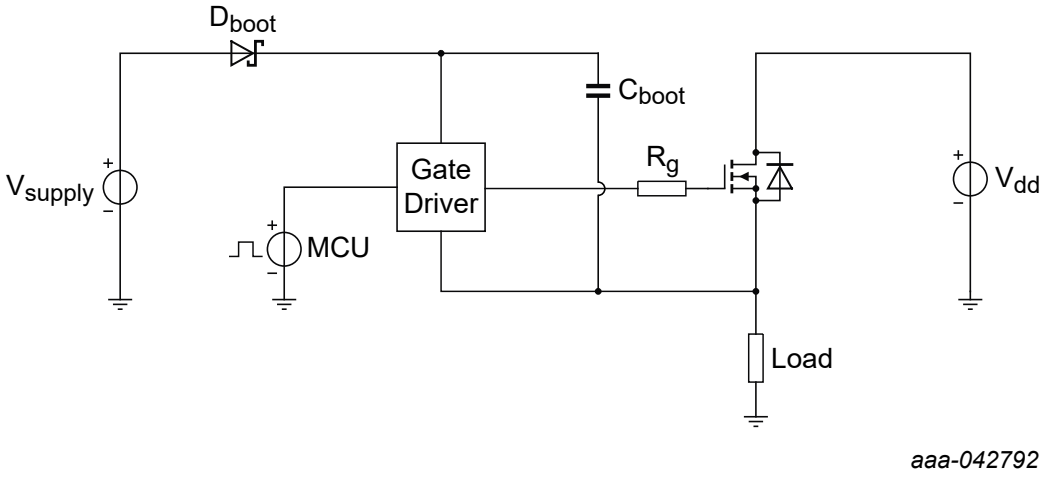


Fig. 21. Bootstrap high side driver circuit

Because of the switching requirements, the bootstrap circuit is usually implemented in switching applications that have a low side FET, for example, half-bridge, H-bridge, inverter, etc., which pulls the bottom pin of the capacitor to ground for recharging, see Fig. 22.

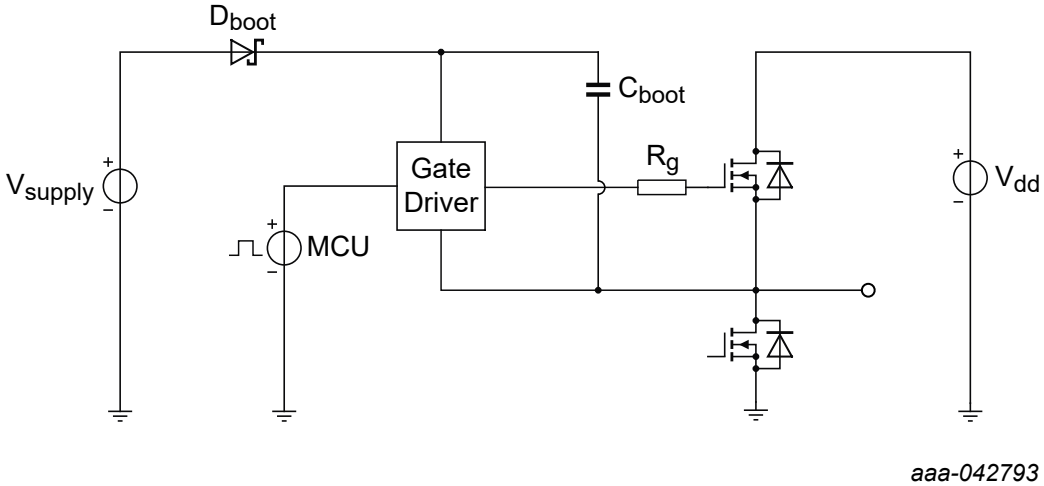


Fig. 22. Bootstrap used to drive high side FET in a half-bridge

4.2.4. Charge pump

A charge pump circuit can be used as an alternative to bootstrap or in situations where a bootstrap driver cannot be used. For example, if the duty cycle is too high, or switching frequency is too low, or if the low side component does not allow for sufficient charging of the bootstrap capacitor. The charge pump uses a similar principle to bootstrap since they both use capacitors to boost the voltage level.

Fig. 23 shows the charge pump circuit. It consists of two diodes and two capacitors. The key feature of the charge pump is that C_{tank} is used to supply the boosted voltage for the driver circuit, and C_{pump} is used to charge and maintain the charge in C_{tank}.

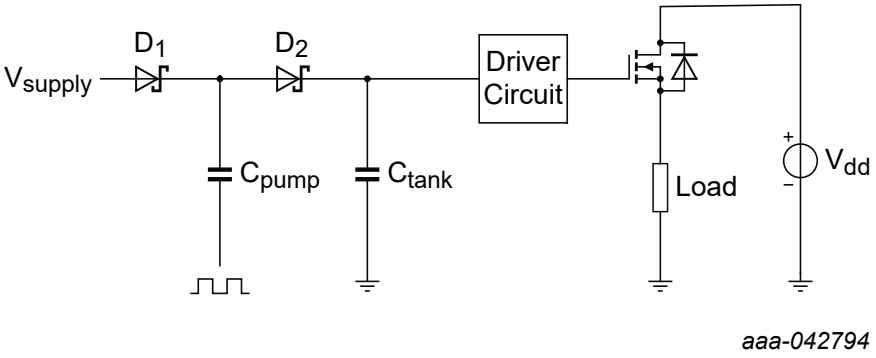


Fig. 23. Charge pump high side driver circuit

Diode voltage drops are ignored for this explanation. A digital signal with 50% duty cycle and amplitude equal to V_{supply} is applied to the bottom pin of C_{pump}, switching between ground and V_{supply}. While the digital signal is low, C_{pump} is charged from V_{supply} through diode D1 so that the voltage across C_{pump} is equal to V_{supply}. When the digital signal goes high, the voltage at the top pin of C_{pump} jumps up to around $2*V_{supply}$ since the voltage across C_{pump} is still V_{supply}. Now D1 is reverse biased and C_{pump} charges C_{tank} through diode D2 to a voltage of $2*V_{supply}$. Hence, the charge pump circuit can be used for voltage multiplication.

In practice, the C_{tank} voltage is not exactly equal to $2*V_{supply}$ due to diode voltage drops. The diode drops can be minimized by using Schottky diodes.

Contrary to the bootstrap, the advantage of charge pump is that it has no minimum frequency or maximum duty cycle limitations. However, it requires more components and complexity. If the gate drive voltage supply is not large enough, additional charge pump stages can be implemented.

A more complete and robust usage of the charge pump is shown in Fig. 24. This circuit uses a level shift and BJT push-pull circuit to supply the square pulse to C_{pump}. A voltage regulator is placed after the charge pump to regulate the V_{GS} to around 11 V by using a 12 V Zener diode D3. Then a UVLO (under-voltage lockout) stage is used so that the MOSFET does not switch unless there is a suitable amount of gate drive supply voltage – the gate drive supply voltage is kept below MOSFET's threshold until the output of the voltage regulator reaches about 10 V by using a 9V Zener diode D4. Another level shift and BJT pair is used for sourcing or sinking large currents to or from the gate for fast switching.

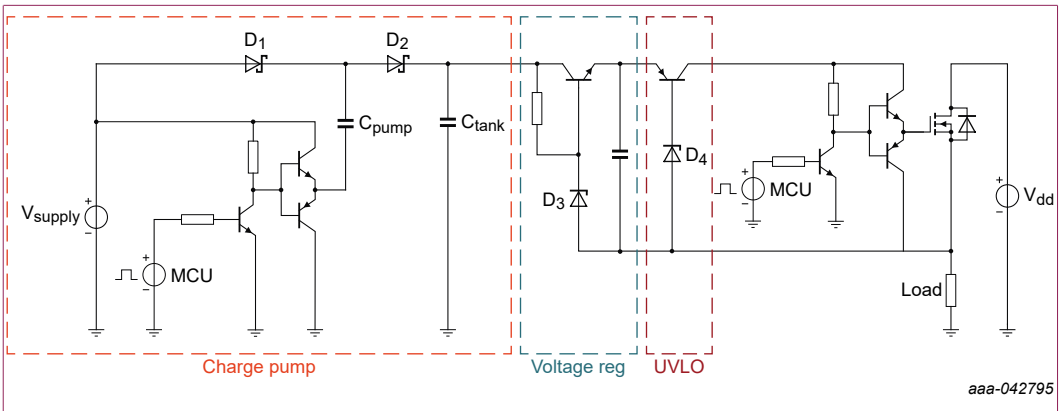


Fig. 24. Charge pump gate driver with V_{GS} regulation, UVLO and push-pull stage

4.3. Isolated gate driver circuits

In some cases when there is high voltage on the power switch side, for example 400 V or more, it is desired to have the control circuitry isolated from the power switch side to ensure its protection and as a safety measure to protect any operators interacting with the system.

The most common isolated gate drivers are transformer and optocoupler based. In addition to providing galvanic isolation (they can be rated to several kilo voltages of isolation), optocoupler

and transformer coupled gate drive circuits have the flexibility to drive either high side or low side MOSFETs since the secondary side can be floating and referenced to the source pin of the MOSFET.

4.3.1. Transformer-based gate drive

The types of transformers used in these circuits are called pulse transformers or gate drive transformers. They are often surface mounted and have a maximum volt-time rating. The volt-second product of the application must not exceed the rating of the transformer.

For example, if the switching frequency is 100 kHz, the duty cycle is 50%, and the voltage on primary coil is switching between -6 V and +6 V, then the volt-second product is 6 V*5 µs=30 Vµs. Therefore, the transformer must have a rating greater than 30 Vµs to avoid saturation of the magnetic material.

To build an understanding of its operation, a transformer based gate driver is shown in Fig. 25. In this example, a square pulse V_{drive} is switching between 0 V and $+V_{drive}$. DC blocking capacitor C1 is needed on the primary side to ensure that the average voltage on the primary coil is zero. The volt-second product of the positive pulse must be equal to the volt-second product of the negative pulse, for example, area under voltage waveform is zero. If the average voltage across the primary coil is not zero, then the current through it would continue to drift until the coil reached saturation. A low value resistor R1, for example, a few ohm, is included on the primary side to provide damping.

With the DC element removed, we are left with an AC square pulse on the primary coil, which is induced onto the secondary coil. It is sometimes desired to restore the square pulse back to its original form. A DC restorer can be used for this purpose. This consists of the capacitor C2 and diode D1 on the secondary side. During the negative pulse, C2 gets charged through the forward biased diode. The voltage across C2 adds to the AC square pulse from the secondary coil. This adds the offset required to restore to its original DC square pulse form.

This circuit can have some trouble with primary side resonance during startup. Driving the primary coil with an AC square pulse, for example, with an H bridge, can avoid resonance issues since the DC blocking capacitor can be removed.

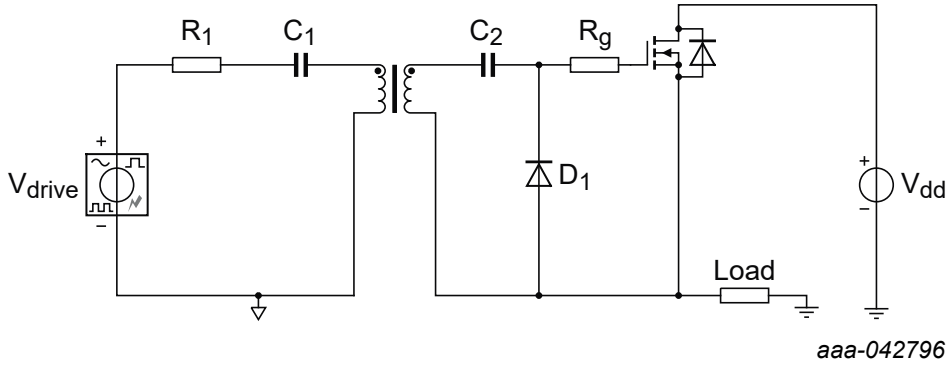


Fig. 25. Transformer based gate drive circuit

In some cases, the DC restorer is not needed and the MOSFET can be driven by an AC square pulse once the MOSFET's V_{GS} limits and requirements are adhered to.

In half bridge or H-bridge applications, a double ended transformer can be used. Therefore, we can have two secondary coils for one primary coil, meaning two MOSFETs can be driven from a single gate drive signal. One secondary coil is usually configured with opposite polarity so that only one FET in the half-bridge is switched on at a given time.

If using a PWM controller, it is possible to connect the primary winding across two PWM output pins and eliminate the need for the DC blocking capacitor (see Fig. 26). In the first half of the cycle, OUT1 is driving a square pulse voltage. In the second half of the cycle, OUT2 is driving a square pulse voltage. The primary coil therefore sees an AC square pulse with an average voltage of zero.

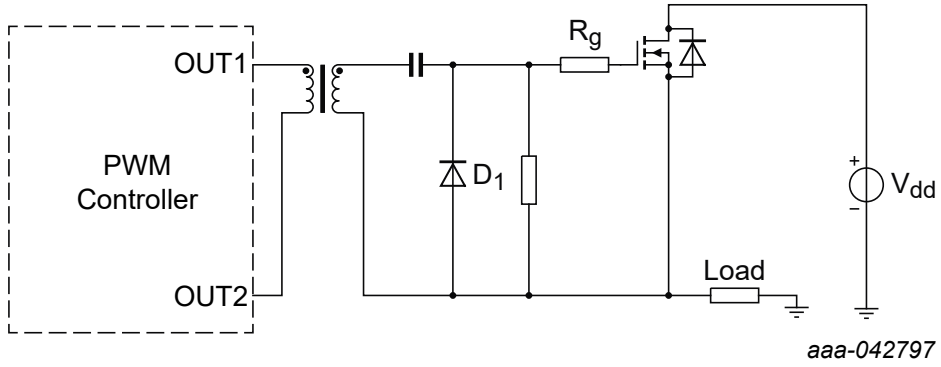


Fig. 26. Driving gate drive transformer with two outputs of a PWM controller

The turns ratio of the transformer can be used to multiply the voltage on the secondary side.

A downside of using the gate drive transformer is that there is a minimum frequency requirement, which is dependent on the size and volt-time rating of the transformer.

4.3.2. Optocoupler-based gate drive

Optocoupler-based gate drivers provide good isolation, but they have some limitations. Over time, the insulating material between the photodiode and phototransistor can degrade, reducing the phototransistor's ability to detect emitted photons and resulting in performance degradation.

Additionally, optocouplers are often slower devices, with propagation delays that can reach several microseconds. They also require a secondary-side voltage supply, which can be floating or boosted if driving a high-side FET.

One advantage of optocouplers over transformer-based gate drivers is their capability to drive both DC and switching applications.

Fig. 27 shows a typical optocoupler-based gate drive circuit using a BJT totem pole for faster switching. The optocoupler in this example features an open collector output.

When selecting an optocoupler, key parameters to consider include dV/dt and isolation ratings. A high dV/dt on the output side can induce current spikes due to the optocoupler's intrinsic capacitance, which may cause unwanted switching of the phototransistor. This issue is typically more prominent in high-side applications.

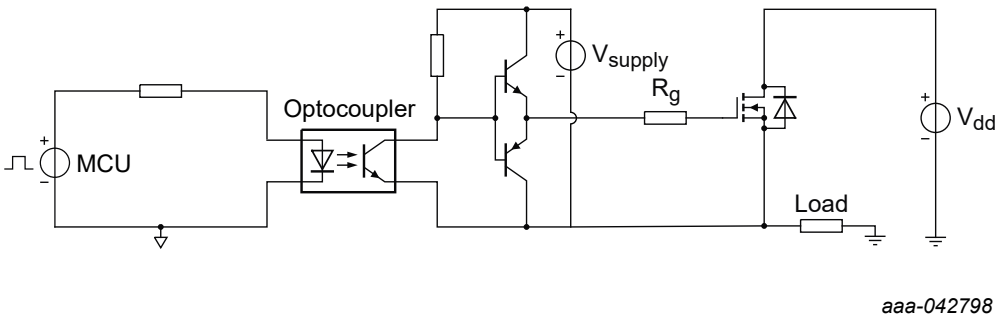


Fig. 27. Optocoupler-based gate drive circuit

5. Turn-off speed enhancement

In most applications, optimizing turn-off speed is more critical than turn-on speed, particularly in half-bridge or DC-DC converters. This is due to the reverse recovery current caused by the diode (or body diode) during turn-on. Faster turn-on increases the dI/dt, which leads to higher reverse recovery current. Additionally, turn-off is typically slower than turn-on when using a single gate resistance.

A simple method to improve turn-off speed is to use a lower gate resistance for turn-off than for turn-on. This can be achieved by placing a diode in series with a lower value resistor, as shown in Fig. 28. During turn-on, the gate drive circuit sees a resistance of RG_ON, while during turn-off, the resistance becomes RG_OFF in parallel with RG_ON. In some cases, RG_OFF can be set to 0Ω to maximize turn-off speed.

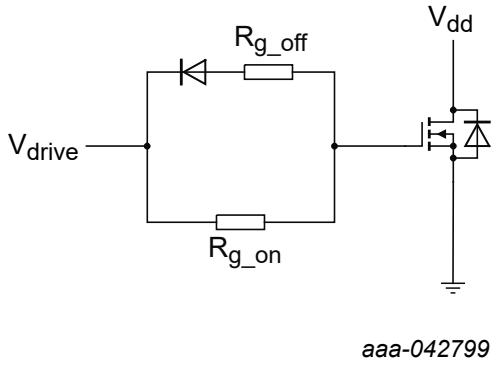


Fig. 28. Faster turn-off using low-value RG_OFF in series with turn-off diode

Some gate driver ICs feature separate output pins for turn-on and turn-off paths, allowing for a lower RG_OFF value compared to RG_ON without the need for a diode.

Another approach to speed up turn-off is to use a PNP transistor, as shown in Fig. 29. During turn-on, the gate current flows through RG_ON and the diode. When V_{drive} goes low, the PNP transistor turns on and pulls the current from the gate. This method reduces loop inductance by positioning the PNP transistor near the MOSFET. Note that the diode's forward voltage (V_F) reduces the logic high V_{GS} by approximately 0.7 V, and the PNP's base-emitter voltage (V_{BE}) causes the logic low V_{GS} to be around 0.7 V when V_{drive} is 0 V.

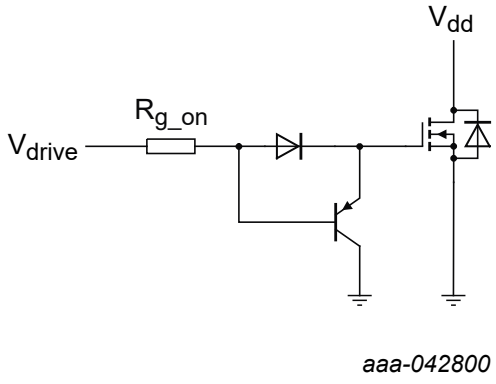


Fig. 29. Faster turn-off using pull-down PNP transistor

These turn-off speed enhancement circuits can be applied to both high-side and low-side MOSFETs.

6. Protection circuits

A pull-down resistor placed between gate and source ensures that the MOSFET is in a known state (off) in the case of a fault with the gate drive circuit or when there is no power being applied to the circuit (see Fig. 30). A gate-source resistance in the kΩ range is usually suitable.

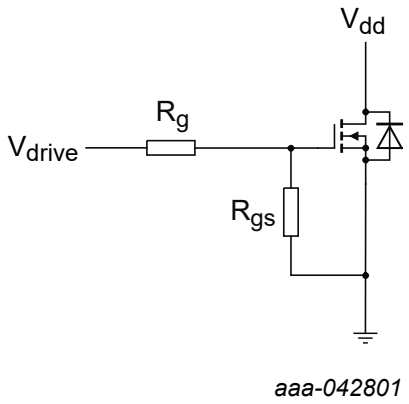


Fig. 30. Gate-source pull down resistor

To prevent gate-source overvoltage and keep the V_{GS} of the MOSFET within the limits given on the datasheet, one or more Zener diodes can be placed between the gate and source, see Fig. 31. Placing two Zener diodes back-to-back clamps both positive and negative V_{GS}. The Zener diodes add some capacitance which can impact switching times for small MOSFETs. For example, Zener diode BZX84-B15 has a maximum capacitance of 75 pF.

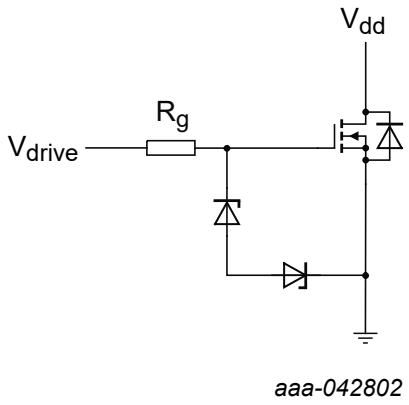


Fig. 31. Gate-source overvoltage protection

These protection circuits can be applied to either high side or low side MOSFETs.

During turn-off, there can be a risk of gate bounce (also known as self turn-on or dv/dt triggered turn-on). Gate bounce happens when a high dV_{DS}/dt causes a current to flow through C_{GD}. This current results in a rise in V_{GS} which can momentarily turn the MOSFET on again. This can cause large, undesirable shoot-through current in a half bridge. The risk of gate bounce can be reduced by adding an external C_{GS} or by reducing the gate drive impedance. The turn-off speed enhancement circuits described in the previous section can be implemented for this purpose. Refer to 3, 4, and 5 for details.

7. Summary

The MOSFET's intrinsic capacitance and gate charge parameters are crucial for understanding its switching process. In particular, the gate charge parameters indicate how long it takes for the MOSFET to switch, which is essential for determining switching losses.

A gate drive circuit is required to provide sufficient V_{GS} for switching the MOSFET on and off. Typically, a 10 V gate drive is used for standard-level MOSFETs, while a 5 V gate drive is used for logic-level MOSFETs. A higher V_{GS} applied to the MOSFET results in lower $R_{DS(on)}$—refer to the V_{GS} vs $R_{DS(on)}$ graph in the datasheet for more details.

The gate drive circuit must source and sink current to and from the gate of the MOSFET during switching events. A large peak gate current results in shorter switching times due to the fast charging and discharging of the input capacitance.

A gate resistor is typically placed on the gate of the MOSFET, and it can be used to control the switching speed. Increasing the gate resistance leads to a longer switching time. While a larger gate resistance can help reduce spiking and oscillations, contributing to improved EMC performance, slower switching results in higher switching losses because there is significant voltage and current present simultaneously during the switching event.

Another important consideration is the circuit layout. It is essential to minimize the area of the gate-source loop to reduce parasitic inductance. Parasitic inductance can cause voltage spikes and oscillations, which can lead to EMC issues.

The most common gate drive circuits, focusing on discrete components, have been discussed. These include low-side, high-side, and isolated gate drive circuits. Driving the MOSFET as a high-side device introduces the additional challenge of requiring a floating power supply or a boosted voltage supply.

For protection and safety, isolated gate driver circuits can be used when there is high voltage, such as 400 V or more, present on the power switch side. Additionally, isolated gate driver circuits can be used to drive either high-side or low-side MOSFETs since the secondary side can float.

Finally, methods to improve turn-off speed and provide protection were demonstrated.

8. References

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2. AN50005 Paralleling power MOSFETs in high power applications
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4. AN90001 Designing in MOSFETs for safe and reliable gate-drive operation
5. TN00008 Power MOSFET frequently asked questions and answers
6. Signal and Power Integrity - Simplified, Eric Bogatin, 2017
7. Fundamentals of Power Semiconductor Devices- B. J. Baliga

9. Revision history

Table 3. Revision history

Revision number	Date	Description
1.0	2025-04-22	Initial version.

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