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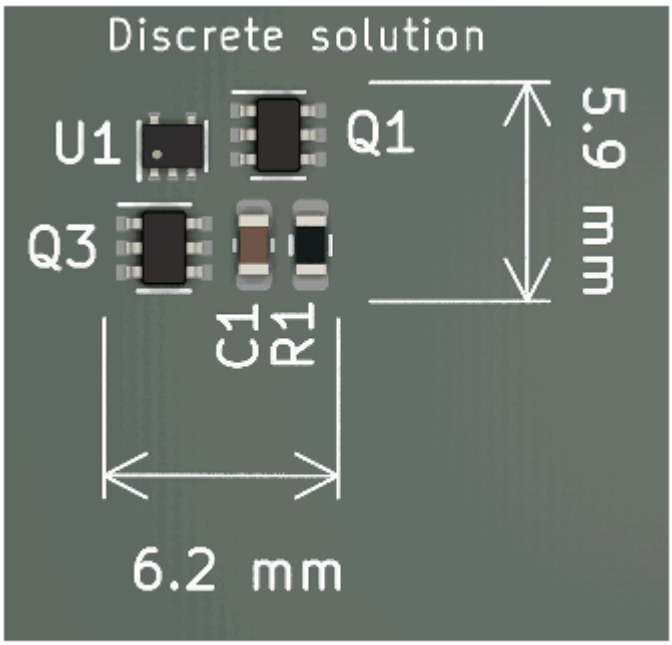
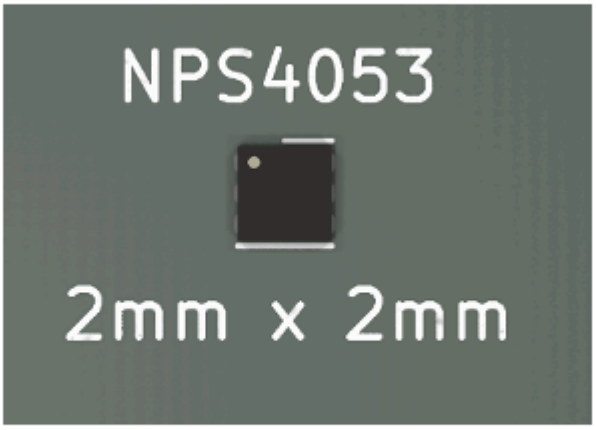
Application note

Nexperia load switch ICs compared to discrete solutions





Abstract: This application note compares integrated and discrete load switches used in electronic circuit design. Integrated load switches offer a consolidated solution with a smaller footprint, simplified design, and potential cost savings compared to discrete load switches. The note considers the trade-offs associated with each approach, offering practical insights and real-world examples to guide designers in selecting the most appropriate solution for their specific applications.

Keywords: Load switch, NPS4053, Discrete switch

nexperia

1. Introduction

In electronic circuit design, the choice between discrete and integrated power switches is a pivotal decision that significantly influences the performance, efficiency, and overall footprint of a system design.

A typical system design will likely be comprised of a DC power source and one or more loads each with varying current requirements. Typically, the system needs to manage the activation timing and speed of each load dynamically. This can either be done using discrete components, or an integrated circuit. Fig. 1 shows an example of a system with a power switch controlling a load, (e.g. an external USB, HDMI or display port).

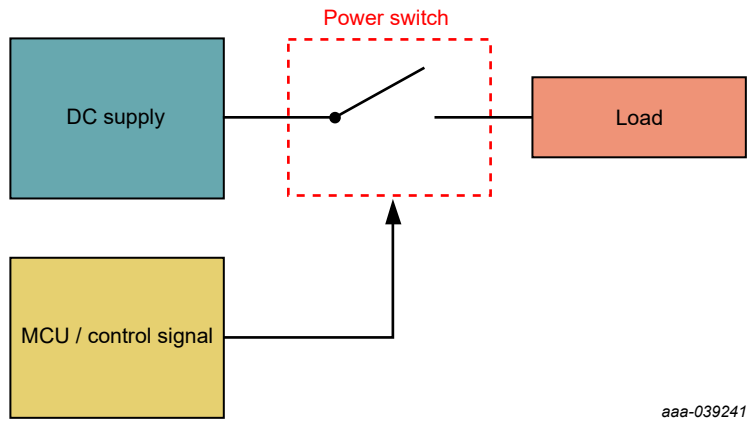


Fig. 1. Power switch in a system design

1.1. Discrete load switch implementations

Fig. 2 shows two discrete implementations of load switch circuits that contain several components to control the gate of a discrete power MOSFET from a microcontroller or control circuit. NMOS FETs and PMOS FETs can both be used to achieve power switching to a load, and each have their own distinct advantages and disadvantages. For instance, PMOS load switches typically do not require a charge pump to control their gate, which results in a lower quiescent current. In comparison, NMOS FETs are typically smaller in size and in cost, as well as typically operating at lower VIN voltages than PMOS load switches.

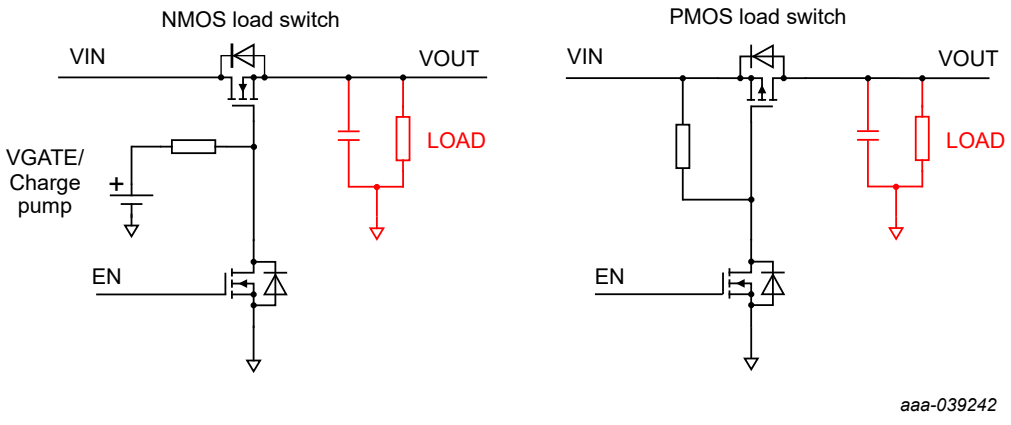


Fig. 2. NMOS and PMOS discrete load switch circuits

1.2. Integrated load switch implementations

An integrated load switch combines various functions related to power management within a single integrated circuit (IC). These devices are designed to simplify the control and distribution of power within electronic systems. The integrated load switch often includes features such as over-current protection, thermal shutdown, and input/output voltage control.

The primary purpose of an integrated load switch is to enable efficient and controlled switching of power to specific loads or circuits within a larger electronic system. Load switch ICs are commonly used in applications where precise control over power distribution, along with protection features, is essential. The integration of multiple functions into a single IC contributes to space savings, ease of implementation, and improved overall system reliability.

Integrated load switches find applications in a variety of electronic devices, ranging from consumer electronics to industrial equipment. Fig. 3 shows how an integrated load switch can fit into a system design.

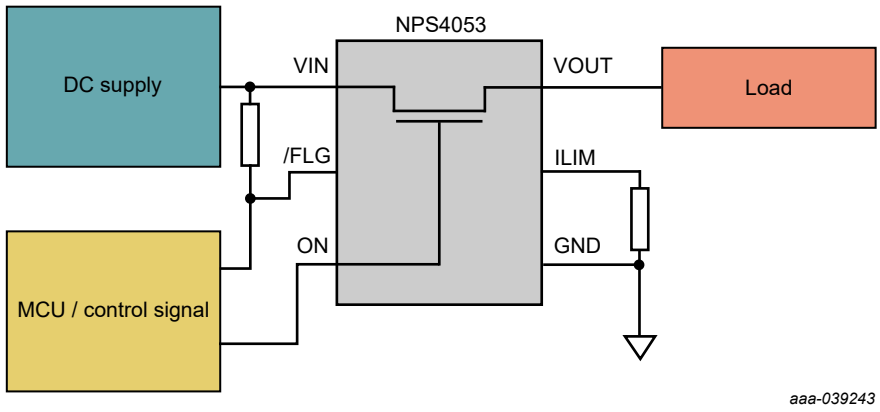


Fig. 3. Integrated load switch design using NPS4053

1.3. Load considerations for each implementation

When selecting a load switch for a system design it is important to consider the amount of inductance, capacitance, and resistance in the load that is being switched. Integrated load switches are excellent at switching the power on and off to loads that are resistive and capacitive but lack the ability to protect against back-EMF for large inductive loads. This back-EMF can lead to voltage spikes that exceed the voltage rating of the load switch, potentially causing damage. Integrated load switches can be used to drive light inductive loads; however, they are typically not recommended to switch inductive loads unless additional protection devices are used such as a flyback diode. As long as the power rating of the integrated load switch is observed and the amount of inrush current is considered, integrated load switches are excellent candidates switching resistive (R) and capacitive (C) loads.

In comparison to integrated load switches, discrete implementations can be designed to handle resistive, capacitive, and inductive loads. To handle inductive loads, discrete switches can be outfitted with a V_{DS} clamp (typically a Zener diode) connected from the gate to the drain of the pass FET. A V_{DS} clamp operates to prevent back-EMF by clamping the voltage to a predefined safe level. This configuration is referred to as a high-side switch, commonly used to switch inductive loads Fig. 4 shows a load switch design with a V_{DS} clamp.

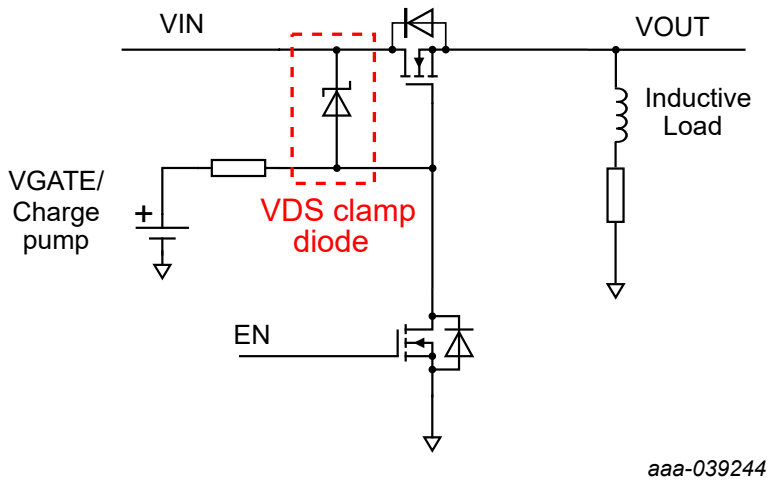


Fig. 4. Discrete switch with VDS clamping diode

2. Integrated load switch features

Integrated load switches offer a consolidated solution with built in features such as under-voltage lockout (UVLO), thermal shutdown, reverse current blocking, quick output discharge (QOD), and much more. This integration facilitates space-efficient designs and simplified implementation, contributing to overall system reliability. While discrete solutions can also include these features along with a high degree of customization, they may require more intricate designs and lack the streamlined features inherent in integrated load switches.

2.1. Under-voltage lockout (UVLO)

Under-voltage lockout is an electronic circuit used to turn off the power to an electronic device in the event of the input voltage dropping below the operational value that could result in unpredictable system behavior. The UVLO function compares VIN with the internal reference voltage as shown in Fig. 5. When VIN reaches the under voltage lockout low level voltage, the comparator output toggles, turning off the output of the load switch IC. When VIN rises back above the UVLO voltage + hysteresis voltage, the comparator output toggles again, turning the IC's output back on.

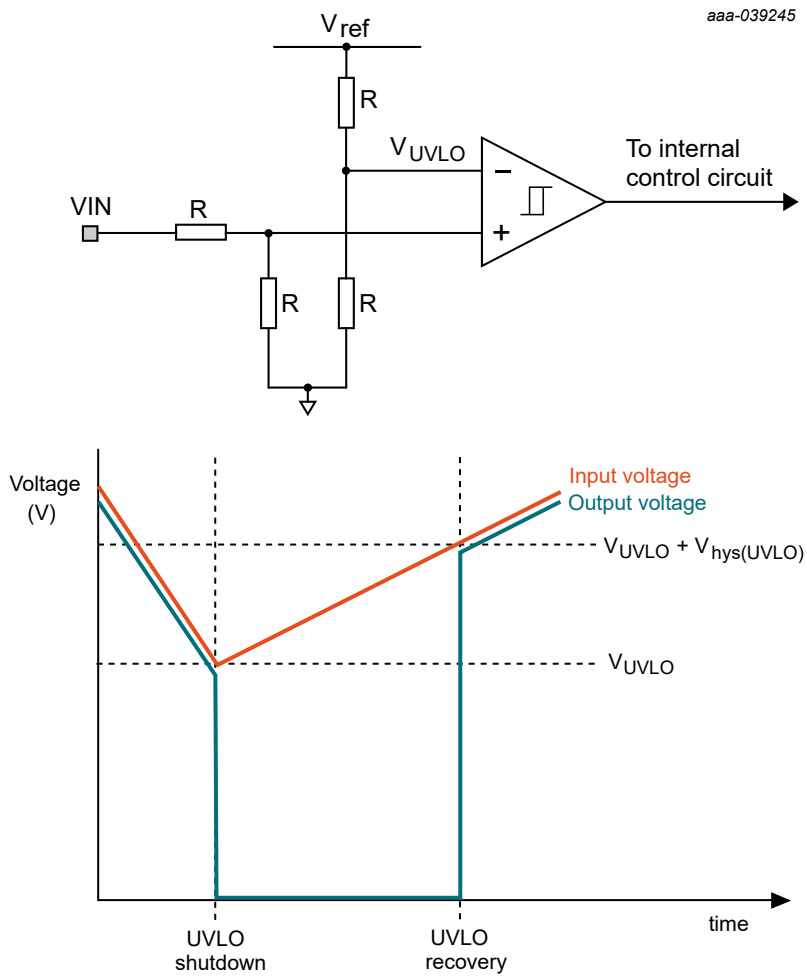


Fig. 5. Under-voltage lockout circuit and timing diagram

2.2. Over temperature protection (OTP)

An over temperature protection (OTP) circuit protects a load switch IC by detecting the internal junction temperature. The OTP circuit turns off the load switch IC when the junction temperature reaches an internally set trip point due to a sharp increase in ambient temperature or self-heating caused by an over-current condition.

An internal diode is used as the temperature sensing element, the diode V_F reduces with increasing temperature. When the OTP set point is reached, the load switch IC turns off its output to reduce power consumption, thereby reducing the junction temperature. When the junction temperature falls to the internally set recovery point, the OTP circuit is disabled allowing the output of the load switch to turn on again. Fig. 6 below shows a typical internal circuit used to implement OTP in a load switch IC:

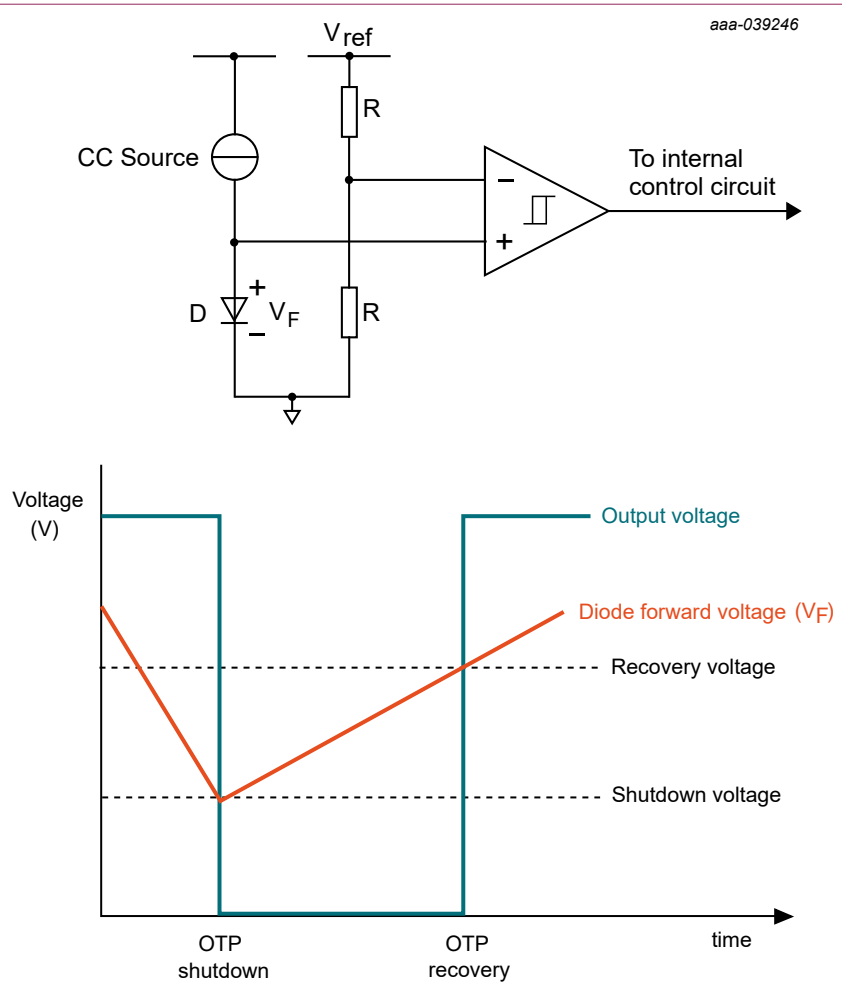


Fig. 6. Over temperature protection circuit and timing diagram

2.3. True reverse current blocking (TRCB)

In many power chain designs, the DC-to-DC converter supplying power to the load is not able to sink current. Since load switches connect the output to the input with a pass FET, it is possible that the connected load at the output causes a rise in voltage greater than VIN. This causes current to start flowing in the reverse direction which can damage upstream devices including the DC-to-DC converter.

A true reverse-current blocking (TRCB) function prevents reverse current from flowing from the output terminal to the input terminal regardless of whether the pass FET is on or off. In many TRCB designs, the body diode of the pass FET is mitigated by controlling the back gate of the FET or by using multiple FETs in series to prevent current flow in the reverse direction when the device is off.

Fig. 7 shows another common method that integrated load switches use to protect devices from reverse current. When the output voltage rises above the input voltage by a set threshold, the comparator monitoring the input and output will assert, and after a small de-glitch period, the driver controlling the pass FET will turn the pass FET off. This feature can be particularly useful for ORing power supplies.

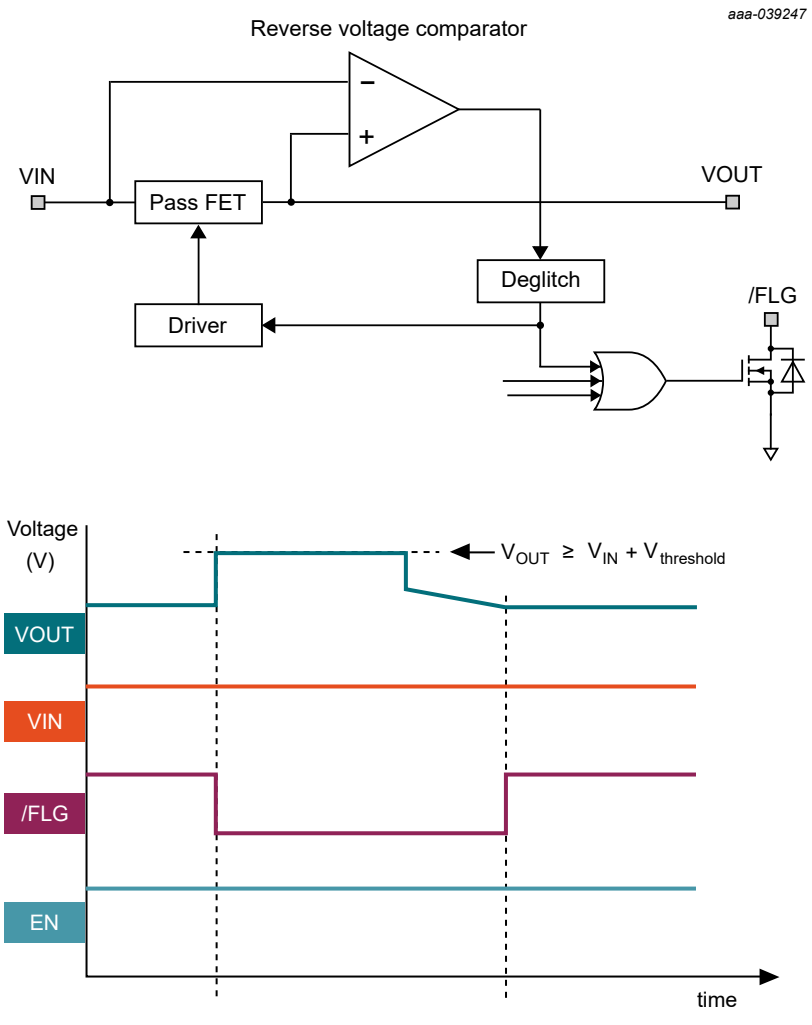


Fig. 7. Common reverse current blocking circuit and timing diagram

2.4. Quick output discharge (QOD)

Quick output discharge is a feature in load switches that will rapidly discharge the output when the enable pin is toggled to turn the device off. When the device is turned off, the output voltage is quickly disconnected from the input voltage and is discharged through a resistive path to GND. The timing of the discharge is proportional to the resistance of the QOD MOSFET and the capacitance at the output of the device. A useful equation is shown below to show the decay of the output as the quick output discharge circuit turns on after the device has been disabled.

$$V_{OUT} = V_{IN} \times e^{\left(-\frac{t}{R_{QOD} \times C_{LOAD}}\right)} \quad (1)$$

where:

V_{OUT} = output voltage of the load switch (V)
t = time since disable (s)
R_{QOD} = resistance of quick output discharge circuit (Ω)
C_{LOAD} = load capacitance (F)

It is important to note that the quick output discharge circuit is only present if the input voltage, and bias voltages are within the correct operating ranges of the device specs. If the input voltage and/or bias voltage are out of range, the quick output discharge circuit is not guaranteed to work.

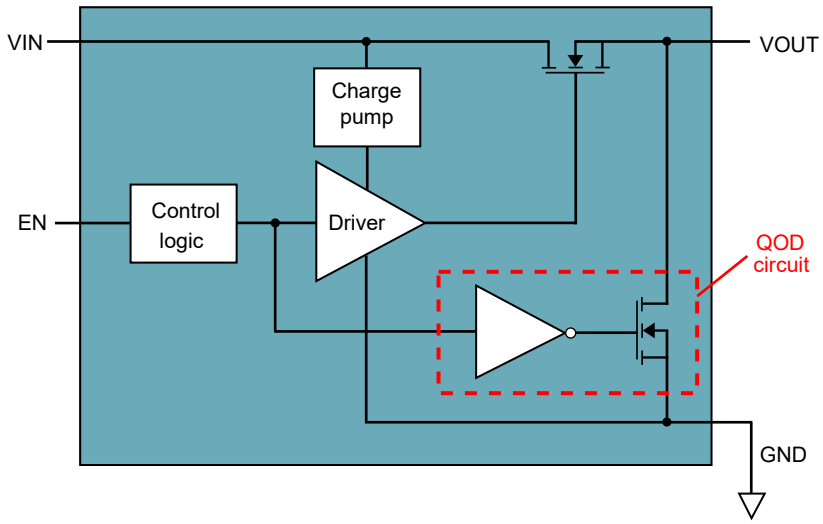
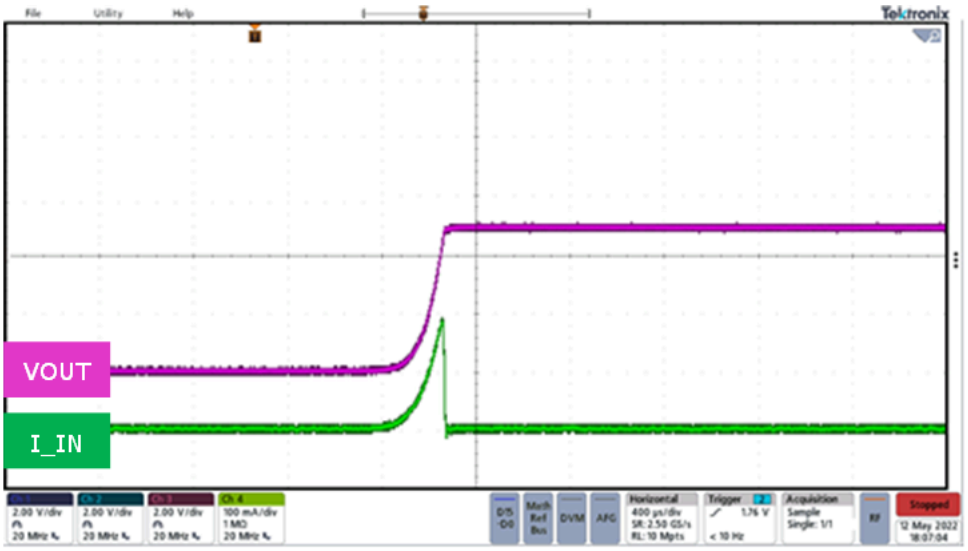


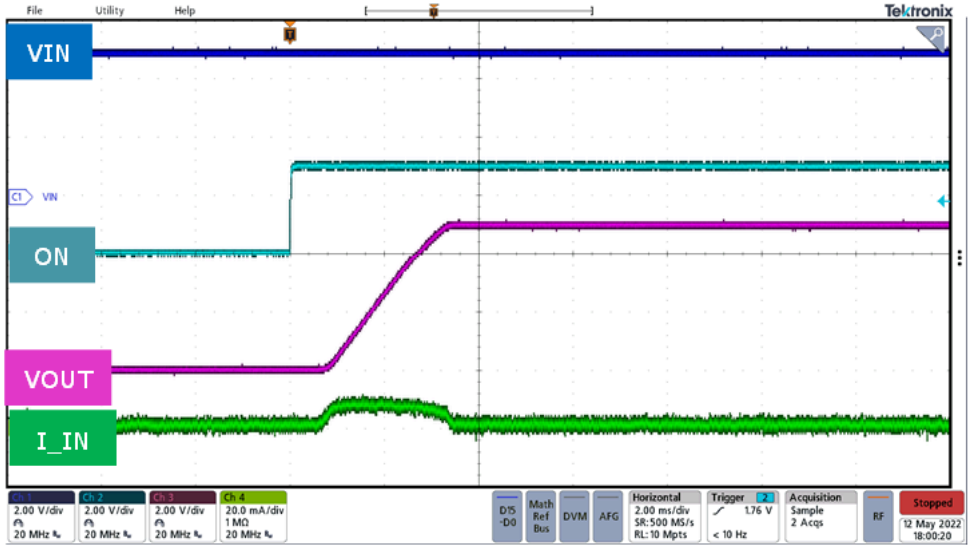
Fig. 8. Simplified load switch IC with quick output discharge functionality

2.5. Soft start

A soft start circuit in an integrated load switch circuit refers to a feature designed to control the inrush current when the load switch is first turned on. It minimizes large start-up currents from flowing to the load by turning on of the pass FET slowly to avoid stressing connected loads. For integrated switches that have a soft start feature, the output voltage will rise at a linear rate, reducing the amount of inrush current that flows through the device. Integrated circuits with soft start features will either have them built into the IC for a predetermined rise time, or they can be programmable via a pin and an external capacitor to GND. The differences in rise time between circuits with and without soft start can be seen below in Fig. 9.



a) discrete load switch turn-on



b) load switch IC with soft start turn-on

Fig. 9. Comparison of load switch turn-on

3. Discrete load switch overview

When evaluating the performance of integrated versus discrete load switches, several key aspects must be considered. Integrated load switches typically offer superior compactness, integrating control and protection features within a single package, which is advantageous in space-constrained applications. They usually have lower on-resistance and better efficiency, translating to lower power losses and heat generation.

Discrete load switches on the other hand, while they generally take up more board area and have higher on-resistances, provide greater design flexibility. They allow for the customization of components to specific application needs, such as selecting a MOSFET with a particular on-resistance or adding specific protection features. This can lead to optimized performance in applications where the size is less critical, and specific requirements are more pronounced.

Overall, the choice between integrated and discrete load switches often hinges on the trade-off between space-saving and efficiency versus customization and flexibility.

3.1. Common discrete load switch implementations

A very common implementation of a discrete load switch circuit is shown in Fig. 10. This load switch utilizes a PMOS FET with a pull-up resistor to VIN. An additional NMOS FET is used to control the turn-on of the PMOS FET controlling voltage to the load.

The advantage of this load switch implementation is its simplicity and its ability to be customized. However, this circuit also has its disadvantages. One of the disadvantages is that a persistent leakage current flows from VIN to the ground through the pull-up resistor when the NMOS FET is ON. Another important disadvantage of this discrete implementation occurs when this circuit is turned ON. After the circuit is turned ON, a significant inrush current flows through the pass FET, resulting in a drop in the input voltage. Lastly, when the device is powered off, there is a path for reverse current to flow into the input through the body diode of the pass FET. This reverse current could potentially damage devices connected to the input of this discrete implementation.

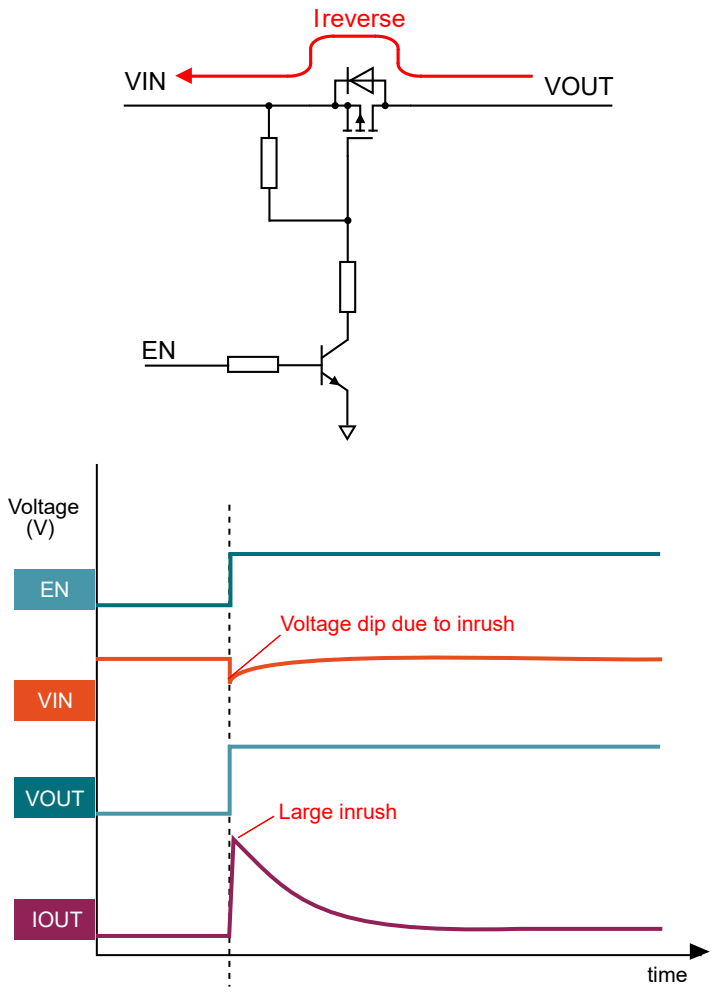


Fig. 10. Active high PMOS discrete load switch circuit and timing diagram

An alternative discrete approach to controlling inrush current involves positioning a capacitor on the input side. This is achieved by attaching a capacitor between the source and the gate of the PMOS FET, thereby generating an R×C delay that diminishes the inrush current and decelerates the switching speed of the PMOS FET. Additionally, incorporating a resistor between the gate of the PMOS and the bottom transistor helps to further reduce the output rise time which further reduces inrush. It is important to note that adding the R*C delay to the circuit causes the output voltage and consequently the inrush current to rise non-linearly. Another disadvantage that is carried over from the previous discrete configuration is the path through the body diode of the pass FET when the MOSFET is OFF. This configuration does not protect from reverse currents when the pass FET is OFF. The design and typical performance characteristics are shown in Fig. 11 below.

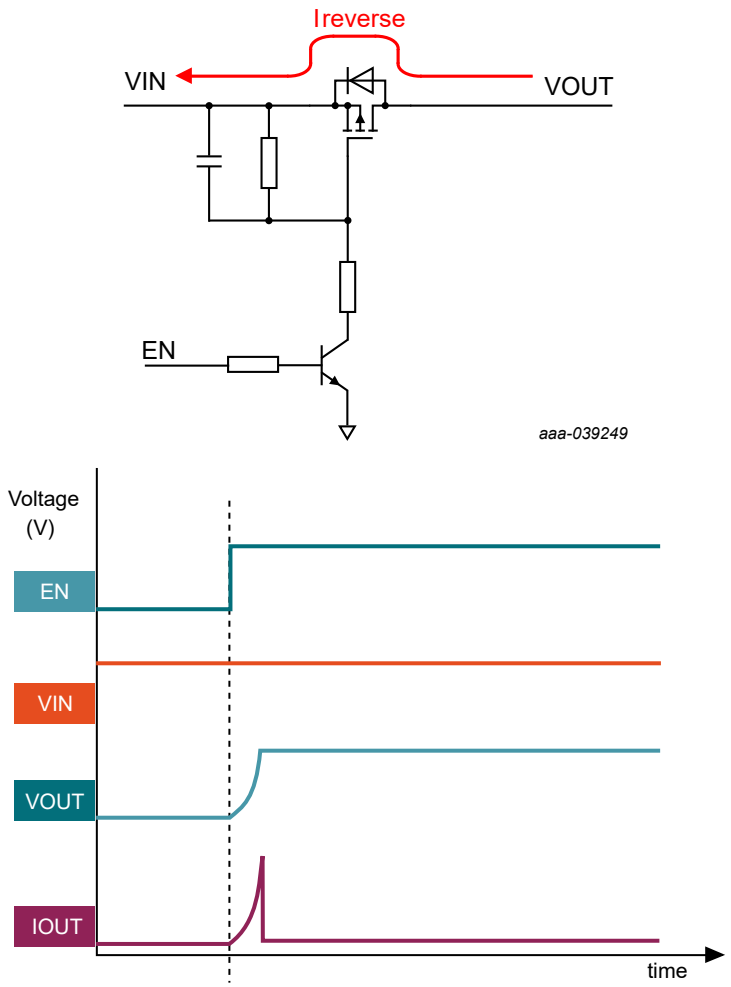


Fig. 11. Active high PMOS discrete load switch circuit with inrush control and timing diagram

3.2. Multi-featured discrete load switch circuit

Discrete load switch solutions typically only include features required by the system design. Implementing features in a discrete solution that are not used by the system design adds significant cost and limits space. For example, if the designer want to implement a discrete load switch solution with reverse current blocking and quick output discharge, the designer may use a solutions similar to the circuit shown in Fig. 12.

This solution uses back-to-back MOSFETs to block the flow of current in the reverse direction when the MOSFETs are turned off. It is important to note that this configuration does not protect from reverse current when both MOSFETs are turned on. Each MOSFET has an intrinsic body diode, and these diodes are oriented in such a way that one diode will block reverse current when the other is forward-biased. This allows the design to protect the supply on the input side of the load switch. Additionally, for quick output discharge, an NMOS FET can be positioned on the output of the discrete solution with its gate controlled by an inverter that is toggled by the enable signal.

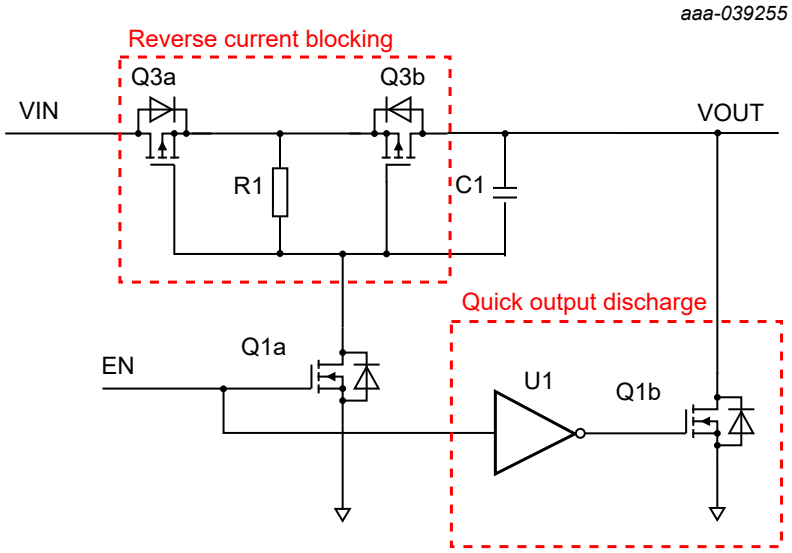


Fig. 12. Multi-feature discrete load switch solution

The discrete solution shown in Fig. 12 contains two of the features shown in the integrated load switch solution. One of the main draw backs of incorporating features like this into a discrete design is the size on the PCB, and an increase BOM cost due to the additional components needed to implement the features.

Fig. 13 shows the size of this discrete design compared with Nexperia's integrated load switch IC NPS4053. In discrete solutions, the amount of features added is directly proportional to the board area consumed.

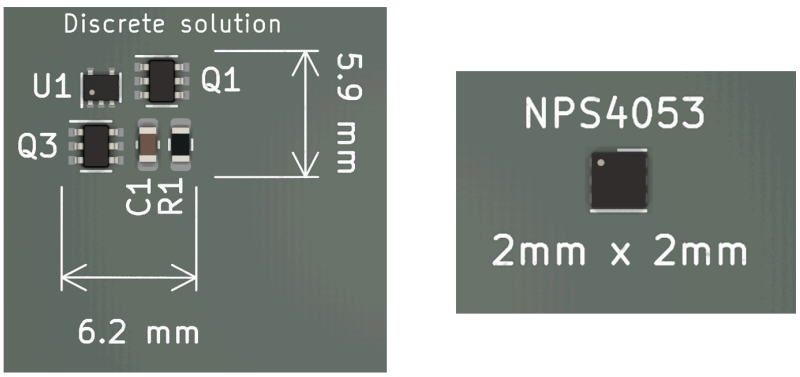
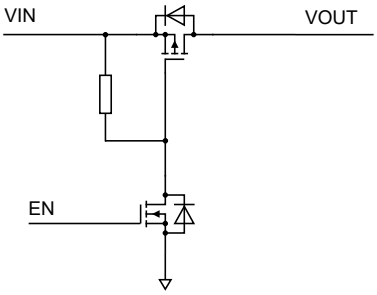
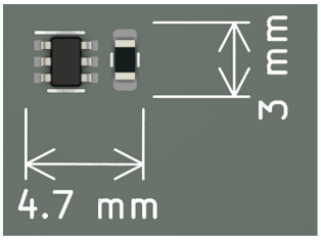
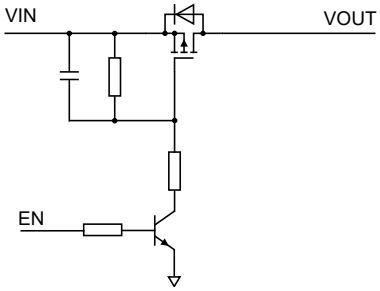
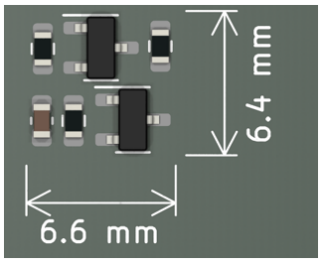
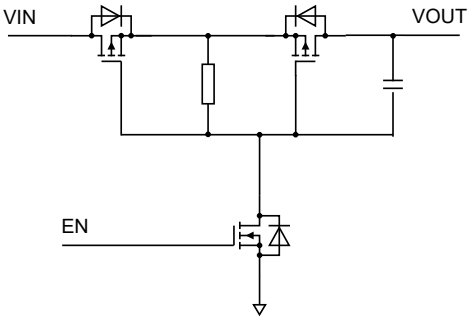
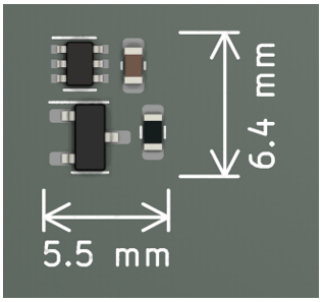
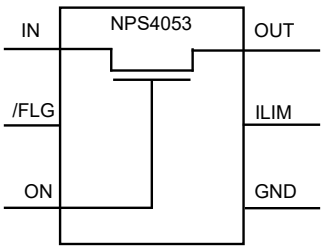
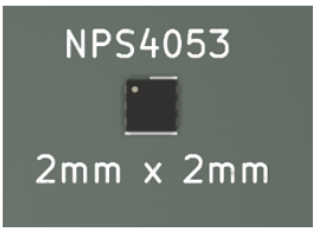


Fig. 13. Size comparison between Nexperia NPS4053 IC and discrete PMOS solution with reverse current blocking and quick output discharge

4. Load switch comparisons

Table 1. Common load switch configurations with comparisons

Circuit	PCB dimensions	Advantages / Disadvantages
Discrete PMOS load switch with NMOS for EN control 		Advantages: • Simple • Relatively small in design and PCB area • Customizable to user needs Disadvantages • Increased power consumption due to leakage path through resistor • No reverse current protection when pass FET is OFF • No slew rate control for VOUT
Discrete PMOS load switch with inrush control 		Advantages: • Slew rate control for VOUT • Customizable rise times with R and C selection Disadvantages • Non-linear (dv/dt) for VOUT • Non-linear inrush current • No reverse current protection when pass FET is OFF NOTE: Turn-on time can increase depending on R and C values chosen.
Discrete load switch with reverse current protection 		Advantages: • Suitable for power ORing designs • Current blocking in both directions when both MOSFETs are OFF Disadvantages • Requires more PCB area due to additional MOSFET • Only prevents reverse current when MOSFETs are OFF • $R_{DS(on)}$ is increased due to additional MOSFET

Integrated load switch
 
		Advantages:
		• Small package size
		• Built in protection features, e.g.:
		  • Active reverse current protection
		  • Hard short protection
		  • Over temperature protection
		  • Quick output discharge
		  • Adjustable current limit
		  • Built in soft start
		  • Under-voltage lockout
		• Low BOM cost
		• Fault indication

5. Revision history

Table 2. Revision history

Revision number	Date	Description
1.0	2024-03-26	Initial version.

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