



Pin FMEA for LSF family

Abstract: This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of Nexperia's LSF family under typical failure situations.

Keywords: FMEA, LSF, CMOS, 0.8V - 5 V systems

1. Introduction

The LSFxxxx family is a x channel bidirectional multi-voltage level translator family for push-pull and open-drain applications. It supports up to 100 MHz up translation and ≥ 100 MHz down translation at ≤ 30 pF capacitive load. There is no need for a direction pin which minimizes system effort.

The LSFxxxx supports 5 V tolerant I/O pins for compatibility with TTL levels in a variety of applications. The ability to set up different voltage translation levels on each channel makes those devices very flexible and suitable for a lot of different applications.

2. LSF family overview

- Specified from -40 °C to $+125$ °C
- Bidirectional voltage translation with no direction pin
- Up translation:
 - ≤ 100 MHz; CL = 15 pF, 30 pF
 - ≤ 50 MHz; CL = 50 pF
- Down translation:
 - ≥ 100 MHz; CL = 15 pF, 30 pF
 - ≥ 50 MHz; CL = 50 pF
- Hot insertion
- Bidirectional voltage level translation between:
 - 0.8 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
 - 1.2 V and 1.8 V, 2.5 V, 3.3 V and 5.0 V
 - 1.8 V and 2.5 V, 3.3 V and 5.0 V
 - 2.5 V and 3.3 V and 5.0 V
 - 3.3 V and 5.0 V
- Low standby current
- 5 V tolerant I/O pins to support TTL
- Low R_{ON} provides less signal distortion
- Latch-up performance exceeds 100 mA per JESD78 class II level A
- Multiple package options
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Pin FMEA

This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of Nexperia's LSF family under typical failure situations such as a short-circuit to V_{CC} or GND or to a neighboring pin, or if a pin is left open.

A failure is classified according to its effect on the LSF device and the functionality of the application; see [Table 1](#).

Table 1. Classification of failure effects

Class	Failure effect
A	damage to device
	affects application functionality
B	no damage to device
	may affect application functionality
C	no damage to device
	no affect to application functionality

Table 2. FMEA matrix for pin short-circuit to V_{refA} *V_{refA} is the reference voltage associated with the A port.*

Pin	Class	Remarks
Enable	B	Normal operation condition, no damage, no leakage, may affect functionality.
An terminal	B	If An defined LOW, External short circuit current, no damage to device, will affect functionality
An terminal	B	if An defined HIGH, no external current, Bn level will not change.
refB	B	External short circuit current, no damage to device, will affect functionality of the application.
Bn terminal	B	If Bn defined LOW, External short circuit current, no damage to device, will affect functionality
Bn terminal	B	if Bn defined HIGH, no external current, An level will not change.
GND	B	Will affect functionality.

Table 3. FMEA matrix for pin short-circuit to V_{refB} *V_{refB} is the reference voltage associated with the B port.*

Pin	Class	Remarks
Enable	C	Normal operation condition
An terminal	B	If An defined LOW, External short circuit current, no damage to device, will affect functionality
An terminal	B	if An defined HIGH, External short circuit current, Bn level will not change.
refA	B	External short circuit current, no damage to device, will affect functionality of the application.
Bn terminal	B	If Bn defined LOW, External short circuit current, no damage to device, will affect functionality.
Bn terminal	B	If Bn defined HIGH, no damage to device, will affect the functionality.
GND	A	short-circuits and high currents can damage device, will affect functionality.

Table 4. FMEA matrix for pin short-circuit to GND *V_{refA} is the reference voltage associated with the A port.* *V_{refB} is the reference voltage associated with the B port.*

Pin	Class	Remarks
Enable	B	normal operating condition, no damage, no leakage, may affect functionality.
An terminal	B	if An defined LOW, no damage, no leakage, no output level change, affects application functionality.
An terminal	B	if An defined HIGH, no damage, no leakage, will affect application functionality.
refA	B	Increased supply current from refA into GND. No damage, no leakage, will affect application functionality.
refB	B	Increased supply current from refB into GND. No damage, no leakage, will affect application functionality.
Bn terminal	B	if Bn defined LOW, no damage, no leakage, no output level change, affects application functionality.
Bn terminal	B	if Bn defined HIGH, no damage, no leakage, will affect application functionality.

Table 5. FMEA matrix for pin left open V_{refA} is the reference voltage associated with the A port. V_{refB} is the reference voltage associated with the B port.

Pin	Class	Remarks
Enable	B	undefined operating condition, no damage, increases leakage, may affect functionality.
An terminal	B	Depends on direction; A to B direction: Bn= "1". No damage, no leakage.
Bn terminal	B	Depends on direction; B to A direction: An= "1". No damage, no leakage.
GND	B	undefined operating condition, no damage, will affect functionality.
refA	B	undefined operating condition, no damage, will affect functionality.
refB	B	undefined operating condition, no damage, will affect functionality.

Table 6. FMEA matrix for pin short-circuits between neighbor pins V_{refA} is the reference voltage associated with the A port. V_{refB} is the reference voltage associated with the B port.

Pin	Class	Remarks
An to A _{n+1}	C	if An terminals have same voltage levels: no damage, no leakage.
	B	if An terminals have different voltage levels: will affect functionality.
An to Bn	B	if An and Bn have different voltage levels, no damage, will affect functionality.
	B	if An and Bn have same voltage levels, no damage.
An to GND	-	see Table 4
An to V _{refA}	-	see Table 2
An to V _{refB}	-	see Table 3
Bn to B _{n+1}	C	if Bn have same voltage levels, no damage, no leakage.
	B	if Bn terminals have different voltage levels: will affect functionality.
Bn to An	B	if An and Bn have different voltage levels, no damage, will affect functionality.
Bn to An	B	if An and Bn have same voltage levels, no damage.
Bn to GND	-	see Table 4
Bn to V _{refA}	-	see Table 2
Bn to V _{refB}	-	see Table 3
GND to V _{refA}	-	see Table 2
GND to V _{refB}	-	see Table 3

4. Revision history

Table 7. Revision history

Rev	Date	Description
AN90050 v.1	20231214	AN90050 initial version

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