AN90048

Understanding of critical SiC parameters for efficient and stable designs

Rev. 2 — 21 December 2023 Application note

Document information

Information	Content
Keywords	SiC-MOSFET, SiC parameters
Abstract	This application note presents and discusses the impact of few important SiC MOSFET parameters which will help the design engineers to benchmark devices from various suppliers.

nexperia

1. Introduction

Megatrends such as connectivity and digitalization, electrification, automation and energy efficiency open considerable opportunities and demands in terms of power conversion systems. Power electronics designers are increasingly faced with resolving the puzzle of achieving maximum efficiency together with lower system size, enhanced reliability, and longer lifetime whilst reducing system costs. Silicon Carbide (SiC) based converters pave the way to achieve this compared to conventional Si based ones.

SiC has unique properties that distinguish it from silicon– it has a three times higher energy gap, meaning it takes three times the energy to elevate an electron from the valence band to the conduction band. This allows SiC to withstand a ten times higher electric field strength. Therefore, SiC-based devices can handle higher voltages – or can be made with thinner and higher doped drift layer for the same voltage class. As a result, similarly rated SiC devices are much smaller, provide lower conduction and switching losses as well as can operate at higher switching speeds. Moreover, the three-fold higher thermal conductivity allows more effective dissipation of heat per unit area designers can use these advantages of SiC to create superior power systems.

While choosing the right SiC MOSFETs for their application, engineers are quite well equipped to look into the standard static and dynamic parameters from data sheets of different suppliers. However, the level of details and impact of each parameter in system level design is not well documented nor fully understood. In this application note, a few such parameters, such as R_{DSon} temperature stability, threshold voltage tolerance, gate charge balance, impact of gate driver voltage, SiC MOSFET body diode robustness have been considered. The guidance provided in this application note will help designers to select the right fit SiC devices from different suppliers and compare them with Nexperia SiC devices and harness maximum benefits to optimize their system performance.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2023. All rights reserved

2. On-resistance R_{DSon} temperature stability

The on−resistance (R_{DSon}) of a SiC MOSFET consists of the contributions from several internal, V_{GS} dependent, resistive elements. Most notable are the channel resistance (R_{CH}), JFET resistance (R_J) and drift region resistance (R_{DRIFT}). R_{CH} has a negative temperature coefficient and dominates R_{DS} at lower V_{GS}. Conversely, R_J and R_{DRIFT} have a positive temperature coefficient and are dominant at higher V_{GS} levels. For V_{GS} > 13 V, the on−resistance has a distinct positive temperature coefficient characteristic as shown in Figure 1. This results in a negative feedback effect in current sharing between parallel devices. During parallel operation, when one MOSFET experiences a rise in junction temperature, the positive temperature coefficient causes an increase in R_{DS}, decreasing the current and forcing the parallel MOSFET to take on additional current until a natural balance occurs.

The temperature dependence of the on-resistance depends on the breakdown voltage and the device type also. For example, the 1200 V devices are having higher temperature coefficient because of the higher resistance of the drift layer compared to lower voltage class devices. Moreover, with high temperature, the R_{DSon} is increased to limit the highest saturation current, thus improving the short-circuit ruggedness of the device as well.

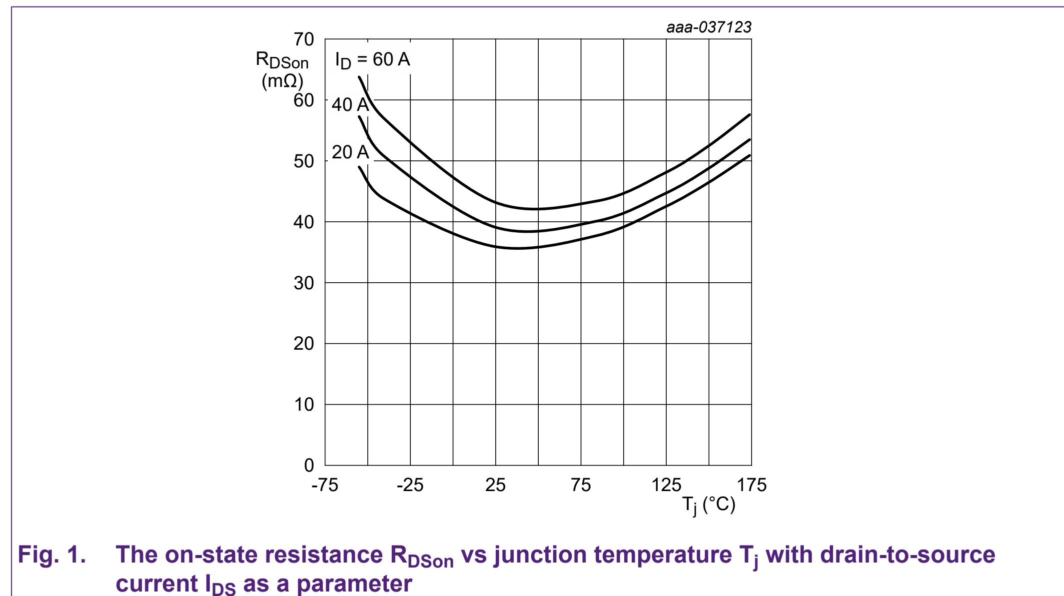


Fig. 1. The on-state resistance R_{DSon} vs junction temperature T_j with drain-to-source current I_{DS} as a parameter

In general, Silicon Carbide is well known for its temperature stability, however, as the junction heats up during operation in power electronics, it is common for R_{DSon} resistance to increase as temperature increases at a factor typically between 1.6 to 2.

Consequently, a 40 mΩ device at 25 °C, can end up at 80 mΩ when a junction temperature of 175 °C is reached.

Unlike other devices, Nexperia 1200 V SiC MOSFETs deliver the smallest R_{DSon} temperature drift. For example, a 40 mΩ Nexperia device at 25 °C, will only increases to 56 mΩ at a junction temperature of 175 °C. Therefore, a temperature drift with a factor of only 1.4 is visible as shown in Figure 2.

The benefit of this R_{DSon} temperature stability is a lower conduction loss at elevated temperatures compared to similarly rated devices from other vendors. This makes Nexperia SiC devices ideal for demanding power conversion applications such as motor drives, charging infrastructure, solar, uninterruptable power supplies and many more.

All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2023. All rights reserved

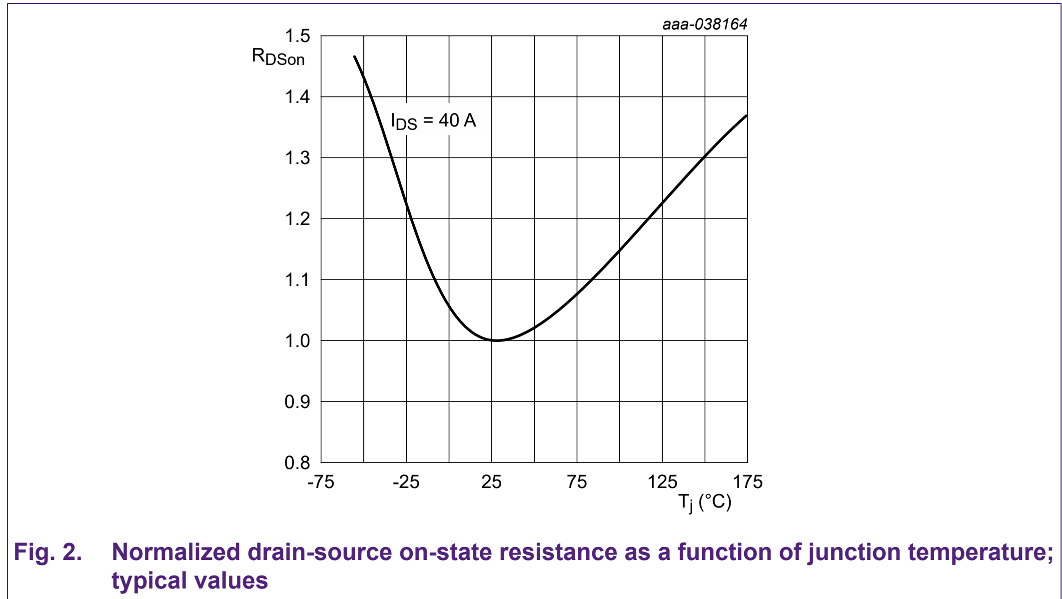


Fig. 2. Normalized drain-source on-state resistance as a function of junction temperature; typical values

3. Threshold voltage tolerance

The threshold voltage of a MOSFET is an important indicator for safe device operation, with the range of 2 to 4 volts usually providing an acceptable operating margin. Nexperia 1200 V SiC MOSFETs have a threshold voltage of 2.3 V (typical), thereby ensuring safe operation.

Going beyond threshold voltage, another key parameter of safe device operation is the threshold voltage tolerance which represents the spread between the specified minimum and maximum threshold voltage. A key advantage of low threshold voltage variation or tolerance is that it enables highly symmetrical switching behavior which is necessary when it is required to have multiple SiC MOSFETs operating in parallel. This balanced parallelization reduces the stress on semiconductors during dynamic switching operation, enhances circuit performance and extends product lifetimes. Nexperia SiC MOSFETs have the lowest threshold voltage spreads of 1.2 V even under worst case conditions and therefore ensures excellent balanced parallelization of devices. The threshold voltage generally decreases as the temperature increases as shown in Figure 3 and detail design tolerance analysis should be carried out to ensure safe switching patterns and avoidance of parasitic turn-on events.

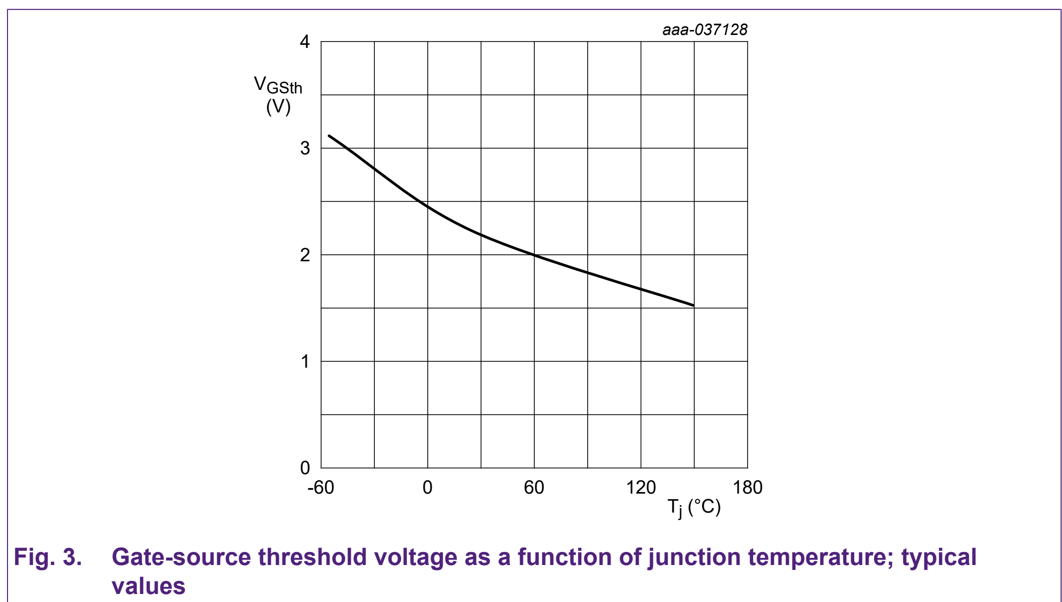


Fig. 3. Gate-source threshold voltage as a function of junction temperature; typical values

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2023. All rights reserved

4. Dynamic parameters - gate charge ratio

The dynamic characteristics determine the switching performance of the device. Several of these parameters are highly dependent on the measurement conditions. Consequently, understanding the dynamic characteristics before comparing data sheets from suppliers with different standard conditions is of utmost importance. Table1 is a sample dynamic characteristics table of NSF080120L3A0 device from Nexperia.

Table 1. Dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DD} = 800 V; I_D = 20 A; V_{GS} = -5/+15 V; T_j = 25 °C		-	52	-	nC
Q_{GS}	gate-source charge			-	22	-	nC
Q_{GD}	gate-drain charge			-	16	-	nC
C_{iss}	input capacitance	V_{DD} = 800 V; f = 0.5 MHz; V_{GS} = 0 V; T_j = 25 °C		-	1335	-	pF
C_{oss}	output capacitance			-	74	-	pF
C_{rss}	reverse transfer capacitance			-	4	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 800 V; I_D = 20 A; $R_{G(ext)}$ = 2.2 Ω; V_{GS} = -5/+15 V; L = 82 µH; T_j = 25 °C		-	30	-	ns
t_r	rise time			-	14	-	ns
$t_{d(off)}$	turn-off delay time			-	15	-	ns
t_f	fall time			-	14	-	ns
E_{on}	turn-on switching loss			-	445	-	µJ
E_{off}	turn-off switching loss			-	38	-	µJ

An important consideration when introducing fast switching into an application is the impact of switching transients on system stray and device body capacitances. Impact of these device body capacitances on system dynamics can be summarized in below points for simple understanding and also captured in Table 2.

The gate–source capacitance - C_{gs} (C_{iss} - C_{rss}) determines the delay time and the value of di/dt. The switching speed will decrease if a larger C_{gs} parameter device is selected. It should be noted that the value of C_{gs} does not significantly influence the voltage slew rate.

The gate–drain capacitance - C_{gd} (C_{rss}) determines the value of dv/dt, which is also known as "Miller capacitance." The value of C_{gd} is far lower than the value of C_{gs} and C_{ds}, and a small change in C_{gd} will cause a significant change in the value of dv/dt. It can be seen that the delay time and di/dt have no obvious relationship with the value of C_{gd}.

The drain–source capacitance - C_{ds} (C_{oss} - C_{rss}) influences the value of dv/dt, and there is no clear relationship between C_{ds}, delay time, and di/dt. An additional C_{ds} sometimes added to achieve soft turn-off by increasing C_{ds}. Both turn-on and turn-off dv/dt will decrease with an increase of C_{ds}, and turn-off loss and turn-off voltage overshoot will decrease as a result. However, the stored charge in C_{ds} during the turn-off period will cause a significant current overshoot during the turn-on period, which means an obvious increase in the turn-on loss.

Table 2. Influence of circuit parameters on the switching behavior

	$(di/dt)_{on}$	*$(dv/dt)_{on}$*	*$(di/dt)_{off}$*	*$(dv/dt)_{off}$*	*E_{on}*	*E_{off}*
C_{gs} ↑	↓	–	↓	–	↑	↑
C_{gd} ↑	–	↓	–	↓	↑	↑
C_{ds} ↑	–	↓	–	↓	↑	↑

Although input capacitance values are useful, they do not provide accurate results when comparing the switching performances of two devices from different manufacturers. Effects of device size and transconductance make such comparisons more difficult. A more useful parameter from the circuit design point of view is the gate charge rather than capacitance. Most manufacturers include both parameters on their data sheets. The advantage of using gate charge is that the designer can

All information provided in this document is subject to legal disclaimers. © Nexperia B.V. 2023. All rights reserved

easily calculate the amount of current required from the drive circuit to switch the device on in a desired length of time.

$Q_{G(tot)}$, Q_{GS}, and Q_{GD} are all parameters from the same gate charge curve usually provided in the data sheet. They describe how much gate charge the MOSFET requires to switch, for certain conditions. The gate charge parameters are dependent on the threshold voltage, drive voltages and the switching dynamics as well as the load that is being switched. Due to capacitance variation with voltage and current, it is better to look at the gate charge data rather than the capacitance data when determining switching performance. This is especially true if the gate-driver circuit for the MOSFET is limited to a particular current, and a rapid switch is required.

Total gate charge Q_G includes Q_{GS} and Q_{GD}. Q_{GS} represents the accumulation of charges in Gate-Source capacitance while Q_{GD} is the accumulation of charges in Gate-Drain capacitance. In high frequency operations, Q_G should be selected as small as possible. A low gate charge or Q_G leads to low gate drive losses during switching operation which reduces the power consumption and the requirements for the gate driver.

Another important and often overseen metrics in switching performance is the ratio between the Gate to Drain Charge or Q_{DG} and Q_{GS}, the Gate to Source Charge. Devices deliver the most stable performance without unwanted Miller turn-on instability when the Gate to Drain Charge is lower or very close to the Gate to Source Charge.

Thanks to their relatively low gate charge and well-balanced Gate to Drain Charge and Gate to Source Charge, Nexperia 1200 V SiC MOSFETs are within the desired charge range for Silicon Carbide devices. This means that, in comparison to other Silicon Carbide devices on the market, Nexperia devices deliver the best combination of low power consumption, high robustness and safe switching performance.

While selecting a device for hard switching application, Q_{GD} and R_{DSon} will give a better indication of Figure of Merit of the devices. For soft switching converters, Q_{oss} together with Q_{GD} and R_{DSon} will give a better indication of the device suitability.

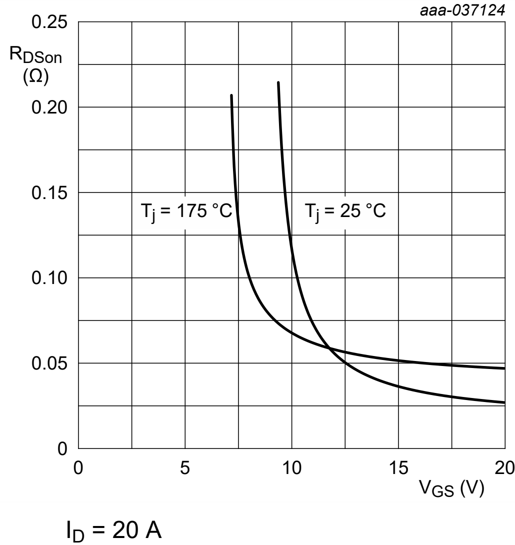
5. Impact of Gate Driver voltage

This section will guide about the impact of the gate drive voltage on the static and dynamic losses of the SiC MOSFETs. On one hand, a high ON-state gate-source voltage V_{GS} is required for proper channel inversion, low ON-state loss and fast switching while on the other hand, a lower ON-state V_{GS} reduces the electrical stress on the gate oxide and improves long term reliability.

While selecting the gate driver voltage optimized for best performance the temperature behavior of the R_{DSon} characteristic should be taken care as shown in Figure 4. Below 13 V gate voltage, the drain current increases with temperature. It is not recommended to have V_{GS} below +13 V for on-state. In general, the device could be driven with higher gate-source voltages than 15 V, which further improves the on-state behavior as shown in Figure 5.

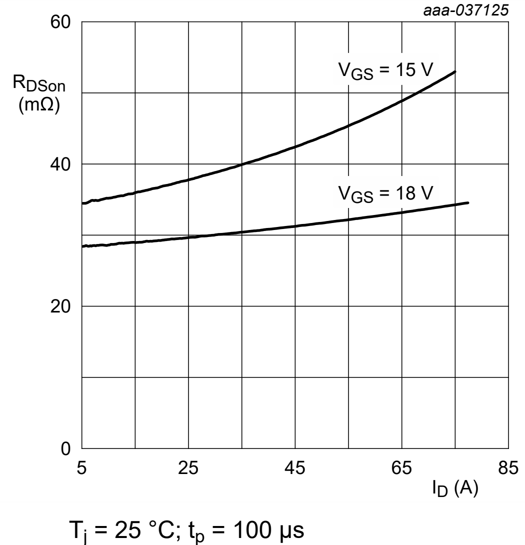
All information provided in this document is subject to legal disclaimers.

© Nexperia B.V. 2023. All rights reserved



I_D = 20 A

Fig. 4. Drain-source on-state resistance as a function of threshold voltage



T_j = 25 °C; t_p = 100 µs

Fig. 5. Drain-source on-state resistance as a function of drain current; typical values

Figure 6 and Figure 7 show the difference in the switching loss (E_{off} and E_{on}) due to variation of the gate drive voltage for Nexperia TO-247, 3 pin, 40 mΩ device. For this package, keeping the $R_{G(ext)}$= 2.2 Ω same, the switching loss when the device is turned ON (E_{on}) decreases as the driving supply voltage $V_{G(on)}$ increases. E_{on} at 18 V is reduced by 1.4 times compared with 15 V. In contrast, the switching loss when the device is at E_{off} shows little variation with $V_{G(on)}$.

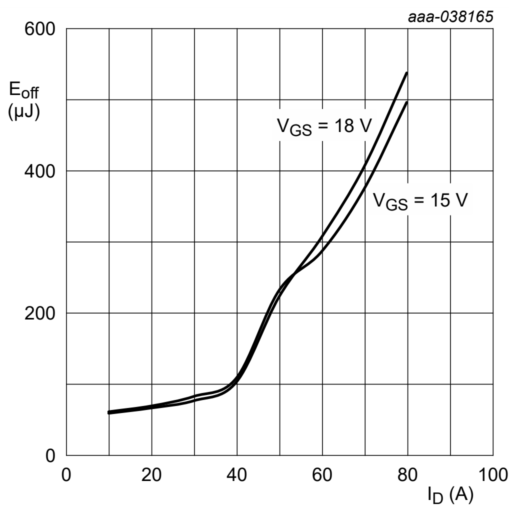


Fig. 6. Turn off energy as a function of drain current; typical values

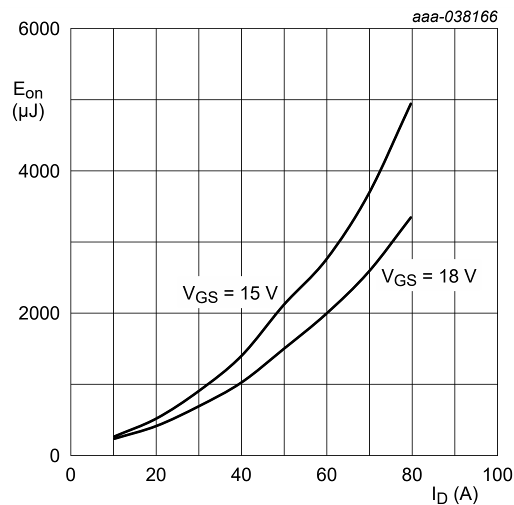


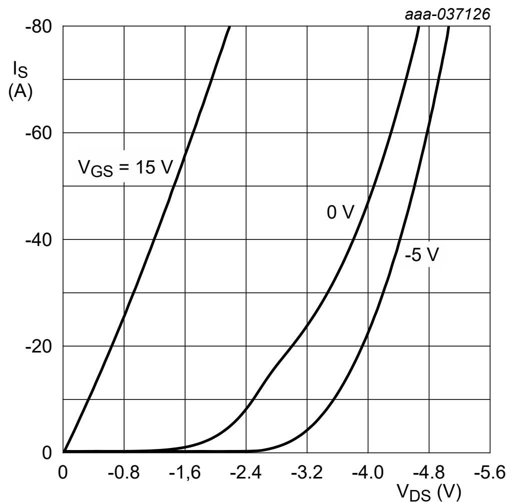
Fig. 7. Turn on energy as a function of drain current; typical values

Understanding the implications of the selected gate voltage on the operation of the power device in application will be fundamental for achieving an optimal balance between electrical performance and reliability. Accelerated stress tests are a suitable tool for evaluating the impact of V_{GS} stress on threshold voltage and gate oxide reliability especially at elevated temperature.

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2023. All rights reserved

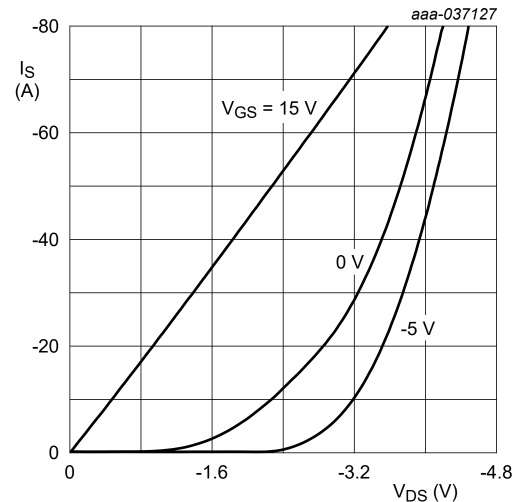
6. Excellent low forward voltage and recovery voltage

SiC MOSFETs are often used in symmetrical bridge configurations, featuring a high side and a low side device, with complimentary switching. A dead time is maintained when both devices are in OFF state and necessary to prevent short circuits. During the dead time, current continues to flow through the body diode of the MOSFETs and the voltage drop of the device is higher than when the device's channel is turned on. This higher voltage drop during dead time leads to higher losses.



T_j = 25 °C; t_p = 100 µs

Fig. 8. Source current as a function of source drain voltage; typical values (third quadrant characteristics)



T_j = 175 °C; t_p = 100 µs

Fig. 9. Source current as a function of source drain voltage; typical values (third quadrant characteristics)

Thanks to their outstanding body diode robustness, Nexperia 1200V SiC MOSFETs' body diodes have a lower voltage drop compared to other similarly rated SiC counterparts on the market. Operating at 25 A and 85 °C, the Nexperia SiC MOSFETs have a voltage drop of only roughly 3.5 V while other vendors with same Rdson have easily more than 5 V. Therefore, compared to other devices used under the same conditions and with the same dead time, the loss during dead time operation of Nexperia 1200 V SiC MOSFETs is much lower. This lower loss prevents the generation of excessive heat and gives designers flexibility in choosing the dead time they need.

The body diode Q_{rr} is an important parameter for bridge topology with hard commutation. With the low Q_{rr} of the SiC MOSFET, switching loss reduces and enables an increase in switching frequency. The higher the temperature, the higher the reverse-recovery charge. Fortunately, the absolute values at the rated current are still fairly low, meaning the Nexperia MOSFET has significantly lower, almost negligible, reverse-recovery losses. At the same time, the risk of failure and noise generated due to the recovery current can be expected to be reduced.

7. Conclusion

This application note presents and discusses the impact of few important SiC MOSFET parameters which will help the design engineers to benchmark devices from various suppliers. Assuming the practical design guidelines and best layout practices have been followed, the information of this application note will help to get the maximum performance out of the SiC MOSFET for any power conversion system application.

All information provided in this document is subject to legal disclaimers. © Nexperia B.V. 2023. All rights reserved

8. Revision history

Revision	Date	Description
1	20231201	Application note
2	20231221	Change: Figures 6 and 7 titles corrected

All information provided in this document is subject to legal disclaimers.
© Nexperia B.V. 2023. All rights reserved

9. Legal information

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

© Nexperia B.V. 2023. All rights reserved

Contents

1. Introduction..........2
2. On-resistance R_{DSon} temperature stability..........3
3. Threshold voltage tolerance..........4
4. Dynamic parameters - gate charge ratio..........5
5. Impact of Gate Driver voltage..........6
6. Excellent low forward voltage and recovery voltage. 8
7. Conclusion..........8
8. Revision history..........9
9. Legal information..........10

© Nexperia B.V. 2023. All rights reserved

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 21 December 2023