



# AN90041

## Gate drive circuit design for Nexperia 650 V Enhancement-mode (e-mode) GaN FETs

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application note

### Document information

Information	Content
Keywords	GaN FET, drive circuit, Kelvin source (KS)
Abstract	This application note provides guidance on the gate drive circuit design for Nexperia's 650 V Enhancement-mode GaN FETs with a Kelvin source terminal.

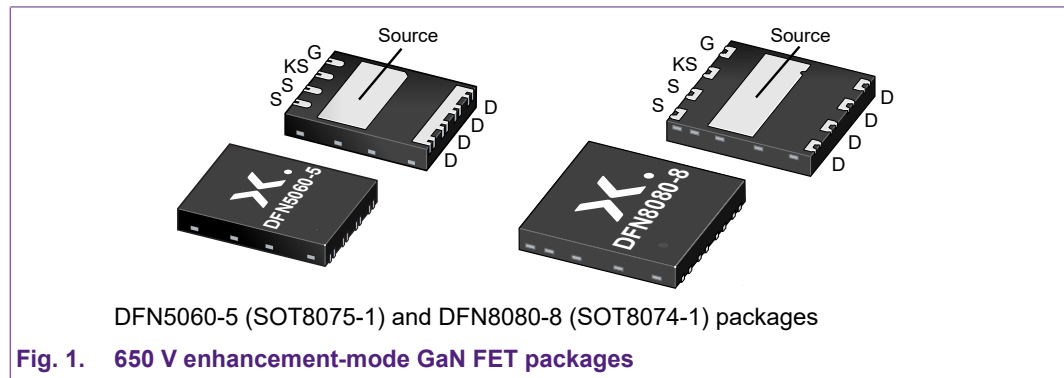
## 1. Introduction

Nexperia have introduced a range of Enhancement-mode (e-mode) GaN FETs. These are available in compact, DFN leadless packages with very low parasitic inductance and feature a Kelvin source terminal to allow for decoupling of the gate drive and power loops.

This application note details some important considerations for the design of their gate drive circuitry.

## 2. 650 V e-mode GaN FET packages

Nexperia's 650 V e-mode GaN FET devices are available in 5 mm × 6 mm and 8 mm × 8 mm Dual-Flat No-lead (DFN) surface mount packages. These packages have very low parasitic inductance and feature a Kelvin source (KS) terminal, see [Fig. 1](#).



## 3. Gate drive parameters

The key gate drive parameters for Nexperia e-mode GaN FETs and for Si MOSFETs are listed in [Table 1](#).

**Table 1. Drive difference between Nexperia e-mode GaN FET and Si MOS**

Parameter	650 V Nexperia e-mode GaN FET	Si MOSFET
Continuous maximum gate-source voltage	-1.4 V / +7 V	-20 V / +20 V
Gate-source threshold voltage	1.2 V - 2.5 V	2 V - 4 V
Recommended operating gate-source voltage	5.5 V - 6.2 V	8 V - 12 V

### 4. Kelvin source KS pin

During hard switching, drain current  $di/dt$  increases rapidly. There will be a voltage drop induced on the internal source inductance  $L_S$ , which will slow down the turn-on speed, (see Fig. 2):

$$V_{GS} = V_{DRV} - L_G \frac{di_G}{dt} - L_S \frac{di_D}{dt} \tag{1}$$

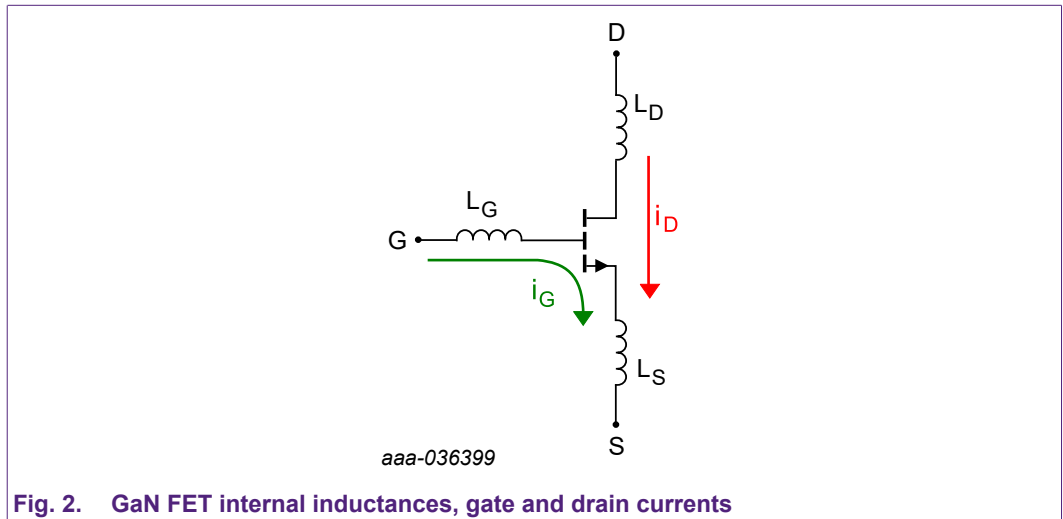


Fig. 2. GaN FET internal inductances, gate and drain currents

The source pins and KS pin are connected together internally, the KS pin can effectively decouple the gate drive loop and power loop to avoid the influence of power loop current change on the drive loop, see Fig. 3.

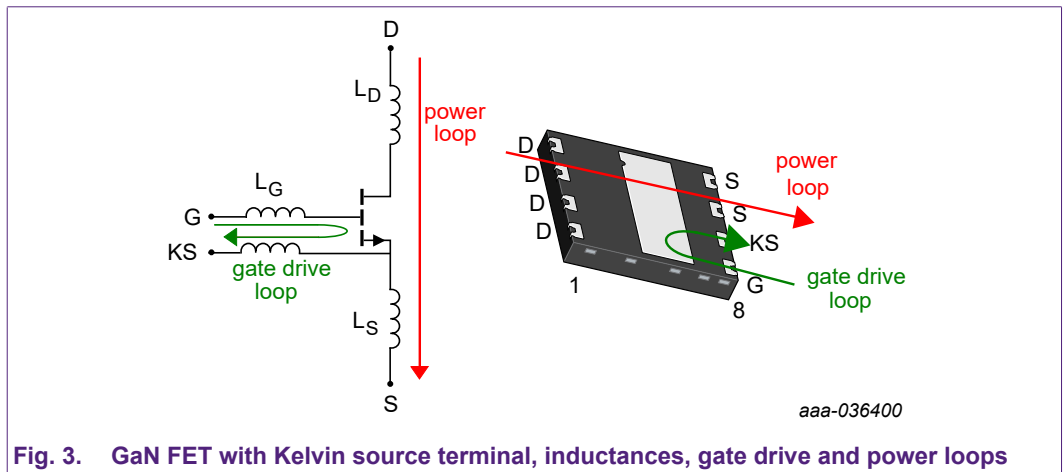


Fig. 3. GaN FET with Kelvin source terminal, inductances, gate drive and power loops

For Quasi-Resonant (QR) and other similar topologies where the controller integrates the gate drive, then the gate drive loop and the power loop are coupled together through  $R_{sense}$  and the KS pin is directly connected to the Source pin; see Fig. 4.

Gate drive circuit design for Nexperia 650 V Enhancement-mode (e-mode) GaN FETs

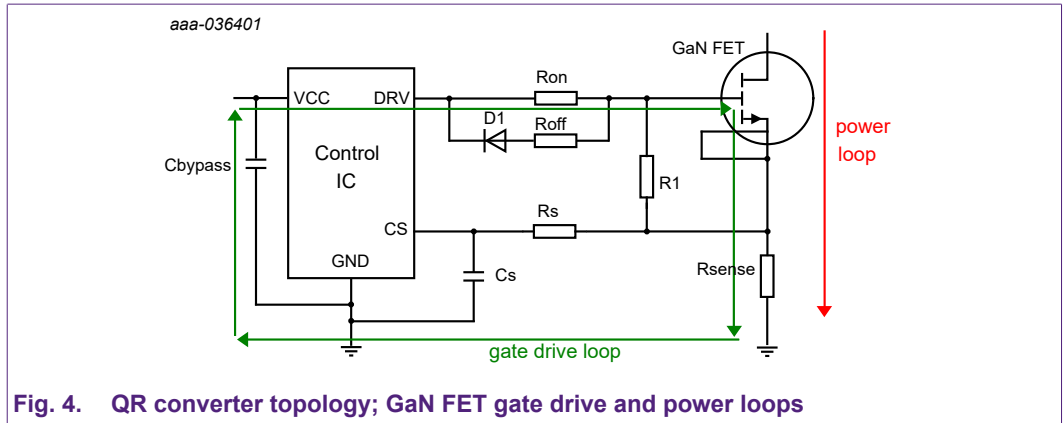


Fig. 4. QR converter topology; GaN FET gate drive and power loops

For half-bridge and other similar topologies, where the gate drive loop and power loop are independent, it should be noted that KS pin and Source pin should be separated during layout; see Fig. 5.

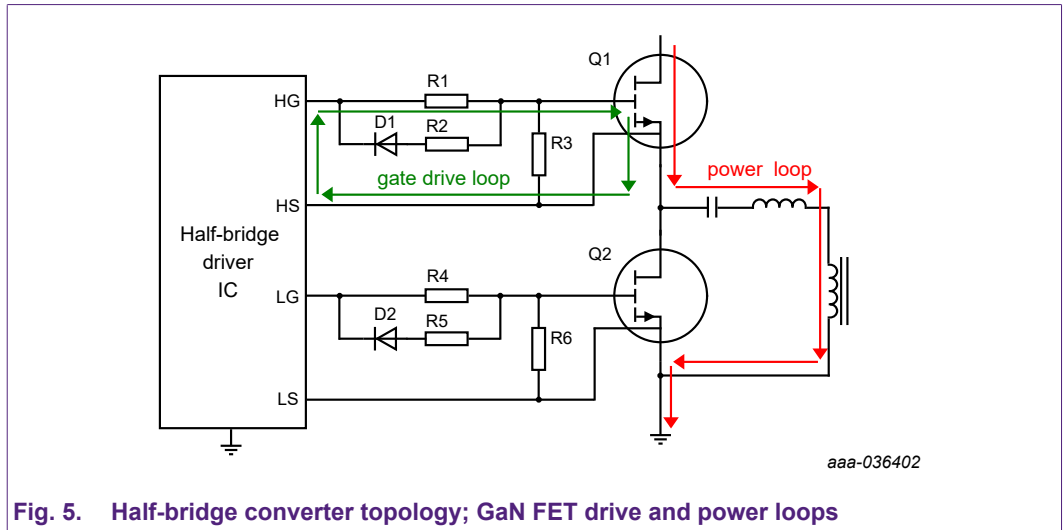


Fig. 5. Half-bridge converter topology; GaN FET drive and power loops

The circuit designer may want to consider using separate isolated gate driver ICs, such as Si8271 from Skyworks as this allows for optimising the layout for the e-mode GaN FETs.

## 5. Single GaN FET drive circuits

### 5.1. Level shift drive circuit

A level shifted drive circuit permits use of higher or unregulated drive voltage. Such a drive circuit is shown in Fig. 6. Table 2 gives typical component values depending on GaN FET type.

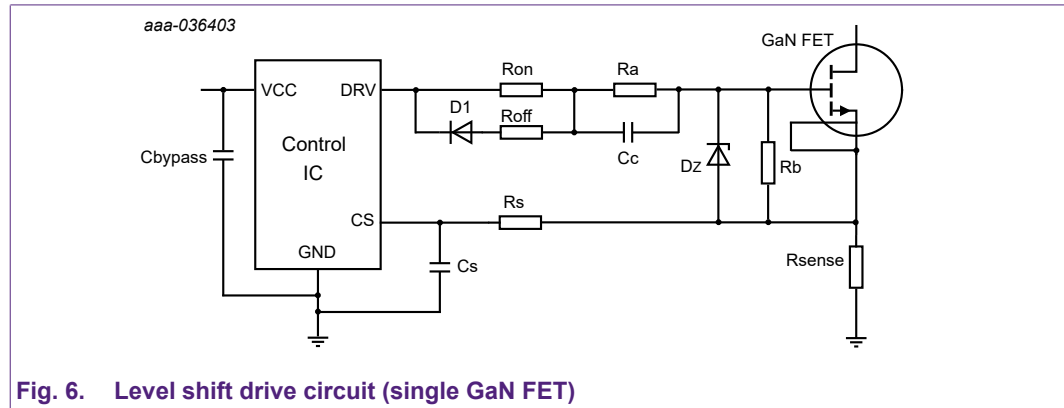


Fig. 6. Level shift drive circuit (single GaN FET)

Table 2. Recommended driver parameters (12 V output of IC)

Symbol	Typical value			Function
	GAN080-650EBE	GAN140-650FBE	GAN190-650FBE	
Ron	10 Ω - 1000 Ω	10 Ω - 560 Ω	10 Ω - 560 Ω	Control turn-on speed
Roff	2 Ω - 47 Ω	2 Ω - 47 Ω	2 Ω - 47 Ω	Control turn-off speed
Dz	6.2 V	6.2 V	6.2 V	Clamp the gate voltage
Ra	7.5 kΩ	7.5 kΩ	7.5 kΩ	Voltage divider
Rb	10 kΩ	10 kΩ	10 kΩ	
Cc	330 pF - 470 pF	680 pF - 1 nF	1 nF - 1.5 nF	Speed-up capacitor

NOTE: driver parameters should be adjusted according to the actual design.

### 5.2. Direct drive circuit

A direct gate drive circuit is shown in Fig. 7. Table 3 gives typical component values depending on GaN FET type.

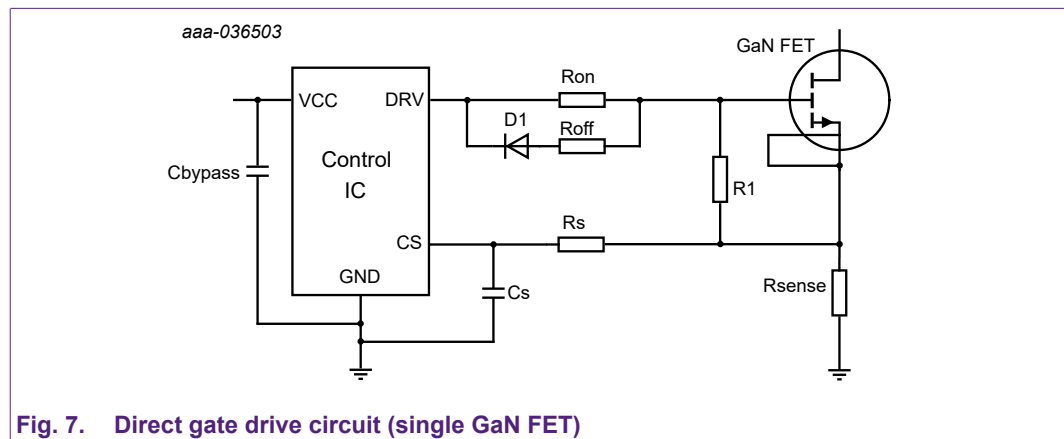


Fig. 7. Direct gate drive circuit (single GaN FET)

Gate drive circuit design for Nexperia 650 V Enhancement-mode (e-mode) GaN FETs

Table 3. Recommended driver parameters (6 V output of IC)

Symbol	Typical value			Function
	GAN080-650EBE	GAN140-650FBE GAN140-650EBE	GAN190-650FBE GAN190-650EBE	
R <sub>on</sub>	10 Ω - 1000 Ω	10 Ω - 560 Ω	10 Ω - 560 Ω	Control turn-on speed
R <sub>off</sub>	2 Ω - 47 Ω	2 Ω - 47 Ω	2 Ω - 47 Ω	Control turn-off speed

NOTE: driver parameters should be adjusted according to the actual design.

5.3. PCB layout precautions; single GaN FET

Correct PCB layout is critical in achieving the best performance from GaN FETs. Best design practice is:

- Minimize the drive loop by:
  - a) place C7 and C8 close to the control IC
  - b) place the drive circuit close to the GaN FET
- Minimize the power loop by placing C<sub>BUS</sub>, which comprises of C1 - C5, inductor and the GaN FET close together.

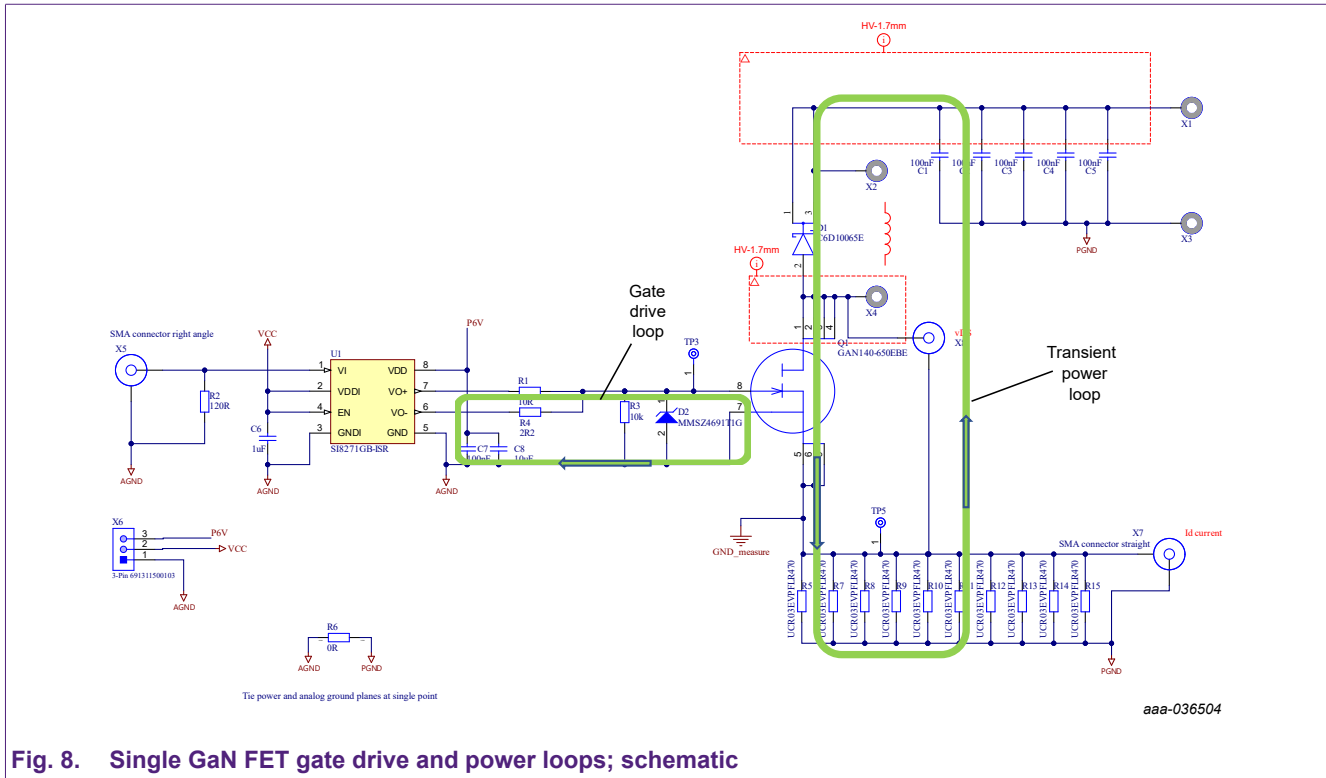


Fig. 8. Single GaN FET gate drive and power loops; schematic

Gate drive circuit design for Nexperia 650 V Enhancement-mode (e-mode) GaN FETs

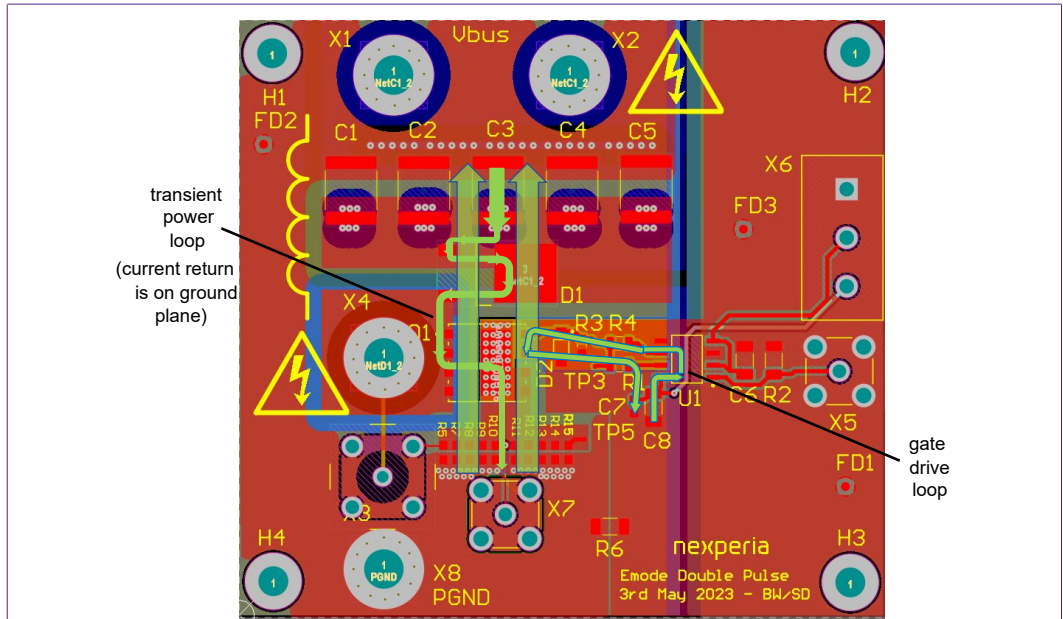


Fig. 9. Single GaN FET gate drive and power loops; recommended PCB layout

### 6. Half-bridge level shift drive circuit

A level shifted gate drive circuit permits use of higher or unregulated drive voltage. Such a drive circuit is shown in Fig. 10. Table 4 gives typical component values depending on GaN FET type.

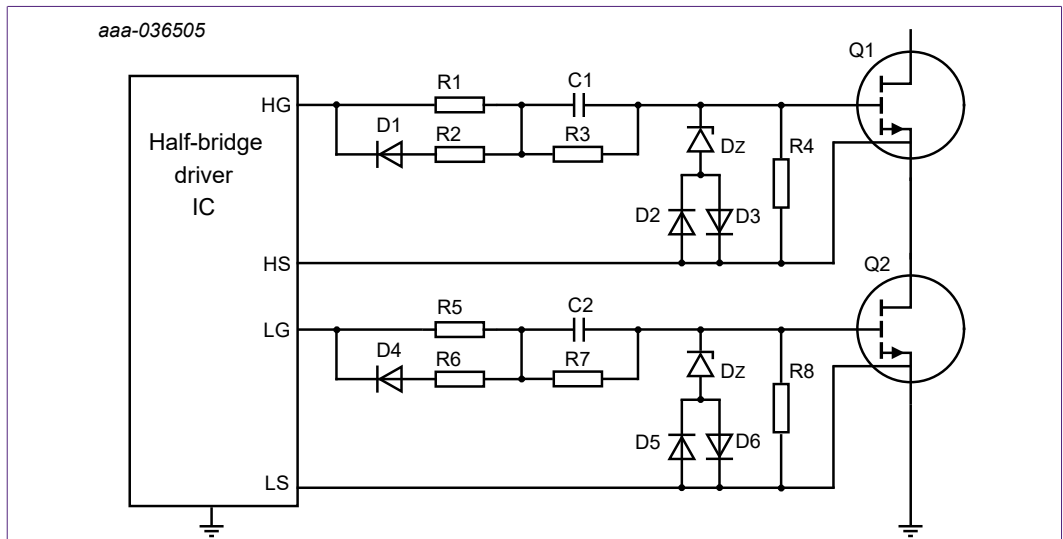


Fig. 10. Half-bridge level shift drive circuit

Gate drive circuit design for Nexperia 650 V Enhancement-mode (e-mode) GaN FETs

Table 4. Recommended driver parameters; half-bridge

Symbol	Function	Typical value	Range
R1	Control turn-on speed	390 Ω	10 Ω - 510 Ω
D1	Driver turn-off path	PMEG6002EB	Schottky diode (high fsw)
R2	Control turn-off speed	1 Ω	0 Ω - 10 Ω
C1	Speed-up capacitor	2.2 nF	2.2 nF - 3.3 nF
Dz1	Clamp positive $V_{GS}$ when turn-on	5.6 V	5.6 V - 6.2 V
D3	Driver turn on path	PMEG6002EB	Schottky diode (high fsw)
D2	Driver turn off path, increase negative $V_{GS}$	PMEG6002EB	Schottky diode (high fsw)
R3	Voltage divider	7.5 kΩ	2 kΩ - 7.5 kΩ
R4		10 kΩ	2 kΩ - 10 kΩ

NOTE: driver parameters should be adjusted according to the actual design.

6.1. PCB layout precautions; half-bridge

Correct PCB layout is critical in achieving the best performance from GaN FETs.

- Use a Kelvin source design, decouple power and gate drive loops
- Place the gate drive circuit close to the GaN FET to reduce parasitic inductance
- Do not route other nets in the drive circuit area to minimize interference and cross coupling
- For the high-side, the plane side below the gate drive should be connected to the switching node.

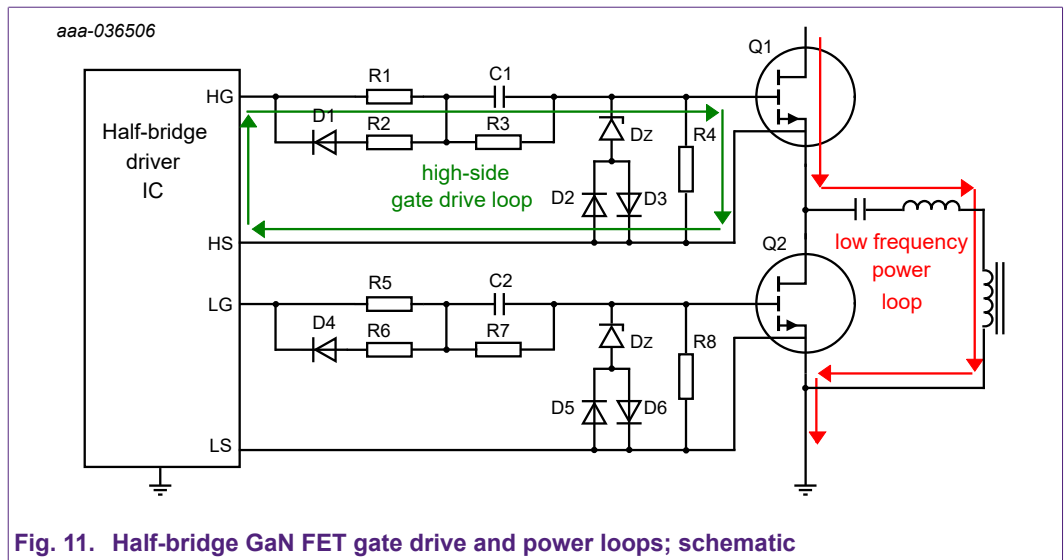
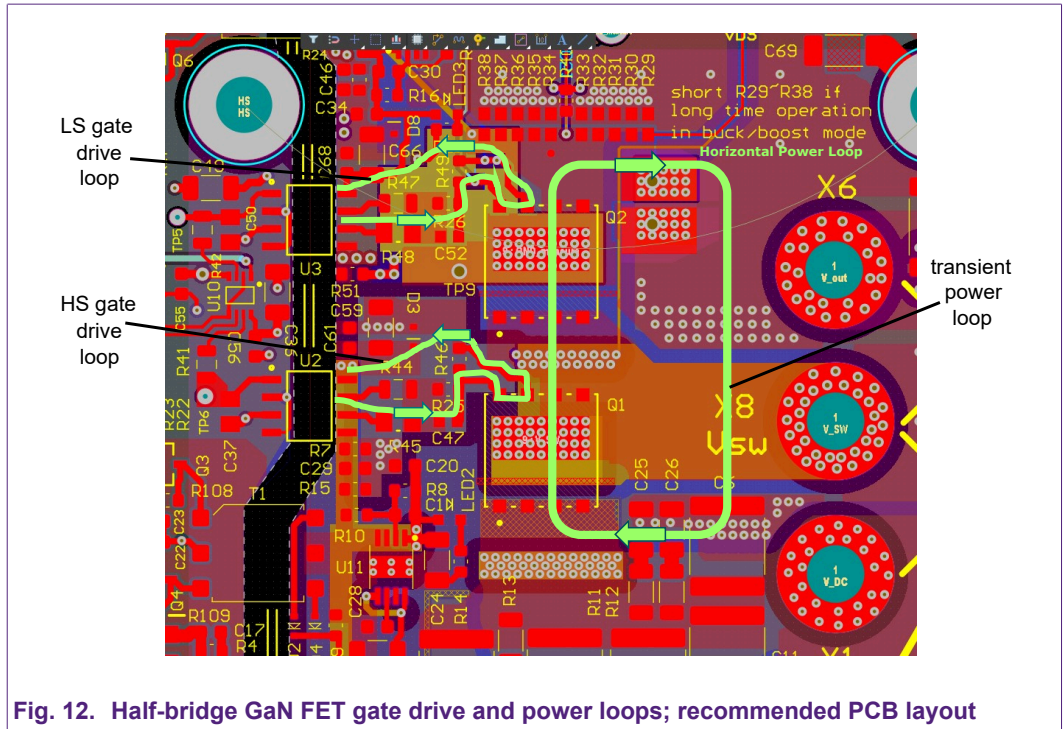


Fig. 11. Half-bridge GaN FET gate drive and power loops; schematic



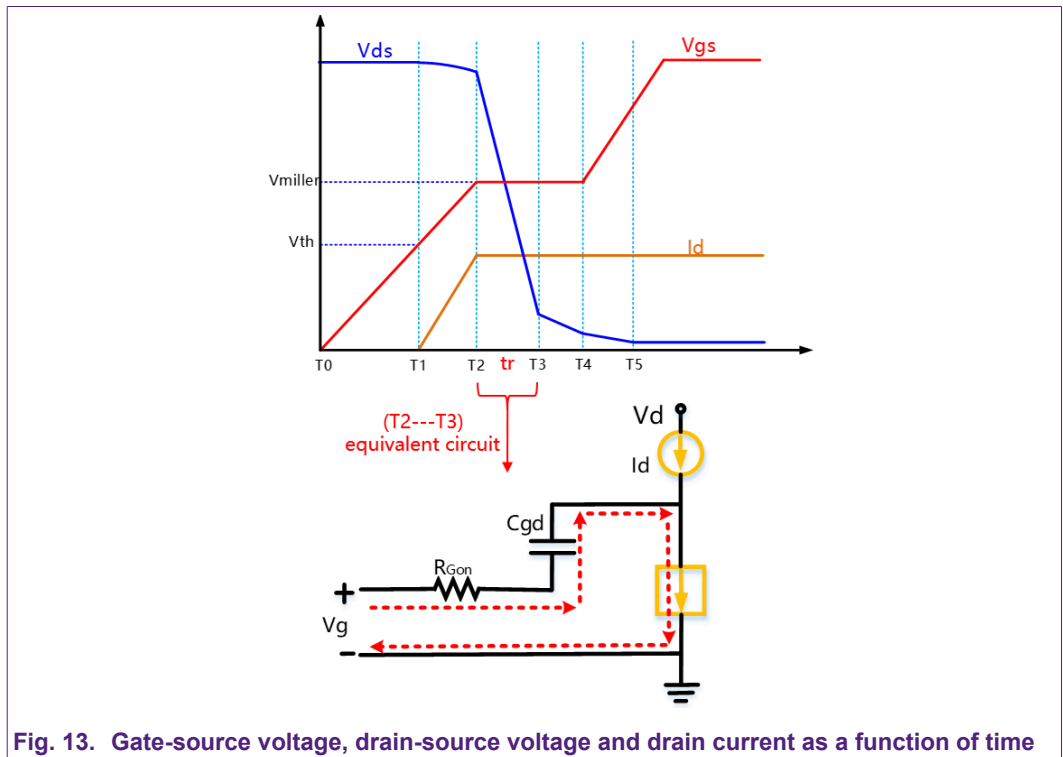
Gate drive circuit design for Nexperia 650 V Enhancement-mode (e-mode) GaN FETs



### 7. Influence of drive resistance on EMI

The turn-on speed,  $dv/dt$ , can be reduced by increasing  $R_{Gon}$  appropriately, thus reducing the switching noise. As shown in Fig. 13,  $R_{Gon}$  affects charging time of  $C_{gd}$ , the larger  $R_G$ , the larger  $t_r$ , the smaller  $dv/dt$  and hence the EMI noise.

Turn-off speed affects system efficiency and has little impact on EMI improvement. It is not recommended to adjust turn-off resistance  $R_{Goff}$ .



## 8. Suggested gate driver and controller ICs

Low-side gate drivers:

- Si8271 (isolated)
- LM5114
- HEY1011 (isolated)
- ACPL-P346 (opto)

Hi-Lo gate drivers:

- MDC901 (200 V)
- LMG1210 (200 V)
- Si8273 (isolated)
- NCP51530 (700 V)

Controller ICs with integrated gate drive:

- NCP1622 (PFC)
- UCC28056 (PFC)
- TEA2017AT (PFC + LLC)
- HR1211 (PFC + LLC)
- JW1515H (QR)

If a gate driver is being used with a bootstrap, then choose a bootstrap diode with low  $C_j$  and fast recovery time. For example an ES1J can be used. It is also advised to fit a 10  $\Omega$  resistor (0805) in series with the bootstrap diode

## 9. Revision history

Table 5. Revision history

Revision number	Date	Description
1.0	2023-05-09	Initial version.

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## List of Tables

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Table 1. Drive difference between Nexperia e-mode GaN FET and Si MOS.....	2
Table 2. Recommended driver parameters (12 V output of IC).....	5
Table 3. Recommended driver parameters (6 V output of IC).....	6
Table 4. Recommended driver parameters; half-bridge.....	8
Table 5. Revision history.....	10

## List of Figures

Fig. 1. 650 V enhancement-mode GaN FET packages.....	2
Fig. 2. GaN FET internal inductances, gate and drain currents.....	3
Fig. 3. GaN FET with Kelvin source terminal, inductances, gate drive and power loops.....	3
Fig. 4. QR converter topology; GaN FET gate drive and power loops.....	4
Fig. 5. Half-bridge converter topology; GaN FET drive and power loops.....	4
Fig. 6. Level shift drive circuit (single GaN FET).....	5
Fig. 7. Direct gate drive circuit (single GaN FET).....	5
Fig. 8. Single GaN FET gate drive and power loops; schematic.....	6
Fig. 9. Single GaN FET gate drive and power loops; recommended PCB layout.....	7
Fig. 10. Half-bridge level shift drive circuit.....	7
Fig. 11. Half-bridge GaN FET gate drive and power loops; schematic.....	8
Fig. 12. Half-bridge GaN FET gate drive and power loops; recommended PCB layout.....	9
Fig. 13. Gate-source voltage, drain-source voltage and drain current as a function of time.....	9

## Contents

---

<b>1. Introduction.....</b>	<b>2</b>
<b>2. 650 V e-mode GaN FET packages.....</b>	<b>2</b>
<b>3. Gate drive parameters.....</b>	<b>2</b>
<b>4. Kelvin source KS pin.....</b>	<b>3</b>
<b>5. Single GaN FET drive circuits.....</b>	<b>5</b>
5.1. Level shift drive circuit.....	5
5.2. Direct drive circuit.....	5
5.3. PCB layout precautions; single GaN FET.....	6
<b>6. Half-bridge level shift drive circuit.....</b>	<b>7</b>
6.1. PCB layout precautions; half-bridge.....	8
<b>7. Influence of drive resistance on EMI.....</b>	<b>9</b>
<b>8. Suggested gate driver and controller ICs.....</b>	<b>10</b>
<b>9. Revision history.....</b>	<b>10</b>
<b>10. Legal information.....</b>	<b>11</b>

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