AN90039

ESD protection devices for automotive Ethernet applications (100Base-T1, 1000Base-T1)

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Document information

Information	Content
Keywords	Automotive, Ethernet, 100BASE-T1, 1000BASE-T1, ESD
Abstract	This application note explains the properties of modern semiconductor ESD protection devices for 100BASE-T1 and 1000BASE-T1. ESD protection devices enable a robust system capable of withstanding destructive ESD events as well as giving improved EMC. Recommendations are given for using a common mode choke (CMC) to increase this robustness.

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1. Introduction

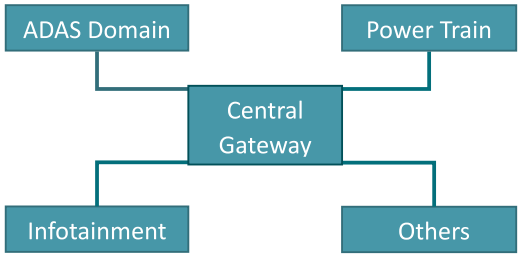
Although several ethernet solutions are popular in industrial and commercial applications nowadays, for several decades it was not widely adopted in the automotive area. Since 2016, there are two standards 100BASE-T1 and 1000BASE-T1 which were introduced in the automotive industry. An additional two standards, 10BASE-T1s and MGB-T1 (multi-gigabit) are in development. From the Institute of Electrical and Electronic Engineers (IEEE), 100BASE-T1 and 1000BASE-T1 are covered by the IEEE 802.3bw and the IEEE 802.3bp. Both standards are based on the industrial and commercial ethernet applications but were adopted to the specific automotive requirements mostly related to electromagnetic compatibility (EMC) [1]. This adaptation was done by the OPEN Alliance committees.

Automotive Ethernet enables fast and robust data communication. Empowering flexibility in bus topologies for several electronic control units (ECUs), automotive ethernet is a high potential candidate to manage the future demand on sharing real-time data, bandwidth, and robust operation. These properties help to accelerate the evolution of automotive network architecture from domain to zonal architecture. Automotive ethernet can be paired with several other protocols such as audio and video (AVB) which increases its potential for usage in ADAS, X-Domain and other complex systems.

In this application note the properties of modern semiconductor ESD protection devices for 100BASE-T1 and 1000BASE-T1 are explained. It will be shown how an ESD protection device acts in synergy within the circuitry resulting in a system that is robust against destructive ESD events and has improved EMC behavior. Furthermore, a recommendation will be made for common mode choke (CMC) to increase this robustness.

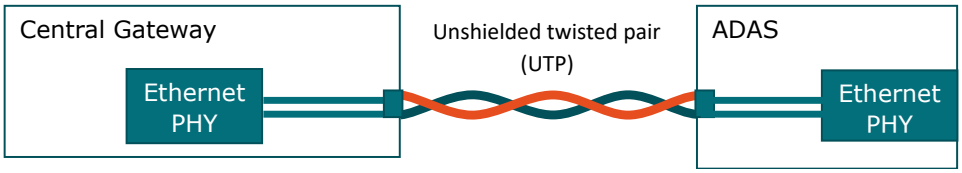
2. Topology of 100BASE-T1 and 1000BASE-T1

Due to the flexibility in usage and a significant increase in data rate (compared to traditional CAN HS/FD), automotive ethernet allows bridging of various complex communication domains, as illustrated in Fig. 1. This strengthens the role of automotive ethernet even more in future in-vehicle data communications architecture where key applications such as ADAS, infotainment and power train will significantly grow within the automotive field.



All domains are mainly connected using automotive ethernet applications.

Fig. 1. Typical topology of modern vehicles



For 100/1000BASE-T1 an unshielded twisted pair is used.

Fig. 2. Typical configuration of two ECU connected using automotive ethernet

The ECUs are usually connected with each other with unshielded twisted pair, (UTP), like in CAN or flexray applications (Fig. 2). This brings several benefits such as simple usage and low costs. However, it should be considered that unshielded cables can be problematic when it comes to the coupling of electromagnetic noise. Since in a real car harness a bunch of different cables are combined in a bundle, there is a certain risk of interference between them. Specifically, within a UTP in a typical bus topology, induced electrical noise can reach 100 V, which was verified by

several testing centers. During such an event, the ESD protection device is not allowed to trigger to avoid communication breakdown and link loss. This implies a novel requirement for an ESD protection device having a trigger voltage above 100 V.

The OPEN Alliance recommends a schematic including the electronic components shown in Fig. 3.

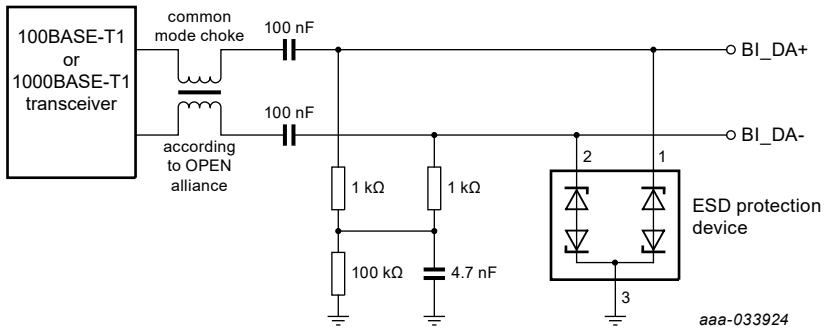
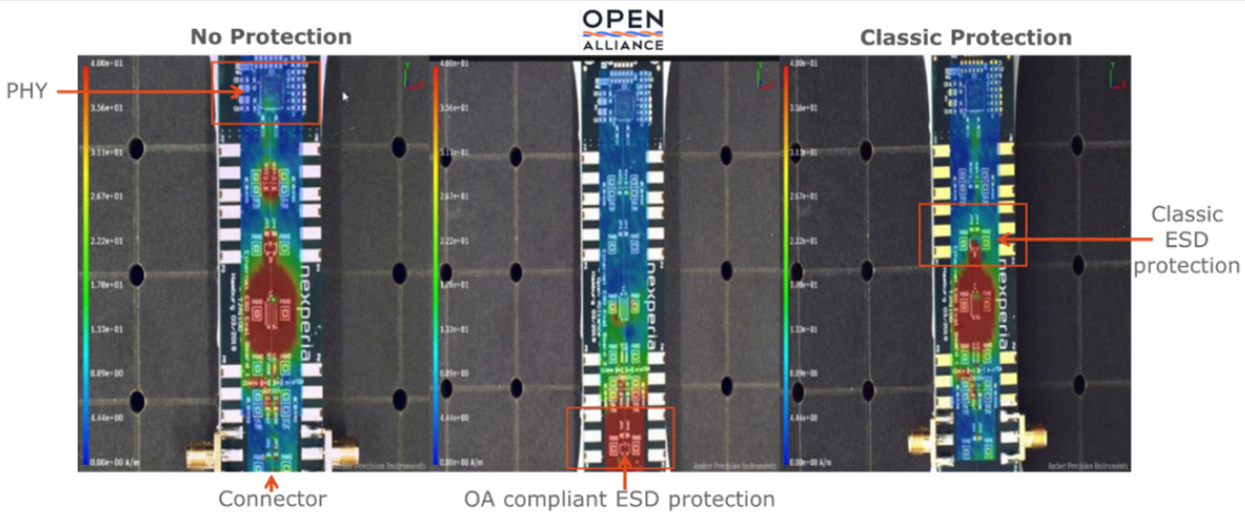


Fig. 3. 100/1000Base-T1 interface

The transceiver block on the left side contains the Physical Layer Interface (PHY) itself as well as some basic filtering components and the on-chip ESD protection. The next mandatory block is the common mode choke (CMC) with the common mode termination to reduce the unwanted common mode, and hence, the EMI. The ESD device is placed close to the connector and it can include two ESD protection diodes in one package e.g. SOT23 or two ESD diodes for each of the individual lines e.g in the DFN1006BD package. In other similar schematics, the position of the ESD is between the CMC and the PHY.

Note: it is strongly recommended that the ESD protection device is placed directly at the connector. At this position, the ESD current is clamped to GND thus not impacting the PCB, the Ethernet PHY or other components, see Fig. 4. In addition, an ESD protection device with >100V trigger as required by the 100/1000MBase-T1 specifications would perform its protecting role significantly better when placed at the connector, before the CMC.

The main difference between 100BASE-T1 and 1000BASE-T1 is the bandwidth (66 Mbps and 750 Mbps, respectively). Therefore, there is some different requirements on Signal Integrity (SI) which reflect in the choice of some of the circuitry. The ESD protection device is allowed to have slightly higher device capacitance for 100BASE-T1 than for 1000BASE-T1. Also, the CMC should follow the Open Alliance (OA) specifications on 100BASE-T1, 1000BASE-T1 and multi-Gigabit applications. More information on this is being provided later in this application note.



Red color highlights high current density. For the OA approach, having the ESD device close to the connector gives the lowest current density at the PHY location, the entire circuitry giving the best ESD performance for the system.

Fig. 4. Field scan of the ethernet circuitry during an ESD event

3. ESD protection device for 100BASE-T1 and 1000BASE-T1

As the 100BASE-T1 and 1000BASE-T1 topology and circuitry are almost the same they have very similar requirements for the ESD protection device used. The ESD device must follow the OA specification for ESD protections devices (Automotive Ethernet Specifications (opensig.org)). Following are some of the main requirements:

- Bi-directional
- No degradation after 1000 ESD pulses with 15 kV (IEC61000-2-4)
- Trigger voltage > 100 V
- V_{DC} > 24 V (short to battery)

In addition, the compliance of an ESD protection device is tested by a set of measurements:

Table 1. ESD protection device compliance measurements

Test	Purpose
S-Parameters	verify signal integrity
Damage from ESD	verify signal integrity after ESD event
ESD discharge current	evaluation residual ESD current which flows into the PHY during ESD event
RF clamping	verify robustness

Those measurements are performed by using the same set-up for 100BASE-T1 and 1000BASE-T1, but the PASS and FAIL criteria are defined by slightly different limits, especially for the S-parameters, e.g. due to the difference in the bandwidth. Those limits are given in the appendix of the corresponding specifications.

3.1. S-parameters

The idea behind the S-parameter measurement is to observe the SI behavior of an ESD protection device in frequency domain. Namely, Insertion Loss (IL), return loss (RL) and the common mode rejection ratio (CMRR). As matrix elements in the mixed mode scattering parameter matrix, those parameter are called S_{dd21}, S_{dd11} and S_{dc21} respectively. The index “dd” refers to differential and “dc” refers to differential to common.

- **IL,** the portion of the signal which is transmitted by the ESD protection device over frequency. The more the signal is transmitted, the better. In simple words it shows how much of the signal is transmitted through the ESD Device. It can be seen as a transfer function with strong focus on the impedance. The PASS condition is to stay above the limits defined in the specification.
- **RL** shows the portion of the signal which is reflected by the ESD protection device over frequency. The less signal is reflected the better. Also here are limits defined by the standardization committees. The PASS condition is to stay below the limits.
- **CMRR** shows the portion of the signal which is converted from the differential mode to common mode over frequency. This mode conversion is caused by asymmetries in the network and it should be minimized in differential signaling.

Some examples of S-parameters are shown in Fig. 5. The limits for all S-parameters are different for 100BASE-T1 and 1000BASE-T1 due to data rate and bandwidth of both.

More general information about the S-parameters can be found on the Nexperia YouTube channel Nexperia - YouTube.

For OPEN Alliance Ethernet, there are special limits defined in the specifications (Automotive Ethernet Specifications (opensig.org).

SCAN ME

Automotive Ethernet Specs

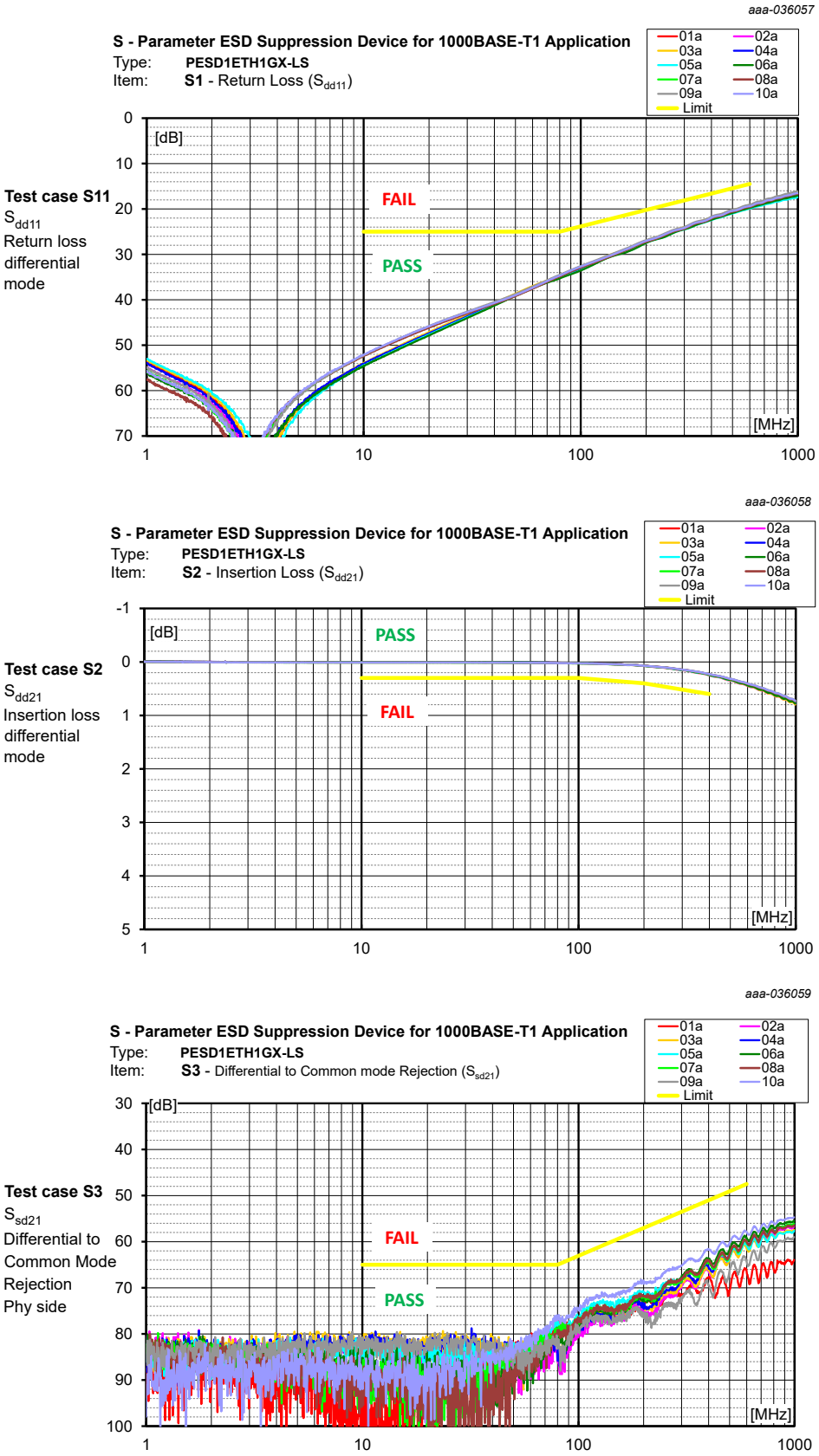
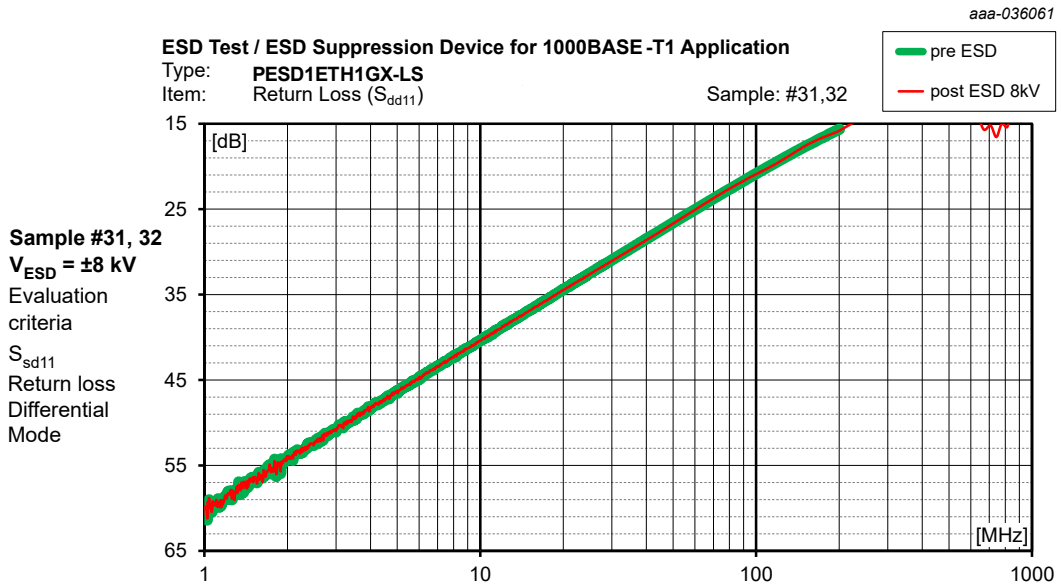


Fig. 5. S-parameter measurements; from test report of the PESD1ETH1GXLS-Q, measured by Forschungs- und Transferzentrum an der Westsächs. HS Zwickau (FTZ).

3.2. Damage from ESD: testing signal integrity after ESD events

The main focus of this test is to evaluate the impact of ESD on SI. Therefore, basically the same S-parameters are measured as previously shown but the measurements are done pre and post 20 pulses each polarity at 8 kV and 15 kV. The target specification is, the ESD device is not allowed to deviate more than 1 dB in the frequency range of 1 MHz to 200 MHz after the ESD stress pulses. S_{dd11} results from one of the ESD Devices are being shown in Fig. 6.

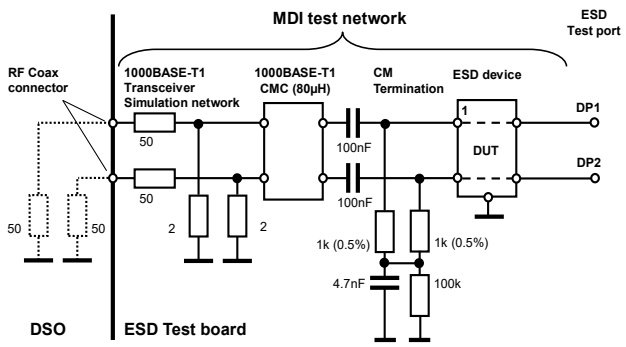


No deviations can be observed.

Fig. 6. S_{dd11} pre and post 8 kV ESD pulse

3.3. ESD discharge current measurement

During an ESD event, the ESD protection devices clamps the majority of the ESD pulse to ground. However, in real world applications there is always a certain portion of the pulse which goes over the ESD protection into the PHY. This residual current is an important parameter to evaluate the protection capability of the ESD device. For OPEN Alliance Ethernet 100/1000Base-T1, this residual current is measured using a standardized set-up. The set-up is shown in Fig. 7. The entire circuitry including the CMC and the ESD protection is included in the set-up. The characteristics of the PHY are simplified by a 2 Ω resistor.

Coupling of ESD:	Direct discharge method according to ISO 10605 (C = 150 pF, R = 330 Ω)
Test circuit:	 Type of CMC: ESD Saturation class II: not available ESD Saturation class I: muRata DLW32MH101XT2
ESD test voltage:	± 3 kV, ± 5 kV, ± 6 kV, ± 7 kV, ± 15 kV
Evaluation criteria:	Measured ESD discharge current shape

The circuitry represents the full Ethernet circuitry as shown in Fig. 1. The PHY is replaced by a 2 Ω resistor.

Fig. 7. Measurement set-up for the ESD discharge current measurement from a test report of the PESD1ETH1GLS-Q

The measurement is done for up to 15 kV for both polarities. The pass criteria are the limits gained from the 2 kV and 4 kV Human Body Model (HBM). In Fig. 8, the results for a 15 kV pulse are shown including the limits and the reference current from the ESD gun.

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JEDEC HBM Specs

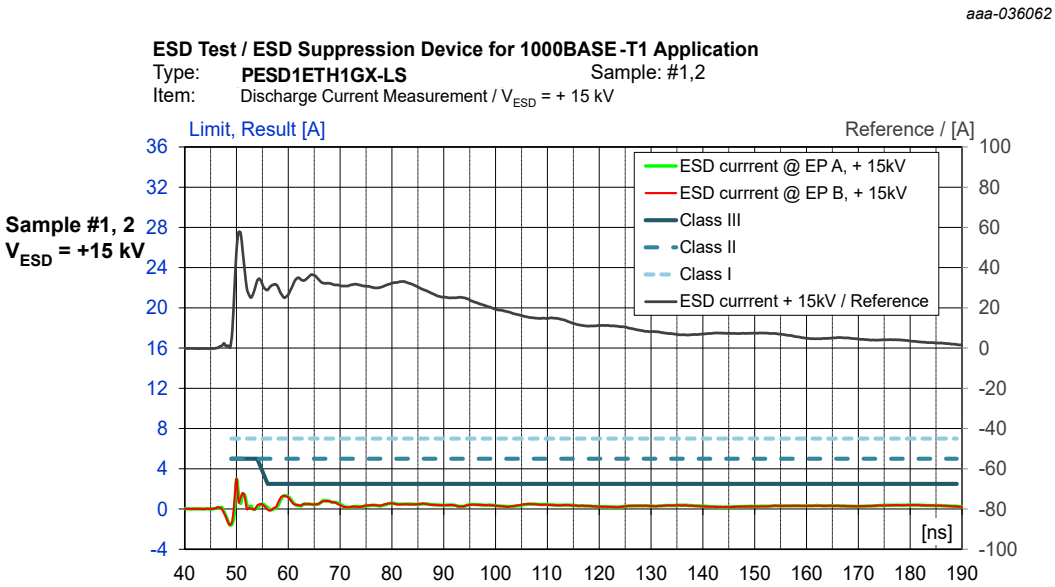


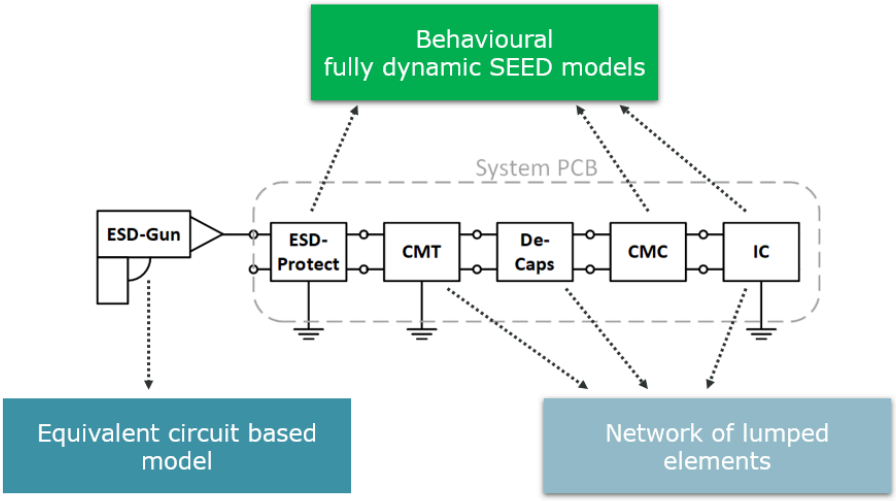
Fig. 8. ESD discharge current for the PESD1ETH1GLS-Q at 15 kV

3.4. SEED - simulation of ESD discharge current measurement

The systematic prediction of the system ESD performance is not a trivial task. The ESD robustness level of the standalone transceiver and of the passive components (including the external ESD protection device) do not allow us to conclude what the overall system ESD robustness level is.

Thus, the interaction between all the integrated components must be considered carefully. Here, a special attention should be given to a suitable match of external ESD protection, the CMC, as well as the on-chip ESD protection characteristics of the IC PHY transceiver pins. Note that these elements show a strongly non-linear high current behaviour.

The System Efficient ESD Design (SEED) methodology allows simulating the transient high-voltage, high-current behaviour of the whole system relevant for ESD. Here, an accurate modeling of the individual elements is required using behavioural models and equivalent circuits. The full simulation environment also includes a model of the ESD pulse generator. By this comprehensive simulation approach the residual ESD stress currents through different system parts as well as the voltages at different system nodes can be predicted.

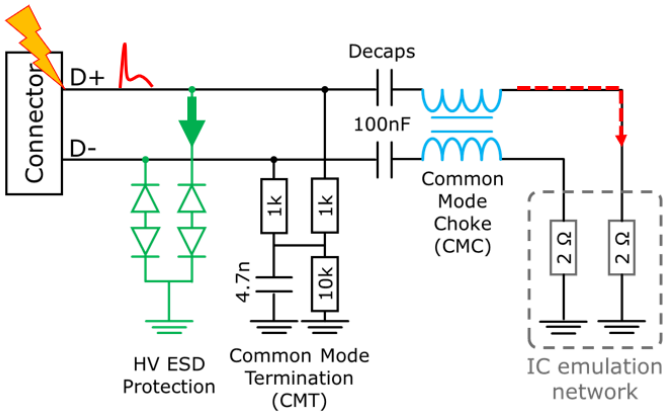


Fully dynamic SEED models are used to represent the behavior of ESD protection component and CMC, the Common Mode Termination (CMT) and decoupling capacitors (De-Caps) are represented by network of lumped elements, the IC internal ESD protection is modeled by 2 Ω lumped resistance as shown in Fig. 10.

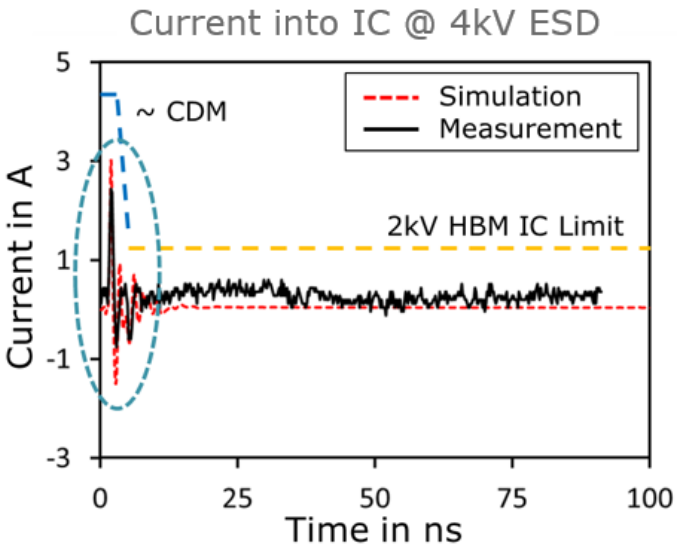
Fig. 9. Equivalent circuit block diagram of SEED model for the ESD discharge current measurement reference circuit

By assessing the transgression of critical quasi-static and dynamic IV limits of the IC PHY transceiver data pins the system level ESD robustness can be determined. Fig. 10 shows the 100/1000BASE-T1 circuitry of a system model and the comparison of system level measurement and simulation for the residual current into IC using a 4 kV ESD pulse according to IEC 61000-4-2.

In general, there is close agreement between the measurement and simulation results. The main characteristics of the current pulse into IC, it's overshoot with respect to the IC CDM limit as well as it's steady state behaviour with respect to the IC HBM limit are captured accurately by the simulation.



Set-up for system-level simulation of ESD discharge current into IC (represented by 2 Ω resistance network).



Measured and simulated residual current into IC for 4 kV ESD generator discharge into D+ data line, protected by snapback high-voltage ESD protection device and by CMC of L = 200 μH.

Fig. 10. System-level simulation of ESD discharge; set-up and results

For further information on the setup of transient system-level SEED simulation for automotive Ethernet circuitry as well as on the modeling details of high-voltage ESD protection with snapback, on the CMC and the ESD generator, please refer to the Nexperia white paper *Efficient prediction of ESD discharge current according to OPEN Alliance 100BASE-T1 specification using SEED* [4] as well as the Nexperia Automotive ESD Handbook [5].

4. SI and impact of ESD protection devices

4.1. PCB stack-up

In automotive applications, Printed Circuit Boards (PCBs) with four or more layers are most often used. The majority of those applications in mass production are usually based on standard FR4 PCB technologies. A typical PCB stack-up, including the dimensions is shown in Fig. 11. It should be mentioned that this stack-up is only one example. Also different PCB dimensions are common, applicable, and valuable. Microstrip lines are found to be suitable for ethernet applications but striplines can also be used.

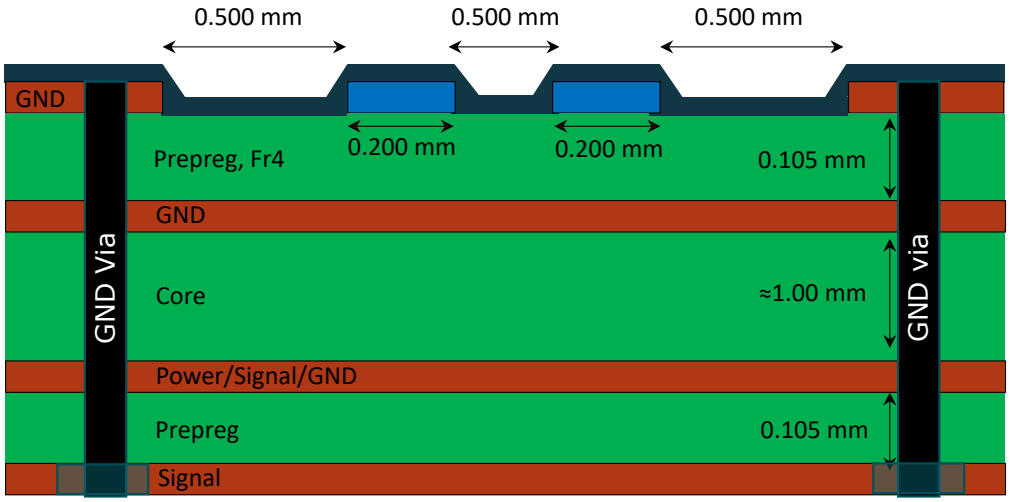


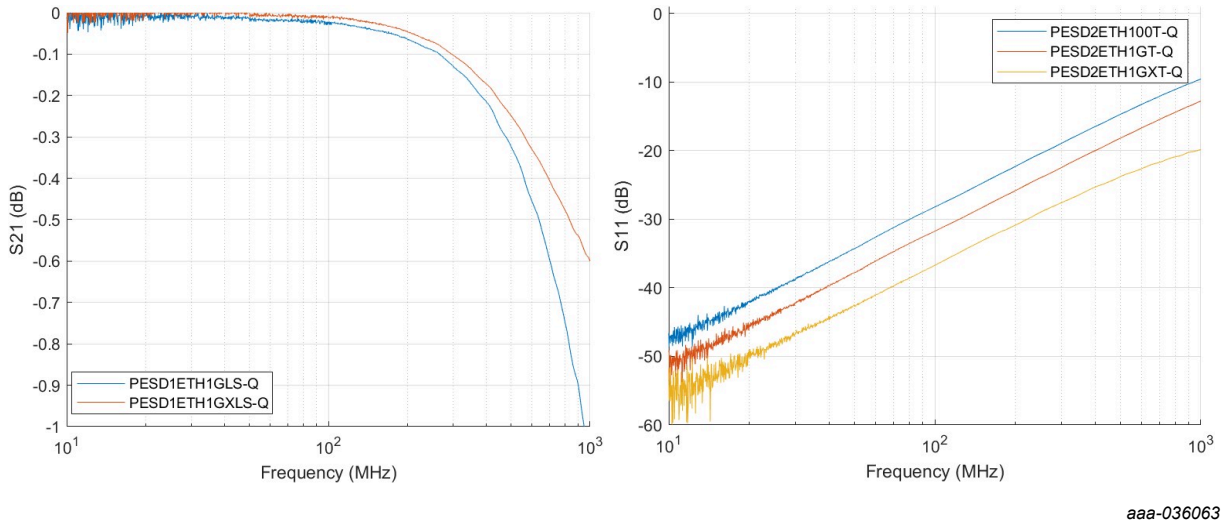
Fig. 11. Example of a typical stack-up and microstripline configuration based on a 4-layer PCB copper and FR4

The focus in high-speed applications is to keep the data traces in a controlled electromagnetic environment. Therefore, a ground (GND) layer directly underneath the traces without any cuts and slots should be considered. Adding a ground plane adjacent to the signal traces is also recommend. The use of multiple vias to connect to the ground plane is a good option. Those measures not only improve the SI but also improve EMC and minimize the internal interference within the PCB.

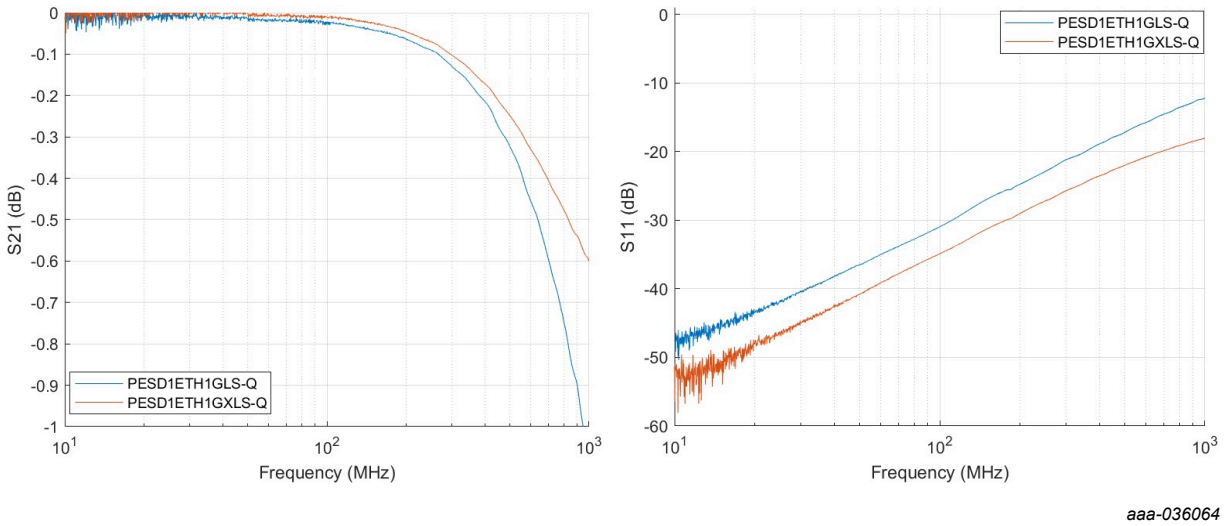
4.2. S-parameters simulations

SI is one of the key factors in automotive Ethernet. Even at data rates of 100 Mbps and 1000 Mbps, the data transmission requires special attention, especially in a multi-node ethernet topology. As described in Section 3, SI of the ESD protection devices is covered by additional measurements. Here, S-parameters of the ESD protection device are measured with respect to dedicated limits in IL, RL and CMRR.

Nexperia offers ESD protection devices for 100BASE-T1 and 1000BASE-T1 in two different packages, the established SOT23 and the leadless DFN1006BD. All devices are measured using a VNA and the S-parameters (see Fig. 12) can be provided on request in a touchstone format (.s2p or .s4p).



ESD devices in SOT23 package

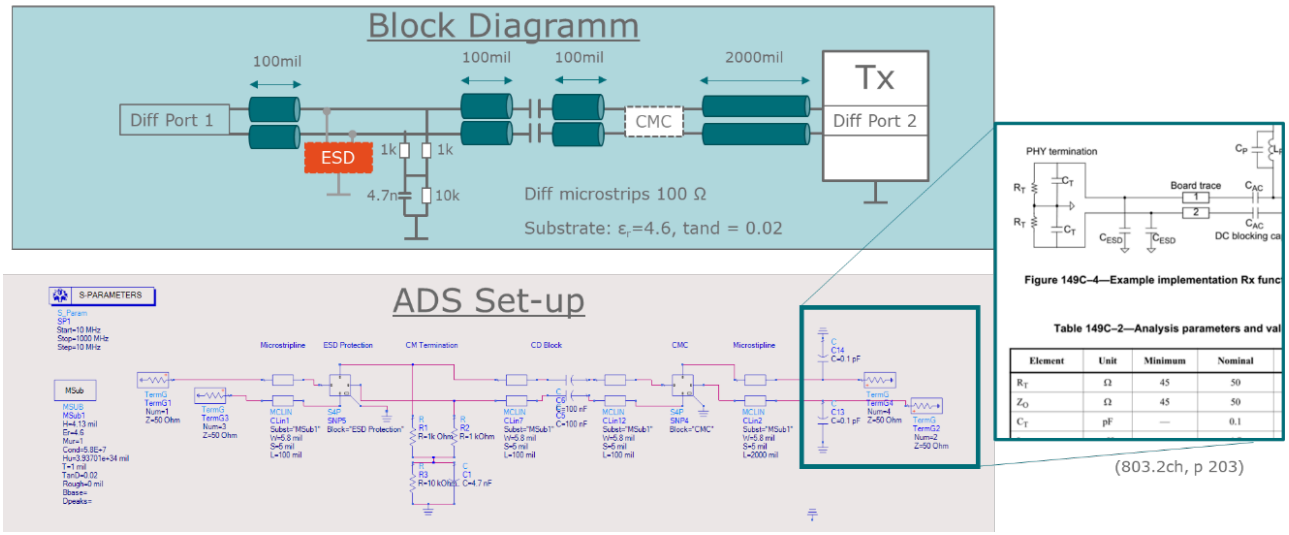


ESD devices in DFN1006BD package

Fig. 12. S-parameters as a function of frequency; SOT23 and DFN1006BD packages

Those measured S-parameters can be further used in a SI simulation. Fig. 13 shows a block diagram and the simulation set-up used in ADS Advanced Design Systems, Keysight [3], Microstrip lines (≈100 Ω differential) are represented using built-in models on a typical, lossy FR4 PCB material. The DC block and the termination network are simulated by ideal lumped elements. The ESD protection device as well as the CMC (DLW43MH201XK2L4532) are represented by measured S-parameters. The influence of the PHY was included by a corresponding termination using 50 Ω and 0.1 pF, as recommended in 803.2ch, p203.

Results of the simulation are shown including some limits for IR and RL from 803.2bp. The difference in the results shows up slightly at higher frequencies which is mostly dominated by the difference in capacitance between the devices.



The PHY was represented using 50 Ω with 0.1 pF in parallel. The microstrip lines are represented by the in-built ADS models, The common mode termination and the DC block are covered by ideal lumped elements. The CMC is represented by S-parameters, as well as the ESD protection device (from and).

Fig. 13. Simulation set-up in ADS to study SI

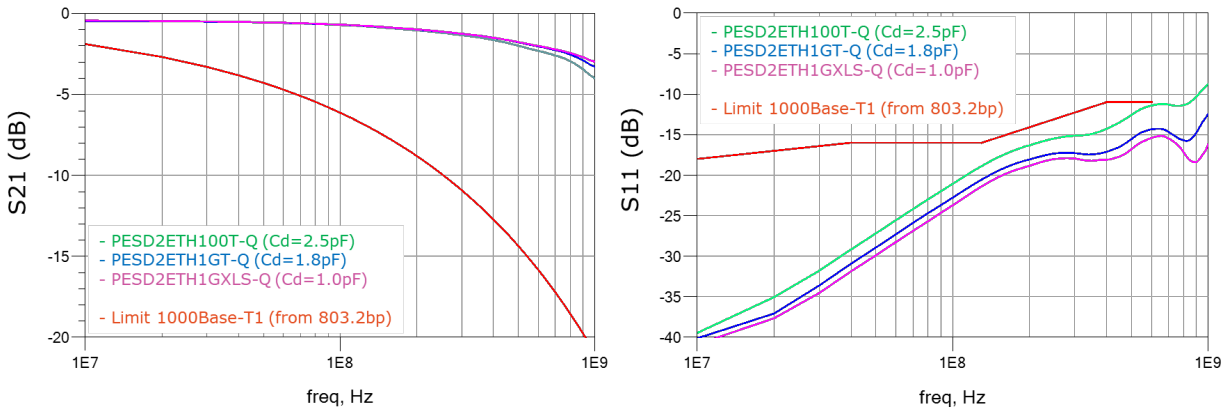
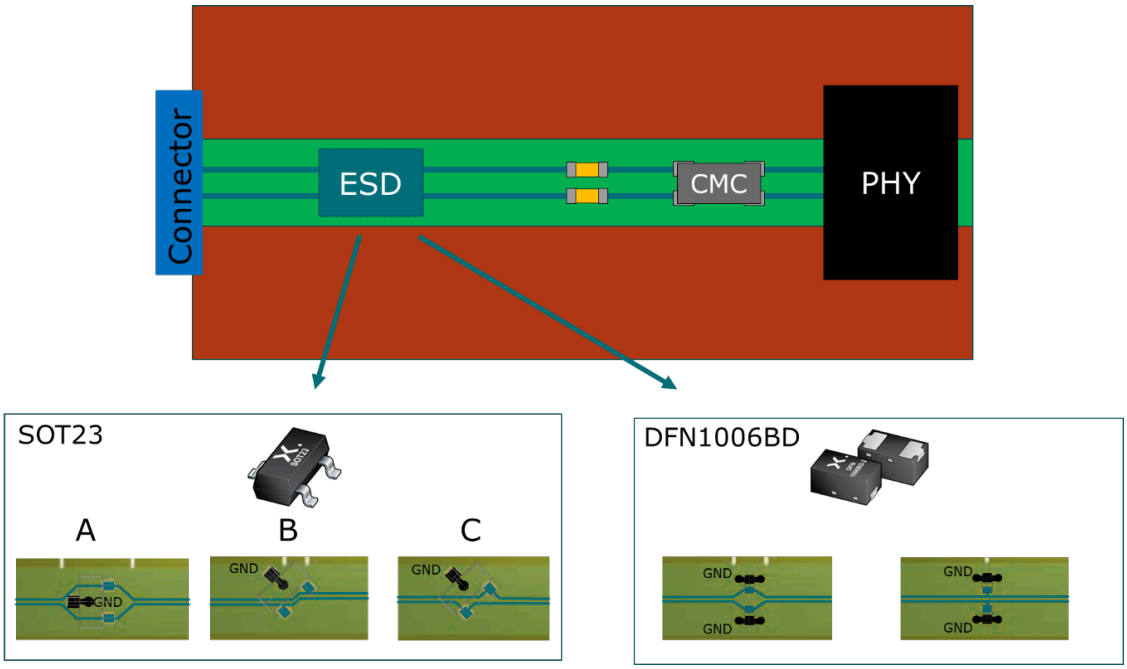


Fig. 14. Simulation results

4.3. PCB routing of ESD protection devices

The PCB routing to and from the ESD protection device is very important when considering the SI and the ESD performance. For the ESD performance, it is very important to route the signal line strictly over the pad and to avoid any stubs etc. Those stubs will have some intrinsic parasitic inductance which can prevent the ESD pulse to enter the ESD Device, especially for long stubs. For the SI it is very important that the impedance of the trance is kept at 100 Ω which means carefully adjusted PCB and trace dimensions within a dielectric environment and a straight line for both signal lines in ideal case. In real application, due to design restrictions, there might be a compromise needed between the best SI and ESD performance. We studied several options for two different packages SOT23 and DFN1006BD, see Fig. 15. The best compromise are option C for SOT23 and option A for DFN1006BD - A (see Table 2).



Especially important is the routing to and from the ESD device. There are different options for the SOT23 and DFN1006BD. The pros and cons are shown in Table 2 below.

Fig. 15. Routing options of an Ethernet network on PCB including the entire circuitry

Table 2. Rating of routing options for SOT23 and DFN1006BD

	SOT23			DFN1006BD	
Routing option	A	B	**C**	**A**	B
SI	↓	↑	↑	↑	↑
ESD	↑	↓	↑	↑	↓

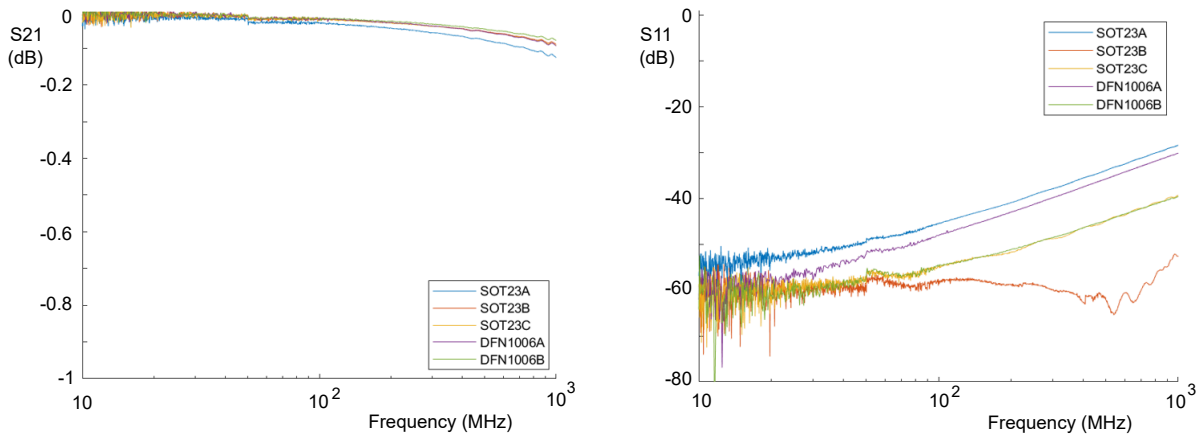


Fig. 16. S-parameters of SOT23 and DFN1006BD footprints

When routing from the connector to the IC, changing layer should be avoided due to SI issues, especially for high-speed interfaces.When the ESD protection device cannot be placed on the same layer as the corresponding IC, the routing should be done over the pad of the ESD protection device to ensure solid ESD operation, as shown in Fig. 17. Please insert an adjacent ground via to provide an appropriate ground reference for the signal transmission.

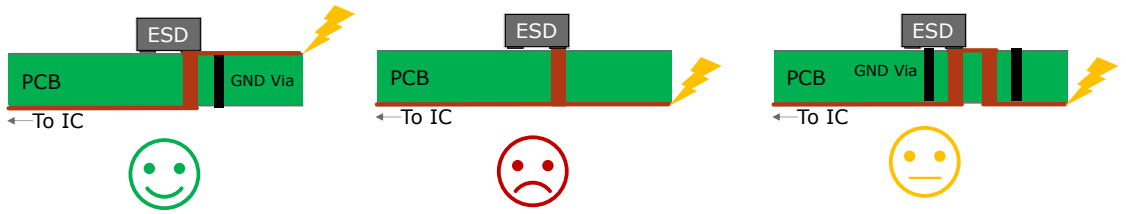
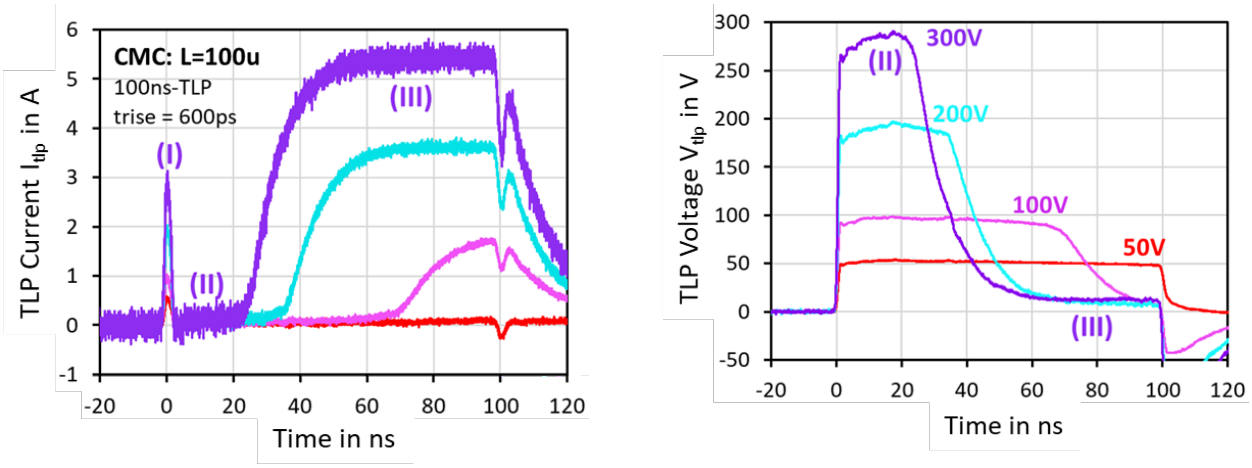


Fig. 17. Routing options when the ESD device cannot be placed on the same layer as the corresponding IC

5. Selection of Common Mode Choke (CMC)

The CMC is a very important component within the Ethernet circuitry. Its initial role (in combination with the CMT) is to block the common mode current and, hence, to prevent electromagnetic emissions (EMI). Prevention of EMI is highly necessary when thinking about the entire topology of the Ethernet system, where the cabling between the nodes is done using unshielded twisted pair (UTP) cables. These cables are usually placed in a bundle adjacent to other cables used within the car. This situation introduces a potential high risk of common mode induction into the cables harness. As mentioned in Section 3 this may lead to high voltages resulting in 100 V trigger requirement for the ESD protection device. Moreover, this phenomenon also introduces the need for a CMC to reduce the EMI.

The additional role of CMC is to protect the circuitry, especially the IC, against entering currents. In combination with the external ESD protection device, an optimal synergetic effect can be achieved. CMC behavior, during single-ended excitation as it can happen during ESD event, can be observed using the TLP measurement method, as shown in Fig. 18.



Phase (I) represents a measuring artifact from TLP; phase (II) shows the blocking behavior; phase (III) shows the end of the blocking phase and the start of the saturation of the CMC.

Fig. 18. Current and voltage response of a typical CMC for 1000BT1 applications based on TLP measurements

The first peak in the current (phase I in Fig. 18) is partly associated with parasitic capacitance of the choke, during TLP measurement. It is however overlayed completely by measurement artifacts of the applied TLP method [6]. The inductive nature of the CMC defines its blocking regime, where CMC tends to block the entering transient pulse for a short period of time (phase II in Fig. 18) until it becomes saturated. The duration of the blocking regime is strongly voltage and time dependent. In phase III, the CMC loses its inductive behavior, goes into saturation and starts to conduct the current. Important aspect here is that the higher the pulse voltage, the faster the CMC will go into saturation. This aspect will be considered again in Section 6.

The higher the voltage the faster the CMC is driven into saturation. This phenomenon can be clearly observed when looking at the saturation times shown in Fig. 19 for CMCs with different inductances.

An additional factor is the package, or the size of CMC. Further investigation comparing TLP plots of CMCs with the same inductance but in different packages show that the blocking voltage is roughly doubled when using 1812 compared to 1210. The reason for this behavior might be a larger ferrite volume.

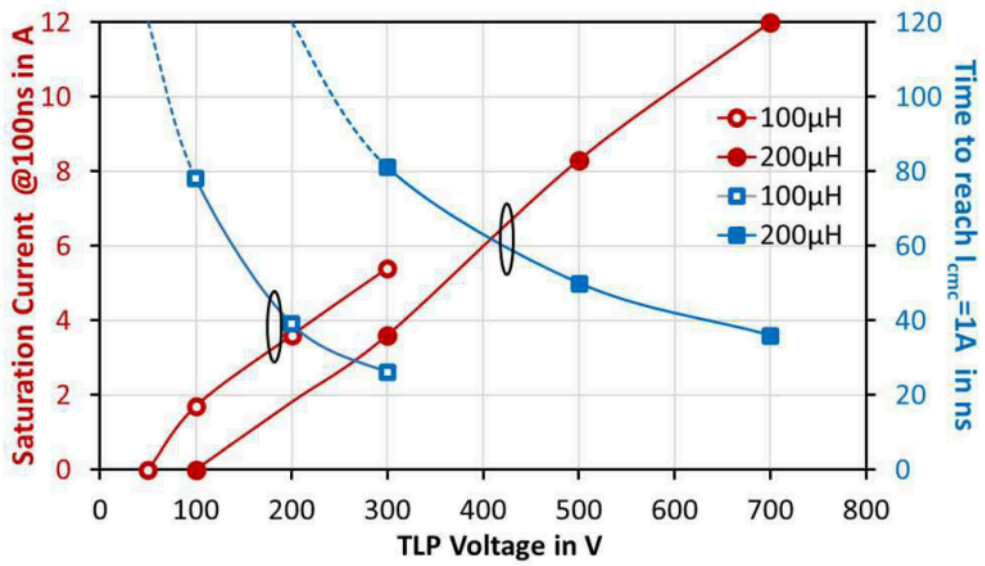


Fig. 19. Saturation behavior of two CMCs with different inductances

Based on these results, Table 3 gives some of our recommendations when choosing a CMC for automotive ethernet applications.

Table 3. Minimum and recommended CMC inductance values for automotive Ethernet applications

Application	Minimum L	Recommended L
10Base-T1s	100 µH	200 µH
100Base-T1	100 µH	200 µH
1000Base-T1	80 µH	100µH (200 µH)

If there is enough SI margin, a better practice is to use CMCs in a larger package having more ferrite material and therefore higher blocking capability.

6. Silicon-based and other ESD technologies

Besides well-established silicon-based technologies, there are several other technologies with a high trigger behavior. The most popular is the varistor-based technology where a specific ceramic material is used to create a Zener-like IV-curve, see red curve in Fig. 20 (competitor 1, red). However, missing snapback the varistor can only provide a very high clamping voltage. At 20 A, this difference to PESD2ETH1GXT-Q is around 300 V. This is a more than significant increase which leads to almost instant saturation of the CMC and, hence, the residual current is far beyond the limits as shown in Fig. 21.

Other suppression technologies (polymer or ceramics) include the snapback but require a more than double trigger voltage. Fig. 20 (Competitor 1 and 2, green and turquoise) shows that the trigger voltage is up to 440 V which is rather high and leads to a significant current overshoot clearly violating the limits (Fig. 21). Although these measurements were done including the full ethernet circuitry (including the CMC), those high trigger and clamping voltages drive any typical CMC into saturation very quickly and hence, the blocking capability of the CMC cannot perform out its beneficial role. As a result, the voltage and the current on the IO Pin of the PHY will increase significantly, exceeding the limits and potentially destroying the PHY.

It should be mentioned again that all devices of the PESDxETHxy-Q Series from Nexperia show very similar behavior as the PESD1ETH1GXLSQ shown in Fig. 21. At Nexperia, the ESD discharge current measurement is included in the qualification and release process.

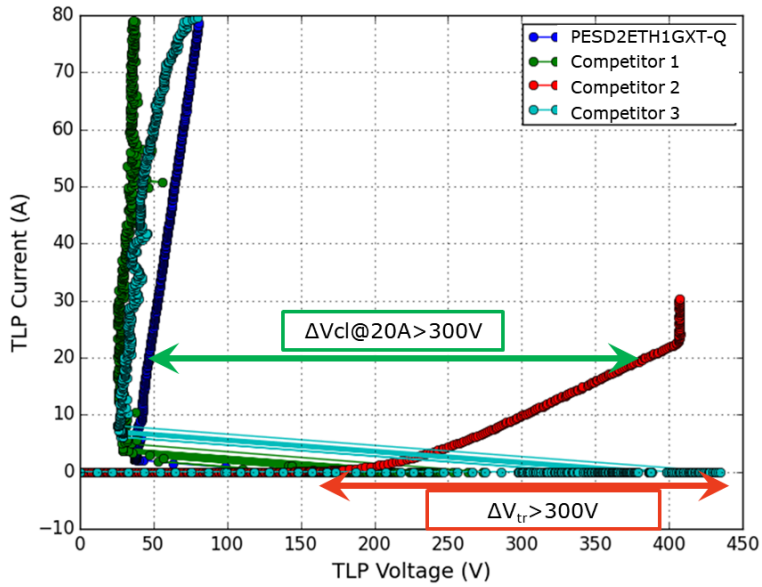


Fig. 20. TLP comparison of PESD2ETH1GXT-Q with three different competitors

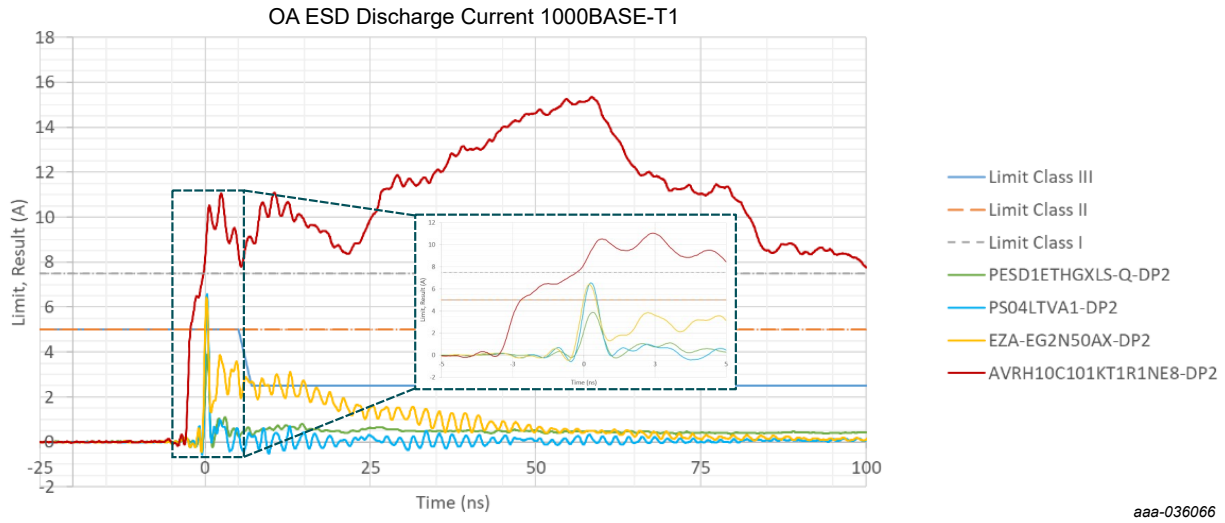


Fig. 21. ESD comparison of PESD2ETH1GXT-Q with three different competitors

7. Future outlook for automotive Ethernet applications

Besides already established 100BASE-T1, 1000BASE-T1 applications and specifications, there are some alternative views, especially on the topology. Closer look in the EMC behavior of the UTP shows that compared to shielded cables the emissions are significantly higher. This might be not strictly critical but for some applications this might lead to serious issues e.g., for car antennas especially at FM and DAB band, as discussed by Rosenberger [7]. For this reason, also shielded cables such as shielded twisted pair (STP) can be used. This will directly influence the requirements on the topology. Firstly, no CMC will be needed since the common mode coupling is mitigated by the shield of the cable. Secondly, due to shielded cables the 100 V requirement on the trigger voltage disappears. The ESD protection device need to have low trigger and lowest clamping behavior with V_{rwm} in the range below 10 V (typically 5 V, 3.3 V or even below).

Automotive Ethernet is continuing to grow and is increasing the number of available protocols. There are basically two different extensions. The first new protocol is 10BASE-T1S and it is suitable for lower data rates. It will fill the gap between the Ethernet and CAN application in the range of 10 MBps. 10BASE-T1S is planned to include most of the benefits of Ethernet protocols while being a low-cost system. The main bus topology and the cabling using UTP will remain the same as for e.g., 1000BASE-T1. Since the circuitry will also be very similar to the 100BASE-T1 (see Fig. 3) the requirements on ESD protection will basically be the same. An important difference is a strong requirement on the device capacitance which is due to high capacitive load of the entire bus topology which could include up to 50 nodes. The capacitance range will be in the range of 0.5 pF.

The second new protocol is MGB-T1 and it extends the Open Alliance automotive ethernet family to higher data rates of 2.5/5/10 Gbps. They are already under discussion within the OPEN Alliance committee. The bus topology will be different from 100/1000BASE-T1. There will be stringent requirements on SI and EMC, hence, shielded cables will be used. The usage of CMC is also under open discussion. In the configuration with shielded cables and without a CMC (in worst case) the ESD device should be matched to the on-chip ESD protection of the PHY. SI will be a even more dominant factor in the MGB.T1 applications because of high data rates. Low device capacitance in combination with a compact package with reduced parasitics should be used here to pass the strong requirements on SI.

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9. Revision history

Table 4. Revision history

Revision number	Date	Description
1.1	2023-02-21	Fig. 16 corrected.
1.0	2023-01-30	Initial version.

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