AN90037

NXS0506 SD-card voltage level translator

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Document information

Information	Content
Keywords	SD-card voltage level translator, data transfer, wi-fi module, PCB design
Abstract	This application note describes the NXS0506 SD-card voltage level translator and explains important operating principles.

1. Introduction

The evolution of Complementary Metal–Oxide–Semiconductor (CMOS) process technologies has been a significant driver of the electronic industry, enabling a higher scale of integration while maintaining lower levels of power consumption. This improved performance is achieved through the reduction of supply voltage, and improved manufacturing capabilities. However, this comes with its fair share of challenges, as the decreased feature size increases susceptibility towards damaging ESD transients and coupled interference.

For High-Speed applications with CMOS, an important design concept is understanding how the fast-edges of transitioning signals will affect signal integrity. Interference or signal artifacts like crosstalk, ringing, overshoot, and electromagnetic interference (EMI) can degrade performance. To circumvent these issues, recommended PCB layout guidelines should be employed.

The purpose of this document is to provide the reader with design applications with NXS0506 SD-card voltage level translator and explain important operating conditions and PCB layout strategies and considerations.

The information in the next few sections of this document displays different designs with the NXS0506 and describes the different requirements for proper operation.

2. NXS translators − brief overview

The NXS is a bidirectional translator capable of multi-voltage level translation. It features an internal pass transistor and additional one-shot circuit that is used to accelerate rising edges of the input signals. After the accelerated rise ramp, an internal 10 kΩ pull-up resistor lifts the output voltage of the channel to its respective pull-up voltage.

3. Typical application – SD-card

Fig. 1 illustrates a typical application that consists of a host processor, such as a baseband processor of a mobile device or SOC. In this application, the translator is designed to operate between the SD-port of the host system and SD-card.

3.1. Voltage supplies

There are a total of three supply rails required for proper operation.

1. The first supply, V_{CCA}, is the Host system I/O voltage. This voltage can either be provided independently, or as in the example below, can be shared with the Host.
2. V_{CCB} is supplied directly to the level translator, NXS0506. The value of this supply should be selectable, with a value of either 3.3 V or 1.8 V. Both voltages need to be available on systems that support the 1.8 V mode – these cards are initially accessed with supply values of 3.3 V.
3. The third voltage, V_{SD}, is the supply rail that is directly connected to the SD-card. This voltage value is fixed at 3.3 V and is independent of the card operating mode.

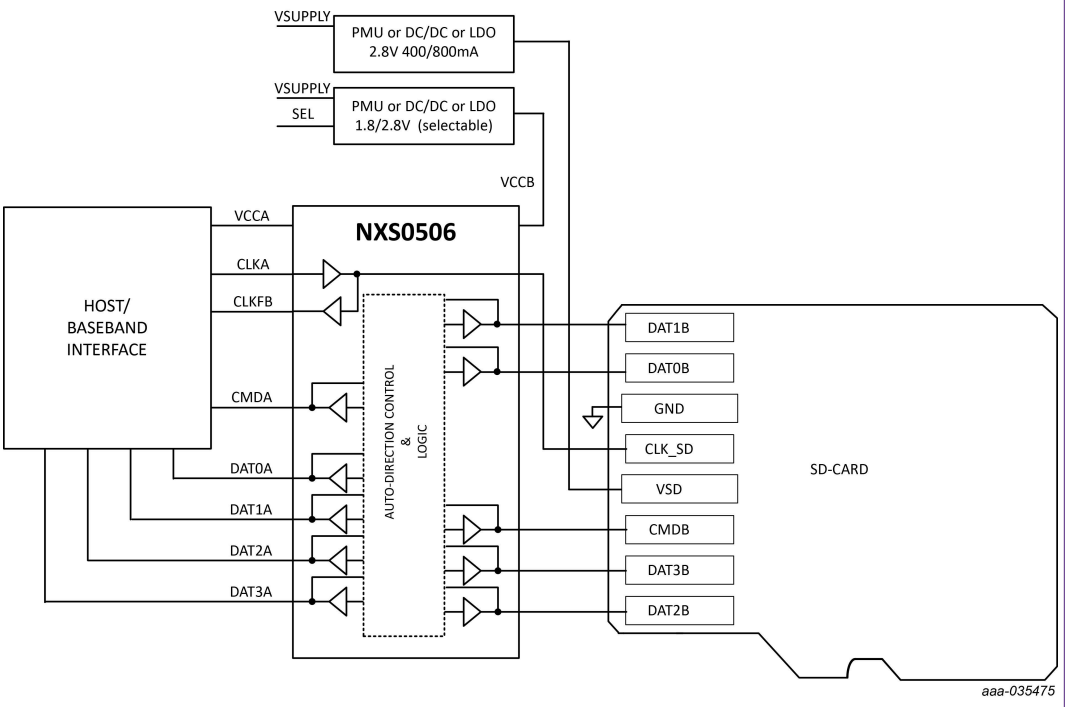


Fig. 1. SD-card application

3.2. Card side I/O voltage generation

The first important consideration for translation applications is the I/O voltage range – the host (or BaseBand Interface) system I/O must match the corresponding host translation port.

In Fig. 1, it is shown that the V_{CCA} supply is shared by both the HOST and V_{CCA} of NXS0506. However, PORTB must have a supply that is independent of the one produced for the SD-CARD. This is required when transitioning from DS/HS to UHS-I mode, as the I/O voltage on the external port must change from 3.3 V to 1.8 V, while the SIM card supply voltage remains at 3.3 V. This is accomplished through a power management system capable of switching between two independent supply voltages. For example, for SD-card protocol, it is common for the V_{CCB} supply to change externally from two independent supplies, 3.3 V and 1.8 V, through a dual voltage LDO or DC/DC converter. This can also be accomplished by controlling the supply values through a Precision Measurement Unit (PMU).

3.3. Data transfer mode and capacitive load

To ensure proper operation, especially at the highest speeds of the different data transfer modes, the design must follow SD-card standards for capacitive loads. These requirements depend on the bus operating conditions, such as the driver type and transfer mode.

For DS and HS modes with 3.3 V signal voltage, and with a single card connected, the total bus capacitance C_L is defined as $C_L = C_{HOST} + C_{BUS} + C_{CARD}$. The maximum limit for C_L is 40 pF with $C_{HOST} + C_{BUS}$ having a maximum value of 30 pF, which would allow a maximum value of 10 pF for C_{CARD}.

For the higher speed UHS and DDR modes with 1.8 V signaling voltage, C_L is defined as $C_L = C_{CARD} + C_{EQ}$. C_{EQ} is the equivalent (lumped load) capacitance of all PCB and interconnecting components between the host and the card. The maximum value for CL is defined as 30 pF for UHS50 and 15 pF for UHS104 modes with Type B driver strength.

The NXS0506 is designed to meet these requirements and provide the interface between Host and SD-card. NXS0506 is designed to meet the load capacitance requirements of the host side interface and it can drive the required load capacitances on the card side. For reference, the load capacitance C_L used throughout the NXS0506 datasheet refers to the capacitance that is externally

added to the level translator. $C_L = C_{EQ} + C_{CARD}$ on the card side and $C_L = C_{EQ} + C_{HOST}$ on the host side.

Another parameter defined in the NXS0506 datasheet is the bus signal equivalent capacitance $C_{I/O}$. This value represents the capacitance of the integrated EMI filter, however this value does not reduce or impact the budget of the load capacitance that can be applied externally. To further clarify, $C_{I/O}$ is part of C_{HOST} for the card side interface and C_{CARD} for the host side interface.

3.4. CLK_FB

As illustrated in Fig. 1, the system clock, CLKA, is transmitted from the host to the SD-card. The voltage translator and PCB traces create some amount of delay that reduces timing margin for data read back from the SD-card. This reduced margin is proportional to data rates, therefore increased data rates will further reduce timing margin for proper read back. A feedback path is introduced, shown as CLKFB, to compensate for this delay. Therefore, proper synchronization of the Host clock, through CLKFB, with data from the SD-card results in proper readback.

3.5. Wi-Fi modules and chipsets

Many microcontrollers and SOCs offer an interface to connect to Wi-Fi modules or chipsets. These interfaces often use the SDIO protocol. As SDIO is part of the SD-card standard the NXS0506 voltage level translator can be used in cases where the host processor IO voltage is different from that of the Wi-Fi chipset. Fig. 2 displays a simplified diagram of the interface between host and Wi-Fi module. Wi-Fi speeds of 300 Mbit/s can be transferred with SD 3.0 mode SDR104 (104 MB/s) @ 208 MHz clock.

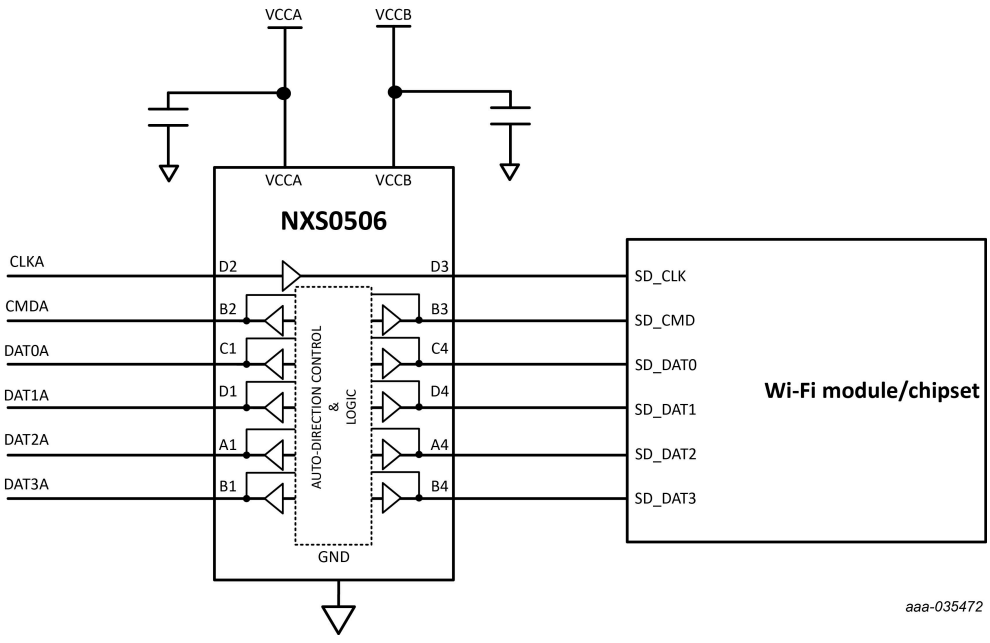
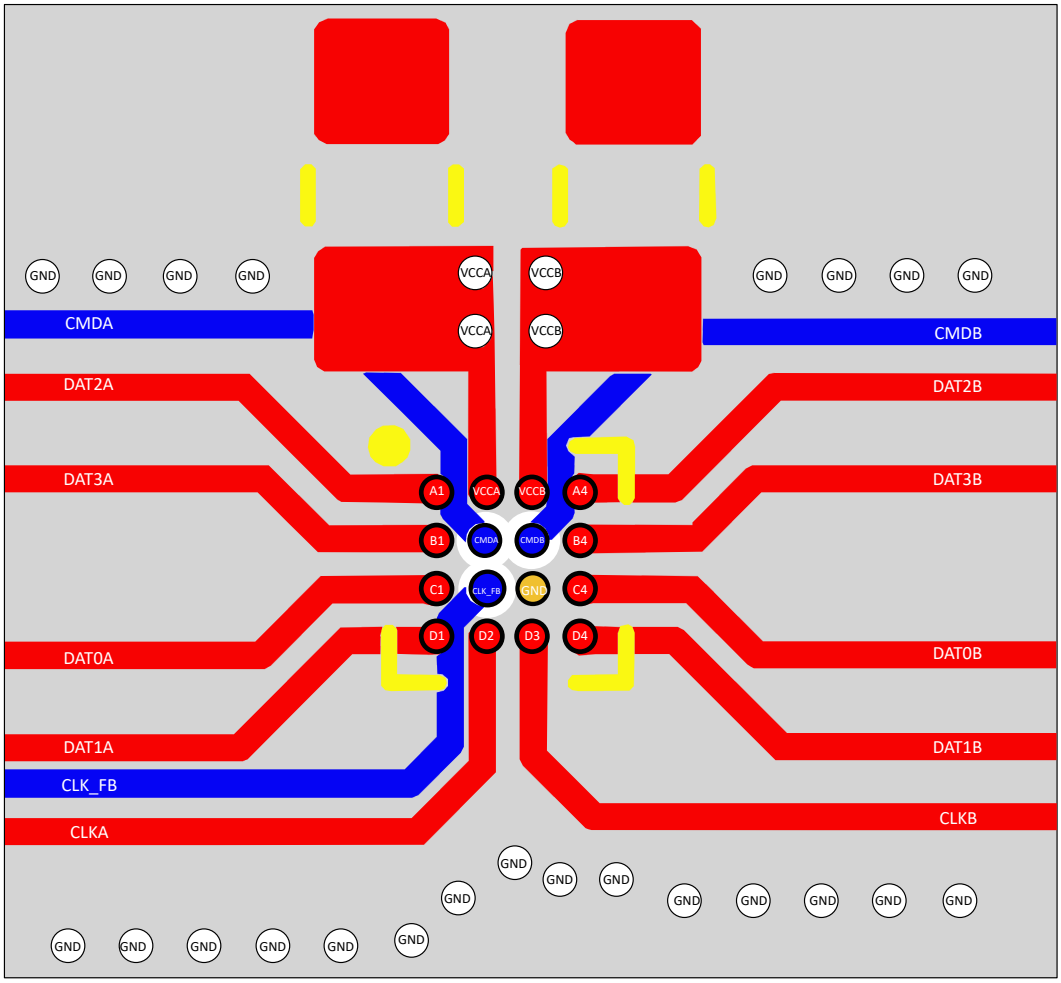


Fig. 2. Typical application with wi-fi module

4. PCB design guidelines

The high-speed signals for the SD-card interface include signals DATB[3:0] CMDB and CLK. To ensure signal integrity with minimal distortion due to reflections and interference, these signals must be routed in a microstrip fashion, where all signals are routed above a uniform ground plane. Any breaks in the plane below these traces result in increased loop impedance and may create unwanted artifacts such as reflections.



1st layer: Signal (red); 2nd layer: GND (light grey); 3rd Layer: Power (not shown); 4th Layer: Signal (blue)"

Fig. 3. NXS0506UP layout

5. Bypass capacitors

As with all integrated devices, proper bypassing should be included to ensure stable supply voltages. These supply terminals should be bypassed to ground with low ESR ceramic bypass capacitors. It is common practice to use two different values to ensure proper filtering of low-frequency and high-frequency transients. These include a 10 uF ceramic and a smaller 0.1 uF capacitor that is generally placed closer to the device. Placing the capacitor as close to the translator pins will ensure minimal loop inductance between the supply pins. NP0 and X7R are recommended, due to their optimal performance across temperature, and very low dissipation factor. To reduce neighboring crosstalk of traces, shielding can be employed, however it should be noted that this would introduce some parasitic capacitance to the high-speed net.

6. PCB stackup and routing

Using a four-layer board with a dedicated power and ground plane is recommended. To minimized loop inductance all high-speed nets should travel across a uniform ground plane. This ground plane should be adjacent to the signal layer – any breaks in the ground layer will increase the loop area and impact performance. An example would be high-speed nets on layer 1, with uniform ground on layer 2.

To reduce signal coupling a minimum trace-to-trace spacing value of 125 µm is recommended. Due to the narrow pitch, 350 µm, of NXS0506UP, connecting the 4 inner pads requires plated u-vias with a minimum drill of 150 µm.

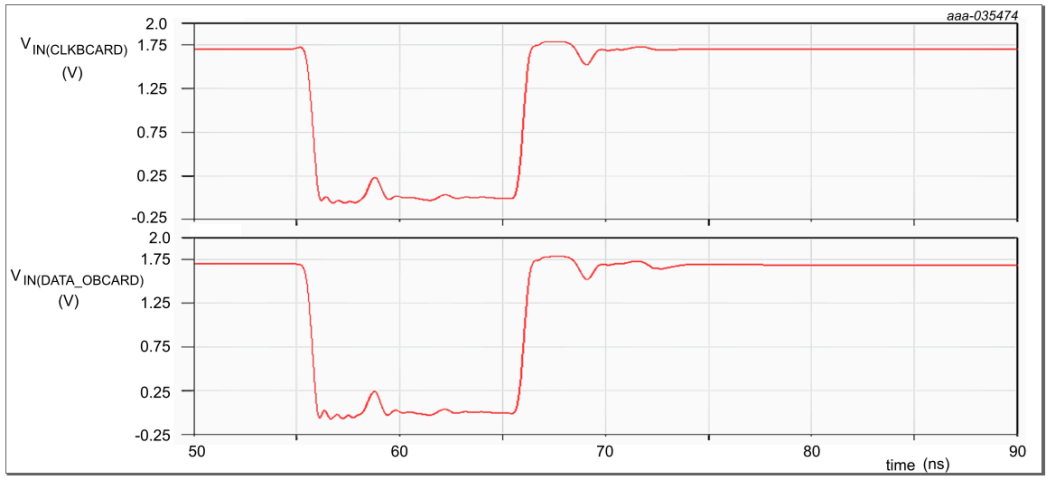
Fig. 3 shows an example layout for NXS0506UP.

In addition to these, the following rules should be observed:

- Net trace width should not change during span of length, as this would impact impedance and performance of net.
- Net traces should only have serpentine or 45° bend. Sharper bends, such as 90° should be avoided.
- Incorporate length matching across all nets to match impedance, which will reduce skew across nets.
- Avoid placing closely grouped vias, as this could impact return current path. Alternatively, place the vias in a staggered grid fashion.

6.1. Signal line impedance simulated results

For optimal results, simulation has shown that using a line impedance of 20-30 Ω results in less noise and ringing due to reflections on the signal line.



Z_{line} = 20 Ω at V_{CCB} = 1.7 V.
Impedance larger than 50 Ω may result in increased noise

Fig. 4. Signal impedance

7. Revision history

Table 1. Revision history

Revision	Date	Modifications
1.0	20220922	Intial version

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