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Resistor Equipped Transistors (RETs): Key parameters and application insights

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Document information

Information	Content
Keywords	RET, polysilicon resistors, digital transistor, pre-biased transistor
Abstract	This application note explains specific product and application aspects of Resistor Equipped Transistors (RETs)

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1. Introduction

Bipolar transistors are controlled via the base current applied. Because of high temperature dependency of the voltage drop across the base-emitter path, it is required to add at least a series resistors at the base for stable and safe operation of a transistor in most applications This is required to keep base current at a desired level.

To reduce the number of components and to make board designs less complex, Resistor-Equipped Transistors (RET) have been introduced. These are single or dual transistors with resistors integrated on the same die. The integrated resistors have higher tolerances than commonly used external resistors. This fact makes RETs most suitable for switching applications where the transistor operates either in on-state or off-state. This is the reason also, why RETs are often referred to as digital transistors.

2. RET basics: topologies and nomenclature

RETs are available with NPN and PNP transistors. The most simple resistor configuration is a series resistor applied at the base as shown in Fig. 1. Another option are RETs with a base divider. Then there is a base series resistor R1 integrated and a second resistor R2 in parallel to the base-emitter path.

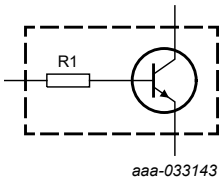


Fig. 1. NPN RET with base resistor R1

Fig. 2 shows this topology with the base divider integration of R1 and R2. Both topologies can be found for PNP transistors as well of course.

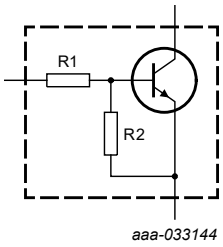


Fig. 2. NPN RET with base divider R1 and R2

For R1 the value can be chosen from a list starting at 2.2 kΩ. Additional options are 4.7 kΩ, 10 kΩ, 22 kΩ and 47 kΩ. R2 option list starts with 10 kΩ with the additional choices of 22 kΩ and 47 kΩ. For the ratio of the resistors there are several options from R2/R1 equal 1, 2.13, 4.55, 10 and 21.

Table 1 explains the nomenclature for single RETs. An example type name is NHDTA124ET which can be decoded with the table below. Most important is the character indicating the Bipolar Junction Transistor (BJT) type and collector current rating. The current clusters are lower or equal higher than 500 mA. The characters A and B stand for PNP device whereas C and D are used for NPN types. For the base resistor network, the series resistor R1 is defined by a base number followed by a multiplier indication number. The character that follows informs the resistor ratio R1/R2. Finally there is a character which tells the package variant. RETs are available in conventional leaded packages such as SOT23 and SOT323 but also in leadless packages like SOT1215 which is a DFN1010 or SOT883 which the same as DFN1006 so a 1 mm x 0.6 mm device.

Table 1. Nomenclature single RETS

1st letter Company Indicator	2nd letter Voltage Indicator	2nd3rd letter	Polarity and Current	1st number	Base number for R1	Multipler for R1	Resistor Ratio R2/R1	Package Indicator
N = Nexperia	H = high voltage	DT = Digital Transistor	A = PNP, < 500 mA	1 = no meaning	1 =1	3 = x 10E3	T = R1 only	T = SOT23
P = Philips (legacy)		BR = Low V_{CEsat}RET	B = PNP, ≥ 500 mA		2 = 2.2	4 = x 10E4	E = 1 R1 = R2	U = SOT323
			C = NPN, < 500 mA		4 = 4.7	5 = x 10E5	V = 0.213	M = SOT883
			D = NPN, ≥ 500 mA		Comp. only:	Comp. only:	W = 0.46	MB = SOT883B
					3 = 3.3	2 = x 10E2	X = 2.13	QA = SOT1215
					5 = 5.6		Y = 4.55	QC = SOT8009
							Z = 10	QB = SOT8015

Table 2 shows an equivalent table for dual RETs. The naming structure is quite different from the one for single RETs. Very important is the 3rd letter which informs the topology of the dual RET, so if two NPNs or PNPs or a complementary pair can be found in the device.

Table 2. Nomenclature Double RETs

1st letter Company Indicator	2nd letter Voltage Indicator	Package Indicator	2ndletter	3rdletter	Number(s)
N = Philips (legacy)	H = High voltage	I = SOT457	M = no meaning	B = 2 x PNP	Consecutive numbering
P = Nexperia		U = SOT363		C = NPN/ PNP ≥ 500 mA	
		E = SOT666		D = NPN/PNP	
		Q = SOT1216		H = 2 x NPN	
		R = SOT1268		N = 2 x NPN >0 = 500 mA	
				P = 2 x PNP 500 mA	
				T = 2 x PNP	
				X = 2 x NPN	
				Z = NPN/PNP	

3. Application Examples

RETs are used as switches mainly, thus in the two states “on” and “off” This is why they are referred to as digital transistors often. A basic example is shown in schematic diagram in using an NPN-RET with integrated base series resistor. V1 is the control voltage and provides the base current for the BJT. If V1 is below Voff the transistor is turned off. Vout is almost equal to V2. Once V1 reaches the turn-on level, base current flows and Vout decreases. The switch changes into the on-state and Vout becomes equal to V_{CEsat}.

The circuit has the behavior of an inverter with voltage translation. V2 can be chosen within the datasheet limits of V_{CE} of the chosen RET. The output voltage swing can be higher and lower than the control voltage V1. So voltage translation can be in provided up and down direction.

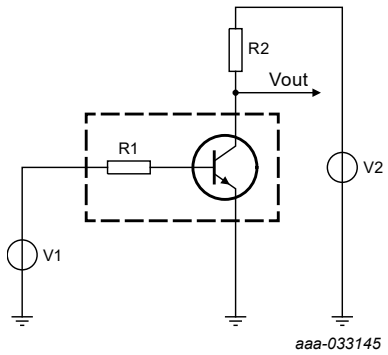


Fig. 3. Basic control BJT circuit with an NPN-RET

Fig. 4 is the equivalent circuit created with a PNP-RET. The control voltage V1 has to be negative against the emitter of Q1 to get the RET turned on.

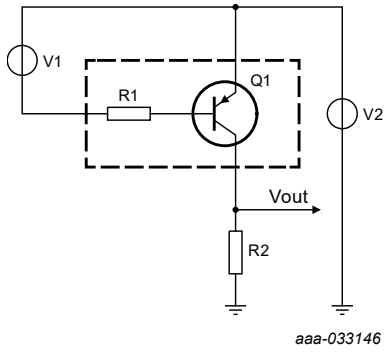


Fig. 4. Basic control BJT circuit with an NPN-RET

A very common load switch application with RETs in depicted in Fig. 5. The BJT Q2 switches the load current through the load resistor RL. Q2 conducts if Q1 is turned on. The control RET Q1 requires a positive base voltage to enable the load switch. The topology does not require high base current nor high voltages for the control signal. Q2 can switch higher load voltages in compliance to the rating of the chosen component (≤ 80 V) and also comparably high load currents of up to 500 mA. Low V_{CEsat} RETs also called **P**erformance-**B**ased **R**ETs (PBR), provide low residual collector-emitter voltages in on-state and therefore achieve high power-efficiency of the load switch. For RET Q2 a product with a base resistor divider achieves a far better turn-off performance compared to a RET with a series resistor in the base-path only. R4 accelerates turn-off time significantly because Q2 is driven by an open-collector stage realized by Q1

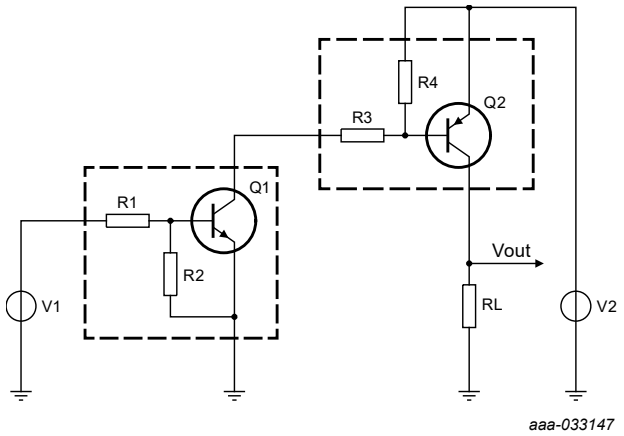


Fig. 5. Load switch with PNP RET in load path and NPN RET in control path

RETs can be used to combine multiple control signals towards one control signal output. Fig. 6 shows two input signals V1 and V2 as base drive for two RETs that share one collector resistor. This circuit behaves like a NOR logic function. If one of the inputs is at high level or both, the output is providing a low state. Only if both input signals are low the output provides a high-level signal. The advantage of such RET solution against a standard logic gate is that the output can support high voltages up to 80 V that cannot be found for logic families. The input drive can also be designed very flexible via the selection of a suitable base resistor or base voltage divider. If required, the NOR function can be changed into an OR function by adding an inverter stage as shown in Fig. 1 behind the output of the discussed circuit.

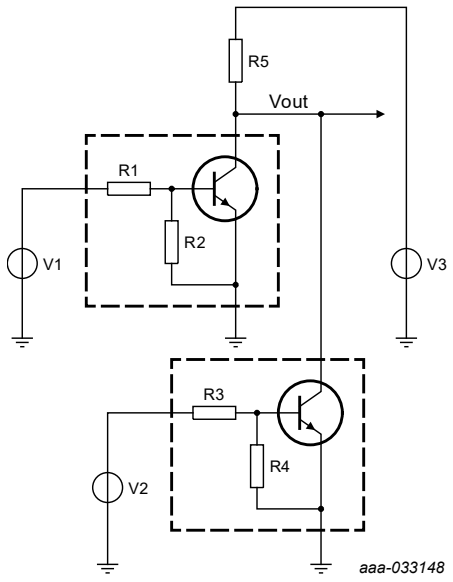


Fig. 6. RETs in wired-NOR application

In a similar way, a NAND function can be implemented if RETs are connected in series for the collector-emitter path like shown in Fig. 7. Only if both RETs are turned on at the same time, the output signal Vout provides a low level. If the output is inverted by another RET, an AND function has been created.

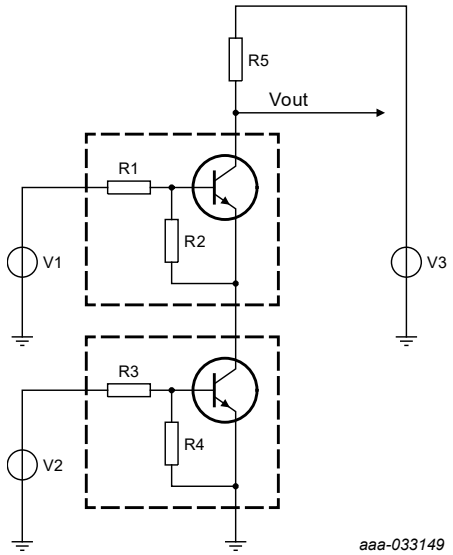


Fig. 7. RETs in wired-NAND application

In Fig. 8 an application example for a push-pull stage is shown. The circuit is powered by two voltage sources V2 and V3, providing a negative and positive polarity supply. Vout is terminated to ground via Rload, which is the connection between the two voltage sources. Q1 and Q2 work as emitter followers and amplify current provided by the input source V1.

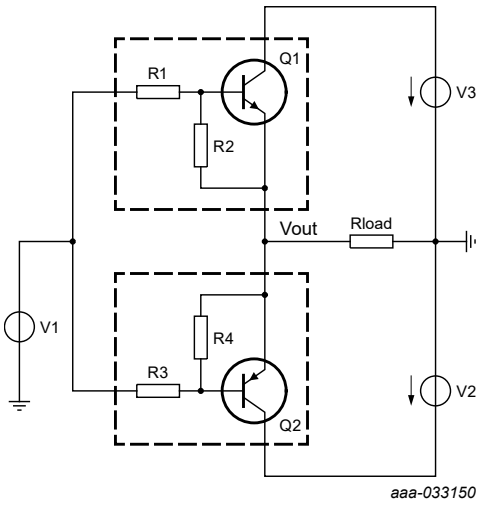


Fig. 8. Application example push-pull stage with RETs

4. Data sheet parameters

In this chapter the Nexperia data sheets for RETs are explained in detail. The major focus is on the electrical parameters. For the discussion in this chapter a rather new Nexperia high voltage RET has been chosen from an 80 V product series for reference.

The first chapter is the “General Description”. It informs the BJT polarity of the RET and the packages available. Table 3 shows the product overview with the resistor variants R1/R2 of the chosen component. The complementary parts are mentioned if applicable.

Table 3. Product overview

Type number	R1	R2	Package		PNP complement:
	kΩ	kΩ	Nexperia	JEITA	
NHDTC114EU	10	10	SOT323	SC-70	NHDTA114EU
NHDTC124EU	22	22			NHDTA124EU
NHDTC144EU	47	47			NHDTA144EU

A list of “Features and benefits” follows in the next section with. The major features like current capability, high break down voltage and automotive qualification are mentioned here.

Features and benefits

- 100 mA output current capability
- High breakdown voltage
- Built-in resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

The following section informs major application areas, . These are digital or switching applications as discussed in more detail the prior chapter.

Applications

- Digital applications
- Cost saving alternative for BC846 series in digital applications
- Controlling IC inputs
- Switching loads

“Quick reference data” are depicted in a brief table with electrical key parameters such as maximum allowed V_{CE0} and output current I_O.

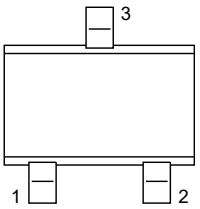
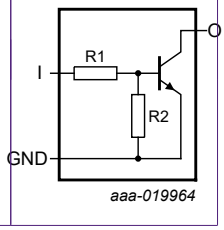
Table 4. Quick reference data

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	80	V
I_O	output current		-	-	100	mA

The pinout of the RET is informed with the emitter, collector and input connections as shown below. The input pin is also referred to as base although there are resistors integrated in between.

Table 5. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)		
2	GND	GND (emitter)		
3	O	output (collector)		

The next section contains the ordering information.

Table 6. Ordering information

Type number	Package		
	Name	Description	Version
NHDTC114EU	SC-70	plastic surface-mounted package; 3 leads	SOT323
NHDTC124EU			
NHDTC144EU			

The marking table in informs the marking of the devices. The last character “%” is a placeholder for the manufacturing site.

Table 7. Marking

Type number	Marking code [1]
NHDTC114EU	5M%
NHDTC124EU	5Q%
NHDTC144EU	5S%

[1] % = placeholder for manufacturing site code

The limiting values follow in the next section of the RET data sheet in Table 8.

V_{CB0} is the maximum collector-base voltage with an open emitter pin. V_{CE0} is the maximum allowed collector-emitter voltage with an open base. For a RET where a resistor is placed between base and emitter it could be called V_{CER} as well because the input of the RET is open, but not the base of the BJT. There is the relation to be considered for the breakdown voltage of the collector-emitter path of a BJT as shown below:

$V_{CES} \geq V_{CER} \geq V_{CE0}$

V_{CES} is tested with the base being short-circuit to the emitter. For RETs the integrated resistors are not taken into account for the nomenclature of parameters. Despite of integrated resistors the term V_{CEO} is used still. This is important to be taken into account for other key parameters as well like leakage current ratings.

V_I has a maximum rating of 10 V for the example data sheet of a PNP RET with a divider ratio of 1. The BJT as a stand-alone device would have the limitation of V_{EB0} = 5 V. Due to the input divider this value is doubled. The base-emitter diode is driven reverse and therefore does not conduct below the limit value. For further details please refer to chapter 5.

For the other polarity of V_I, base current flows, so there is a forward voltage drop across the base-emitter diode to be considered whereas the rest of the input voltage is present at the base series resistor R1. The voltage limit is mainly defined by the maximum power dissipation of the integrated resistor R1. Therefore maximum base current is limited by R1 and thus V_I.

Total power dissipation P_{tot} is informed for two mounting conditions. One is meant for a single layer FR4-PCB using a standard footprint. The second value is provided for a 4-layer FR4-PCB, where bottom layer and the inside layers are solid copper planes.

Table 8. Limiting values

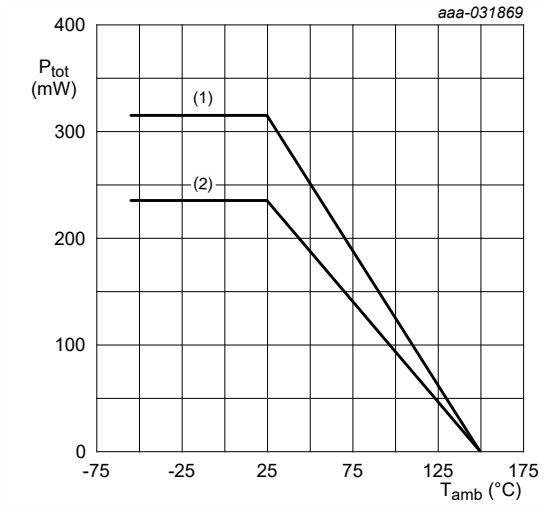
In accordance with the Absolute Maximum Rating System (IEC 60134).

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	80	V
V_{CEO}	collector-emitter voltage	open base		-	80	V
V_{EBO}	emitter-base voltage	open collector		-	10	V
V_I	input voltage					
	NHDTC114EU			-10	+40	V
	NHDTC124EU			-10	+60	V
	NHDTC144EU			-10	+80	V
I_O	output current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	235	mW
			[2]	-	315	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit-Board (PCB); single-sided copper; tin-plated and standard footprint.
[2] Device mounted on an FR4 Printed-Circuit-Board (PCB);4-layer copper; tin-plated and standard footprint.

The maximum junction temperature for gold wire products is 150°C because otherwise the alumina layer of the bond wire joint would be consumed up by diffusion processes of the alumina into the gold. For longer exposure to temperatures above 150°C the wire joint becomes unstable and can fail. Copper wire products can be specified up to 175°C. Storage and ambient temperature have the same limits. With rising ambient temperature the maximum power that can be applied degrades with a linear curve as shown in Fig. 9 below. A RET which is designed for Tj(max) = 175°C has a derating curve which reaches the x-axis at 175°C, so higher power can be dissipated comparably.



(1) FR4 PCB, 4-layer copper, standard footprint

(2) FR4 PCB, single-sided copper, standard footprint

Fig. 9. Power derating curves SOT323 (SC-70)

Further thermal characteristics are provided in Table 9 in the example RET data sheet. Thermal resistance R_{th} is informed for different mounting conditions. The values provided could also be calculated from the related P_{tot} ratings in Tab. 6 with:

$R_{th(j-a)} = (T_{j(max)} – 25°C)/P_{tot}$

For example for $R_{th(j-a)}$ the calculation delivers:

(150 °C - 25 °C)/0.235 W = 532 K/W

Table 9. Thermal characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	532	K/W
			[2]	-	-	397	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	150	K/W

[1] Device mounted on an FR4 Printed-Circuit-Board (PCB); single-sided copper; tin-plated and standard footprint.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), 4-layer copper, tin-plated and standard footprint.

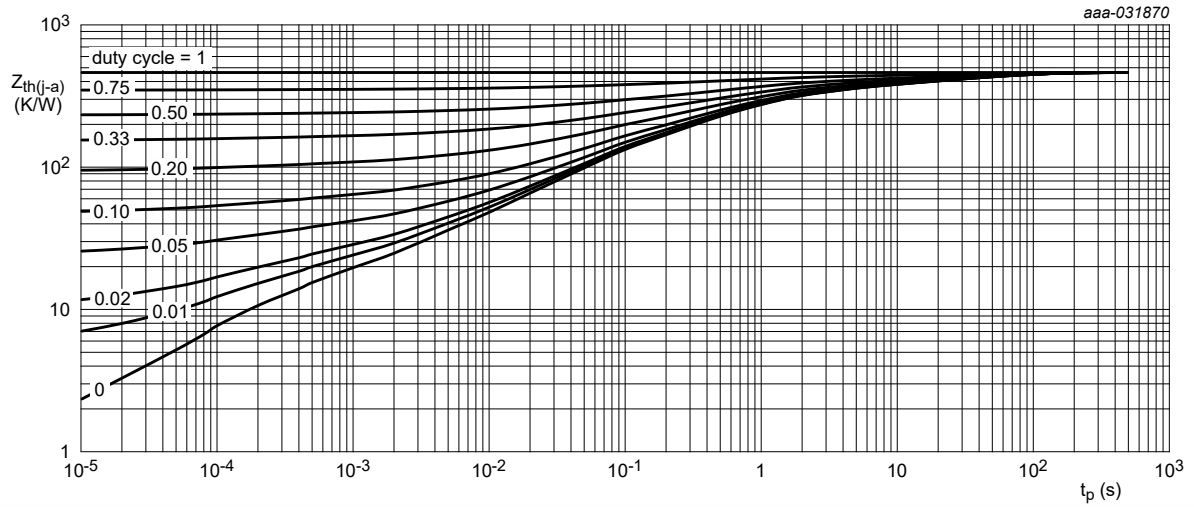
$R_{th(j-sp)}$ is the thermal resistance from junction to the solder point of the pin for the major thermal path of the SMD package discussed. For RETs in SOT23 or SOT323 this is the collector lead. The other two terminals for the emitter and base are connected via bond wires, so they do not contribute to heat dissipation. $R_{th(j-a)}$ informs about the thermal resistance from junction to ambient. This value depends significantly on the mounting condition, for example PCB layout and type as well as copper thickness.

$Z_{th(j-a)}$ is the transient thermal impedance from junction to ambient as depicted in Fig.8 and Fig.9. These diagrams help to calculate a thermal scenario for applications where the RET is not run in DC condition but where it operates in switching mode.

The Z_{th} diagrams are provided for different mounting conditions. Z_{th} is provided versus the pulse length of the on-state for the RET. Curves are depicted for different duty cycles d from single events with d = 0 up to DC mode with d = 1. Duty cycle d is defined as:

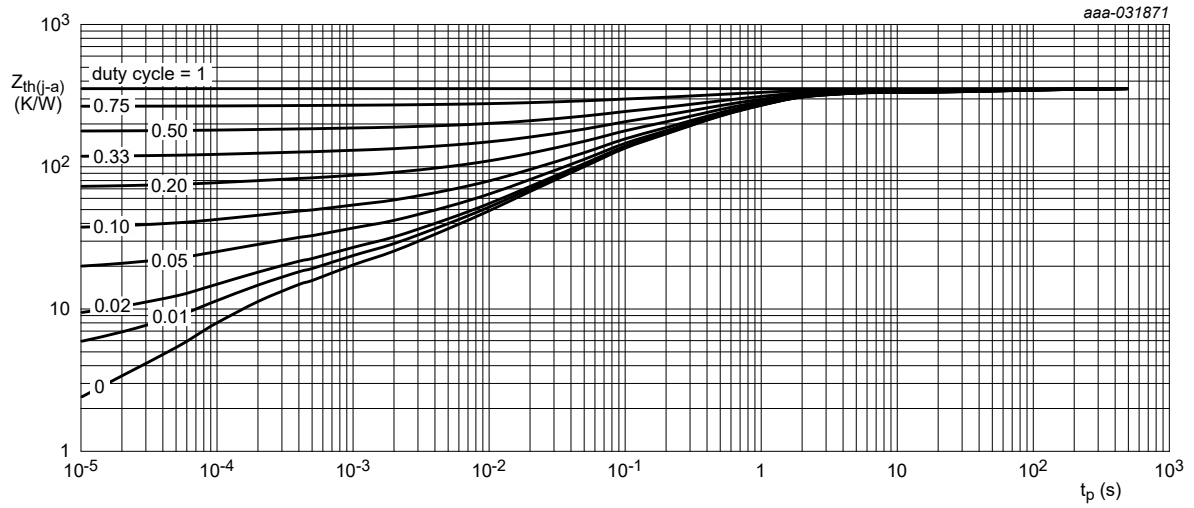
d = ton /T, where ton is the on-state duration and T the cycle time.

The value for the DC-case is identical to the Rth(j-a) parameter in the data sheet. For long pulses with about more than 10 seconds duration rather small SMD components get heated up to the same temperature like for a constant on-state. This is why all curves start at the same level on the right side of the diagrams. If short pulses are applied, the values for Zth are becoming smaller, so higher pulse power can be handled. The curves are getting flat for very short pulses and d > 0.05 in the diagram. This is the case because switching frequency is becoming quite high in this region and the heat generation is averaging out in the crystal. There is almost no time for temperature changes between on-state and off-state.



FR4 PCB, single-sided copper, tin-plated and standard footprint

Fig. 10. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, tin-plated and standard footprint

Fig. 11. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

Every Zth-curve is valid for a specific mounting condition. Fig. 10 represents operation with a standard footprint on a single layer FR4 PCB and 35 µm copper layer whereas Fig. 11 is based on a 4-layer FR4 PCB with the RET mounted on a standard footprint. All other three layers of the test PCB are realized as solid copper areas.

If a very good thermal performance of a board design is required it can be recommended to have an extra thermal pad for the collector on the top layer with about 1 cm² to improve the thermal path into the second layer. The second layer should provide a bigger copper area in order to get heat spread and dissipated via the PCB.

For calculation of the temperature increase of a RET in an application first the pulse power needs to be derived. The Zth-curves are valid for rectangular-shaped power pulses. In many applications the shape of the power pulse can deviate from this. Then it is possible in most cases to convert the measured power pulse into a rectangular pulse with an equivalent pulse power.

The correct Z_{th} value is derived by reading the thermal resistance at the given pulse length t_p in the curve with the relevant duty cycle. The temperature increase of the junction against ambient temperature is calculated then with:

$\Delta T = Z_{th(j-a)} * Pp$ (Pp = Pulse Power in Watt)

$T_{amb} + \Delta T$ may not exceed the defined $T_{j(max)}$ found in the specification.

The next chapter in data sheets of RETs informs the electrical characteristics of the components. Most characteristics are tested at an ambient temperature of 25° C unless another temperature is informed for the test conditions. If the test condition can heat up the device significantly, the related value is measured in a pulsed test mode in order to avoid self-heating.

Table 10. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 100 µA; I_E = 0 A	80	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 2 mA; I_B = 0 A	80	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = 80 V; I_E = 0 A	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 60 V; I_B = 0 A	-	-	100	nA
		V_{CE} = 60 V; I_B = 0 A; T_j = 150 °C	-	-	5	µA
I_{EBO}	emitter-base cut-off current					
	NHDTC114EU	V_{EB} = 7 V; I_C = 0 A	-	-	600	µA
	NHDTC124EU		-	-	270	µA
	NHDTC144EU		-	-	130	µA
h_{FE}	DC current gain					
	NHDTC114EU	V_{CE} = 5 V; I_C = 10 mA	50	-	-	
	NHDTC124EU		70	-	-	
	NHDTC144EU		100	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA	-	-	100	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V ; I_C = 100 µA	-	1.15	0.8	V
$V_{I(on)}$	on-state input voltage					
	NHDTC114EU	V_{CE} = 0.3 V ; I_C = 10 mA	2.5	1.8	-	V
	NHDTC124EU		3	2.3	-	V
	NHDTC144EU		5	3.3	-	V
R1	bias resistor 1 (input)	[1]				
	NHDTC114EU		7	10	13	kΩ
	NHDTC124EU		15.4	22	28.6	kΩ
	NHDTC144EU		33	47	61	kΩ
R2/R1	bias resistor ratio	[1]	0.8	1	1.2	
f_T	transition frequency	V_{CE} = 5 V; I_C = 10 mA; f = 100 MHz [2]	-	170	-	MHz
C_c	collector capacitance	V_{CB} = 10 V; I_E = i_e = 0 A; f = 1 MHz	-	-	2.5	pF

[1] See section "Test information" for resistor calculation and test conditions
[2] Characteristics of built-in transistor

Table 10 starts with the break down voltages $V_{(BR)CBO}$ and $V_{(BR)CEO}$, means break down voltages of the collector-base path with an open emitter respectively collector-emitter path with an open base.

Maximum leakage currents I_{CBO}, I_{CEO} and I_{BEO} are informed next. These are the cut-off currents for the collector-base, collector emitter and base-emitter path. The emitter-base cut-off current values appear quite high compared to a stand-alone BJT. The reason for this is that the integrated base resistors are located across this path. If an R2 resistor is present, the leakage current is proportional to the sum of R1 and R2 at the specified conditions.

The h_{FE} parameters for RETs are defined as I_C/I_{IN}. I_{IN} is divided into the base current and the current which flows through R2 which is $I_{R2} = V_{BE}/R2$. Due to this fact h_{FE} is smaller compared to a RET with a series base resistor R1 only. And of course h_{FE} is getting smaller the lower the resistance of R2 is, because input current is drained away. This fact can be seen in Table 8 clearly.

V_{CEsat} is the residual collector-emitter voltage in on-state of the RET switch. The test condition is to apply 0.5 mA base drive and 10 mA collector current.

V_I considerations

$V_{I(off)}$ informs at which input voltage the RET turns off. The test condition for off-state is to have a collector leakage current of 100 µA at a collector-emitter voltage of 5 V. The lower value provided in the table as $V_{(Ioff)}$max has to be considered as maximum allowed output level of the stage which drives the RET. This condition has to be fulfilled for safe off-state of the RET.

For the other direction, the on-state, there is the important parameter $V_{I(on)}$min to be considered. The circuit controlling the RET has to provide this voltage for a safe turn on at least. As on-state condition a collector current of 10 mA is defined while the collector-emitter voltage is 0.3 V. The data sheet V_I rating is valid for the test condition defined only. If a bigger collector current shall be switched the RET requires more base drive voltage $V_{I(on)}$.

In Fig. 12 the switching characteristic of a RET is shown with a graph of V_{CE} versus V_I.

$V_I < V_{I(off)}$max: a RET is in off-state for every device shipped.

$V_I < V_{I(off)}$typ: a typical RET is in off-state.

$V_I > V_{I(on)}$typ: a typical RET is in on-state.

$V_I > V_{I(on)}$min: a RET is in on-state for every device shipped.

Fig. 12. RET Input voltage V_I versus V_{CE}characteristics

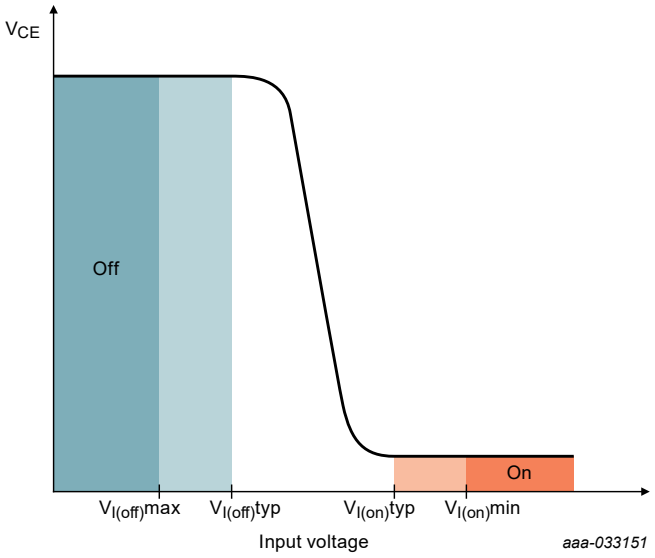


Table 11 shows the dependency of the on- and off-state input voltages on the resistor divider configuration in RETs from the NHDTC series.

For the $V_{I(off)}$ condition a very small base current flows into the BJT (about 0.3 µA) . So the typical value to turn off a RET is coupled almost directly to the resistor ratio R1/R2. It can be calculated with a voltage drop target across R2 or the base-emitter diode where the transistor is turned off. This voltage is about 580 mV for the NHDTC series discussed. Therefore $V_{I(off)}$ values for a resistor ratio equal 1 show the same voltages (rows 1-3 in Table 11).

The typical off-state voltages for R2 equal 47 kΩ and different R1 (2.2 kΩ, 4.7 kΩ and 10 kΩ) are lower in accordance with the above described background. For $V_{I(off)}$max an even value has been defined which safeguards operation in the very left area of Fig.10.

Table 11. $V_{I(on)}$ and $V_{I(off)}$ dependency on resistor configuration R1/R2

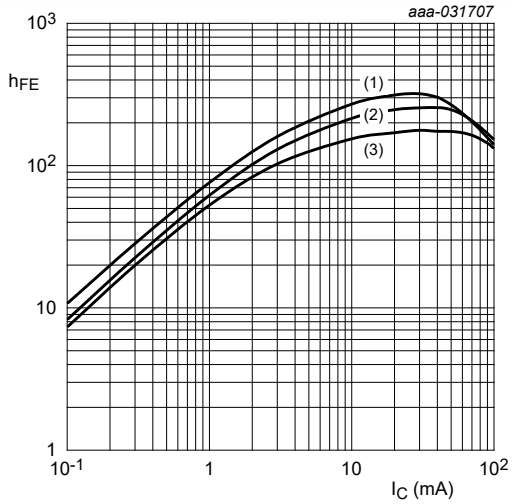
R1 / R2 (kΩ)	$V_{I(on)}$ min (V)	$V_{I(on)}$ typ (V)	$V_{I(on)}$ max (V)	$V_{I(off)}$ max (V)	RET Type
10 / 10	2.5	1.8	1.15	0.8	NHDTC114ET
22 / 22	3	2.3	1.15	0.8	NHDTC124ET
47 / 47	5	3.3	1.15	0.8	NHDTC144ET
2.2 / 47	1.2	0.81	595	0.5	NHDTC123JT
4.7 / 47	1.4	0.95	625	0.5	NHDTC114YT
10 / 47	1.6	1.22	690	0.5	NHDTC143ZT

The selection of a proper resistor divider option is important so that the control voltage window of the RET fits well to the driving stage. The desired collector or load current has an impact on the base current to be provided for the on-state. For a higher collector current a lower value for R1 and/or less bypass current through R2 is the direction to go.

For an application, temperature drift of the VI parameters needs some attention. V_{BE} of BJTs decreases over temperature with a coefficient of about -1.7 mV/K to -2.1 mV/K dependent on chosen silicon diffusion details.

Current amplification $h_{FE} = I_C/I_B$ increases with about 1% per Kelvin for a stand-alone BJT.

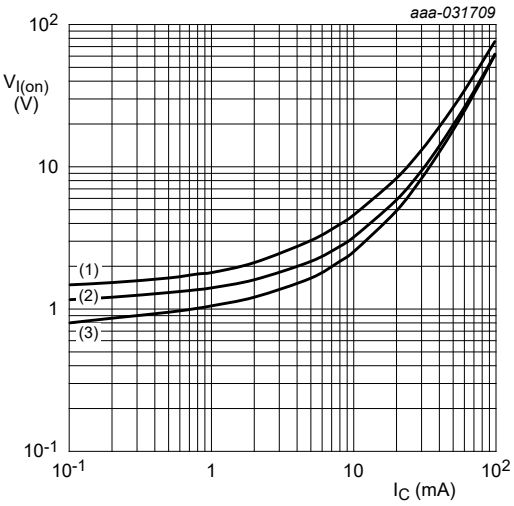
In Fig. 13 the typical DC current gain as a function of collector current is shown for the ambient temperatures 100 °C, 25 °C and -40 °C. Also for a RET with integrated poly-silicon resistor base divider, h_{FE} shows higher values the warmer T_{amb} becomes.



V_{CE} = 5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 13. NHDTC144EU: DC current gain as a function of collector current; typical values

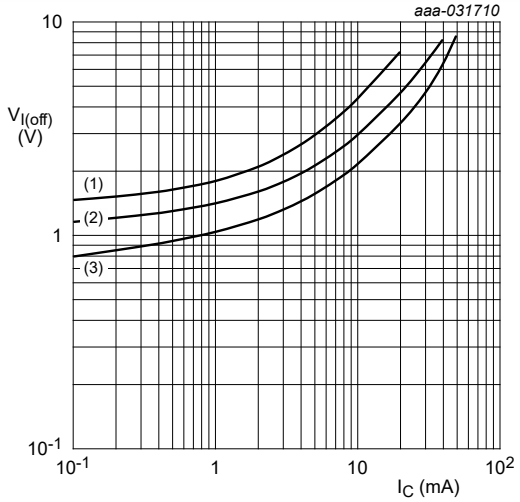
In Fig. 14 of the data sheet, the typical On-state input voltage $V_{I(on)}$ is shown as a function of I_C. As to be expected a higher input voltage is required to drive more collector current at same V_{CE}. A low ambient temperature requires higher input voltage because V_{BE} increases and h_{FE} drops. So turning on a RET switch at low temperature is the most critical operating condition for an application and the user has to apply enough input voltage in order to turn on the device properly.



V_{CE} = 0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 14. NHDTC144EU: On-state input voltage as a function of collector current; typical values

Fig. 15 of the data sheet shows which $V_{I(off)}$ has to be applied typically to guarantee a safe turn off of a RET switch. For this switching direction the input voltage has to be low enough for safe operation. For the off-state high temperature condition is the most critical scenario. In this case the driver circuit has to be designed in a way that it outputs a voltage well below typical VI(off) for the highest temperature in the application.



V_{CE} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 15. NHDTC144EU: On-state input voltage as a function of collector current; typical values

5. RET resistor specifics

RET Resistor specifics

R1, the series resistor towards the base of the BJT has a tolerance of typically +/- 30 %.

R2 is not defined directly but via a ratio R2/R1. This has a tolerance of ± 20% for 100 mA RETs and ± 10% for 500 mA RETs as depicted in Table 12 below.

Table 12. Tolerances of integrated resistors in RETs

Resistor specification	Typical tolerances	RET types
R1	± 30%	all
R2/R1	± 20%	100 mA RETs
	± 10%	500 mA RETs

This means for the range of R1:

$R1_{min} = 0.7 * R1_{typ}$

$R1_{max} = 1.3 * R1_{typ}$

For calculating the minimum and maximum values of R2, the tolerance for the resistor ratio has to be considered. For 100 mA RETs it can be calculate with ± 20% tolerance according Tab.9:

$R2_{min} = 0.7 * R1_{typ} * 0.8 * R2_{typ}/R1_{typ} = 0.56 * R2_{typ}$

$R2_{max} = 1.3 * R1_{typ} * 1.2 * R2_{typ}/R1_{typ} = 1.56 * R2_{typ}$

The temperature dependency of the integrated polysilicon resistors can be described with the quadratic equation below. T0 is 25°C for the values provided in Tab. 10.

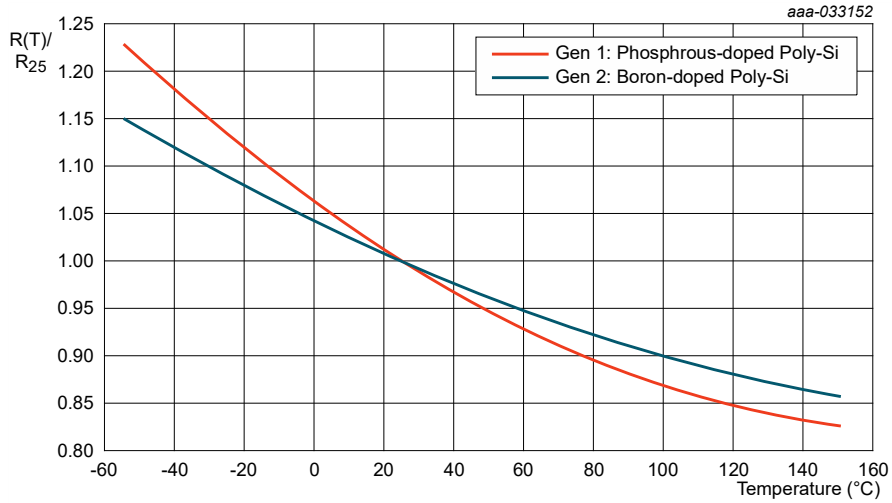
$R(T) = R(T_0) * (1 + \alpha * (T - T_0) + \beta * (T - T_0)^2)$

Table 13 informs the coefficients α and β for Phosphorus-doped Poly-Silicon which is used for generation 1 RETs in Nexperia and Boron-doped Poly-Silicon used for generation 2 wafers. Fig. 16 shows the normalized resistance over temperature for these two process options. The resistance of the integrated resistors decreases over temperature. The Boron-doped Poly-Silicon resistor show a smaller temperature dependance compared to the Phosphorus doping.

Table 13. Coefficients for thermal dependency of Poly-Silicon resistor values in RETs

	α	β
Phosphorus-doped Poly-Si	-0.00229	7.26 * 10E-6
Boron-doped Poly-Si	-0.00161	3.7275 * 10E-6

Fig. 16. Normalized resistance over temperature for Nexperia RETs



As parameters related to the dynamical performance of RETs, #unique_6/unique_6_Connect_42_table_y2n_hgc_q4b informs the transition frequency f_T and the collector capacitance C_c. f_T is the frequency where the current amplification of the BJT becomes equal 1 for the test condition defined.

6. Testing of RET resistors

The integrated resistors of RETs cannot be tested directly, because there is no access to the node of the base of the BJT. The resistors need to be tested between the contacts 1 and 2 as assigned in Fig. 17. The collector contact is left floating.

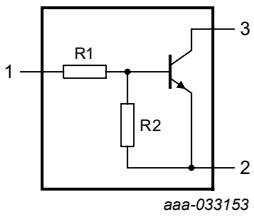


Fig. 17. RET with base resistor divider R1 and R2

For this test set up, an equivalent circuit can be depicted as shown in Fig. 18. The BJT is replaced by a diode D_{BE} representing the base-emitter path. The integrated resistors of the RET are present with R1 and R2. The related voltages V_{BE} representing the input voltage of the RET and the voltage drop V1 at R1 respectively V2 at R2 are depicted.

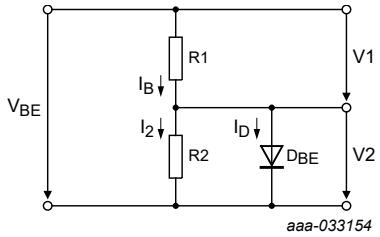


Fig. 18. Equivalent circuit for testing of resistor divider values

Fig. 19 simplifies the circuit further if the polarity of VBE is taken into account. In case the voltage applied has a positive polarity R2 is much bigger than R_{BE}, so R2 canbe neglected. In reverse direction the base-emitter diode does not conduct, so the resistors themselves dominate the test circuit.

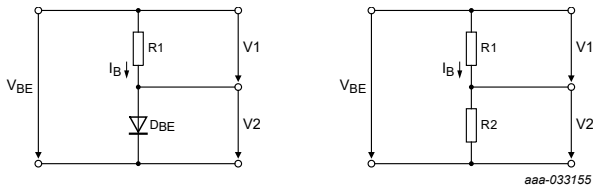


Fig. 19. Simplified test circuit dependent on VBE polarity

Fig. 20 shows an I-V-curve of the base-emitter path, so V_{BE} versus the input current I_B, for an NPN-RET with an R1 of 2.2 kΩ and R2 of 47 kΩ. The diagram is separated into 4 regions.

Region IV corresponds to reverse direction V_{BE}, where in addition breakdown voltage of the base-emitter diode is exceeded. The steepness or dynamic resistance $\Delta V/\Delta I$ in this part of the curve is R1, because the emitter-base diode clamps to the breakdown voltage.

Region III is the reverse blocking voltage range equivalent to the right part of Fig. 18. The steepness is equivalent to R1 + R2. This value is tested in mass production under this condition. Nexperia uses a two point testing method for a more exact measurement result, so R1 + R2 = $\Delta V_{BE}/\Delta I_B$.

In Region II the V_{BE} path is biased in forward direction but the base-emitter diode is not conducting significantly yet. The steepness of the curve is proportional to R1 + R2 like for Region III.

In Region I the diode conducts as depicted on the right side of Fig. 18. The curve ramps up with R1 as steepness. To measure the steepness two operating points have to be chosen in order to calculate $\Delta V_{BE}/\Delta I_B$. R1 is measured following this test method in mass production. In Region I single operating point measurement would not be sufficient because Vf of the base-emitter diode creates an voltage offset of the curve that needs to be eliminated for resistor calculation. Fig. 21 shows an example where the two test points provide a good result for R1, with R1 = (V2 -V1) / (IB2 -IB1) as they are in the linear region of the curve.

With the value for R1 + R2 derived from Region III, R2 can be calculated easily and the ratio R2/R1 as well.

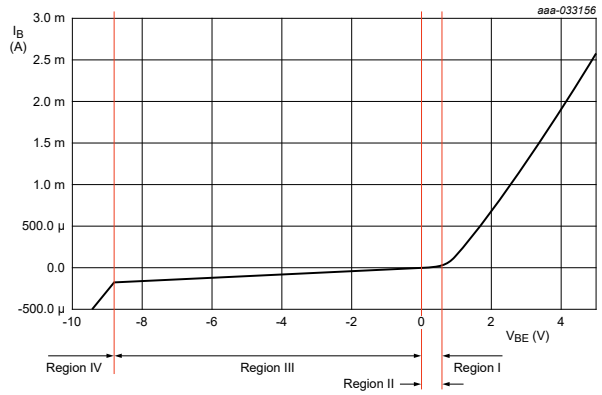


Fig. 20. Typical VBE versus IB curve for a RET with R1 = 2.2 kΩ and R2 = 47 kΩ

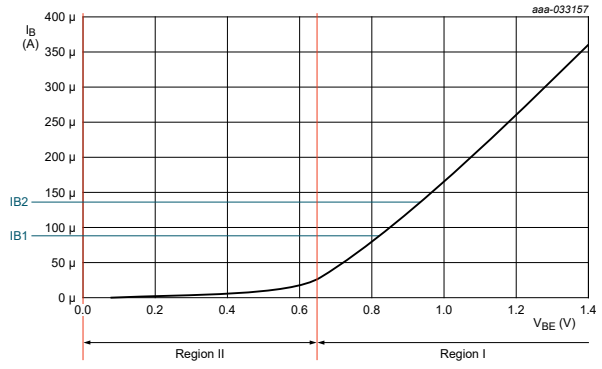


Fig. 21. Example for two test points on the I-V curve in Region I for calculation of the integrated resistor R1

7. RETs exposed to ESD events

Bipolar transistors have a rather good ESD robustness compared to small size MOSFET transistors. For MOSFETs the gate is the most vulnerable pin because gate oxide can get damaged quite easily without a recovery from an exposure to surge events above the breakthrough voltage. This is why most small-signal MOSFETs have an integrated gate-source ESD protection nowadays. The ESD robustness level which is targeted for electronic components has the goal to secure safe handling in mounting and board production. A standard level of robustness is a 2 kV HBM (human body model) rating for ICs and discrete electronic components.

Discrete BJTs meet the target of a 2 kV HBM robustness without problems normally because pn-junctions facing a breakdown are not damaged if current and energy applied is comparably low.

In contrast RETs require some attention for ESD events because the integrated poly-silicon resistors tend to be sensitive to surge pulses. This fact is not specific for any semiconductor manufacturer in the market but requires general attention.

ESD damages can be seen at the resistor R1 most often. R2 is protected via the base-emitter diode of the BJT which does either conduct in forward direction or clamps an incoming surge event to a non-destructive level in reverse direction. Fig. 22 shows typical ESD related crystal damages in the base resistor R1.

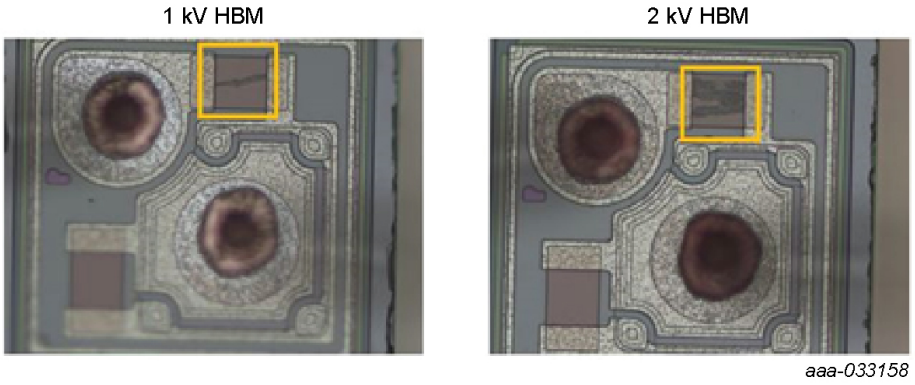


Fig. 22. Example for two test points on the I-V curve in Region I for calculation of the integrated resistor R1

In modern ESD-safe manufacturing environment RETs can be mounted safely. If the base is attached to an interface for external connections, an additional external ESD protection might be considered.

8. Package overview for Nexperia RETs

Nexperia offers RETs in various package options. Table 14 shows the package types available clustered into leaded and leadless types. The size of the package body is informed as well as the power rating for a standard footprint on a single layer FR4 PCB.

The table shows that leadless packages provide a very good thermal performance while saving board space. A DFN1006 RET performs as well as a much bigger SOT23 device. With a DFN1412-6 RET up to 480 mW can be dissipated with a package area of 1.4 mm x 1.2 mm = 1.68 mm² compared to 400 mW for a SOT457 and a much bigger package area of 4.35 mm². The DFN1412 is 40% of the size of a SOT457 for the package body. In a design the occupied area is even more important to be compared. For DFN1412 the occupied area is 1.6 mm x 1.71 mm = 2.736 mm². For SOT457 the area 5.3 mm x 5.05 mm = 26.765 mm² needs to be provided on a board. So space saving is enormous for the DFN package as the factor is close to 10. The reason is that the leads itself and the landing pads of a leaded package require significant extra space compared to a leadless device where the landing pads are almost under the package with small areas outside the package body.

The thermal path from the crystal down into the PCB is short and direct. This is why $R_{th(j\text{-}sp)}$ is very small for DFN devices. Leadless packages allow a more compact design combined with a high power density. This helps designers to have a suitable solution for the industry trend towards further miniaturization.

Table 14. Package options for RETs

Package cluster	Package name	RET type	Size (mm)	P_{tot} (mW) [1]
leaded	SOT23	single	2.9 x 1.3 x 1	250
	SOT323	single	2 x 1.25 x 0.95	235
	SOT457	dual	2.9 x 1.5 x 1	400 (250)
	SOT363	dual	2 x 1.25 x 095	350 (235)
	SOT666	dual	1.6 x 1.2 x 0.55	300 (200)
leadless	DFN1006-3 (SOT883)	single	1 x 0.6 x 0.48	250
	DFN1006B-3 (SOT883B)	single	1 x 0.6 x 0.37	250
	DFN1010D-3 (SOT1215)	single	1.1 x 1 x 0.37	325
	DFN1010B-6 (SOT1216)	dual	1.1 x 1 x 0.37	350 (230)
	DFN1412-6 (SOT1268-1)	dual	1.4 x 1.2 x 0.47	480 (325)

[1] **For dual types the first value is maximum power per device and the value in brackets is valid per transistor.**

9. Revision history

Table 15. Revision history

Revision number	Date	Description
1.0	20210303	AN90024 initial version

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