Abstract

This application note explains the content of Nexperia Power GaN FET data sheets. Nomenclature, pinning and key parameters are detailed.
1. Introduction

This application note examines in detail the data sheet for the GAN063-650WSA GaN FET device from Nexperia. Visit the product information page on Nexperia.com to download the latest version of the full data sheet.

2. Nomenclature

The device name (type number) is shown at the top of the data sheet. The name contains some important information about the device. In the below example for GAN063-650WSA, the maximum on-state resistance and the limiting drain-source voltage are specified, together with letter codes indicating the package, the mounting base electrical connection and the technology generation.

![GaN FET Nomenclature](image)

Fig. 1. GaN FET Nomenclature

3. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>G</td>
<td>gate</td>
<td>mb</td>
<td><img src="image" alt="Diagram" /></td>
</tr>
<tr>
<td>2</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>D</td>
<td>drain</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mb</td>
<td>S</td>
<td>mounting base; connected to source</td>
<td><img src="image" alt="Diagram" /></td>
<td></td>
</tr>
</tbody>
</table>

The Nexperia GAN063-650WSA is packaged in a TO247 (SOT429) package with a source tab. The traditional TO-247 provides excellent heat transfer, and therefore excellent power-handling capability.
Understanding Power GaN FET data sheet parameters

Note: the pin functions are different from a standard MOSFET: pin 1 is the gate, pin 2 is the source and pin 3 is the drain.

Using pin 2 as the source pin allows the circuit designer to keep the gate loop and the power loop separate. This facilitates a very clean design and greatly reduces or eliminates cross coupling. The PCB design can be optimised to take advantage of this feature.

4. Two-chip, integrated, normally-off power switch

The full graphic symbol of a GaN FET is shown in the pinning information section of the data sheet. Note that the symbol includes two devices:

- Low-voltage Si MOSFET with a p-n body diode
- High-voltage GaN FET without a p-n body diode

The full graphic symbol shows that the device is a two chip integrated switch. Functionally the switch is normally off. Internally the device is built with two chips. The high-voltage GaN HEMT or FET is normally on, which is the type most naturally made with GaN, and is combined with a high performance normally-off Si MOSFET specifically developed to complement the GaN HEMT. The two chips are integrated with absolute minimum inductance between them.

In circuit schematics where just the basic switching function is important, a simple N-channel FET symbol is used to represent the complete, integrated switch (see Q1 circled in red above). When you see the simple symbol, understand that it represents this two-chip integrated combination.
5. GaN FET limiting values

The limiting values table provides the range of operating conditions allowed for the GaN FET. The conditions are defined in accordance with the **Absolute Maximum Rating System (IEC 60134)**.

Operation outside of these conditions is not guaranteed, so it is recommended that these values are never exceeded. Doing so risks immediate device failure or reduced lifetime of the GaN FET. To calculate how the limiting values change with temperature de-rating curves are provided.

The limiting values table for the GAN063-650WSA is given as an example of a standard limiting values table, in Table 2.

Table 2. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DS}</td>
<td>drain-source voltage</td>
<td>(-55 ,^\circ\mathrm{C} \leq T_{j} \leq 175 ,^\circ\mathrm{C})</td>
<td>-</td>
<td>650</td>
<td>V</td>
</tr>
<tr>
<td>V_{TDS}</td>
<td>transient drain to source voltage</td>
<td>pulsed; (t_p = 1 ,\mu\mathrm{s}; \delta_{\text{factor}} = 0.01)</td>
<td>-</td>
<td>800</td>
<td>V</td>
</tr>
<tr>
<td>V_{GS}</td>
<td>gate-source voltage</td>
<td></td>
<td>-20</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>P_{tot}</td>
<td>total power dissipation</td>
<td>(T_{mb} = 25 ,^\circ\mathrm{C}; \text{Fig. 9})</td>
<td>-</td>
<td>143</td>
<td>W</td>
</tr>
<tr>
<td>I_D</td>
<td>drain current</td>
<td>(V_{GS} = 10 ,\mathrm{V}; T_{mb} = 25 ,^\circ\mathrm{C})</td>
<td>-</td>
<td>34.5</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(V_{GS} = 10 ,\mathrm{V}; T_{mb} = 100 ,^\circ\mathrm{C})</td>
<td>-</td>
<td>24.4</td>
<td>A</td>
</tr>
<tr>
<td>I_{DM}</td>
<td>peak drain current</td>
<td>pulsed; (t_p \leq 10 ,\mu\mathrm{s}; T_{mb} = 25 ,^\circ\mathrm{C})</td>
<td>-</td>
<td>150</td>
<td>A</td>
</tr>
<tr>
<td>T_{stg}</td>
<td>storage temperature</td>
<td></td>
<td>-55</td>
<td>150</td>
<td>^\circ\mathrm{C}</td>
</tr>
<tr>
<td>T_J</td>
<td>junction temperature</td>
<td></td>
<td>-55</td>
<td>175</td>
<td>^\circ\mathrm{C}</td>
</tr>
<tr>
<td>T_{sd(M)}</td>
<td>peak soldering temperature</td>
<td></td>
<td>-</td>
<td>260</td>
<td>^\circ\mathrm{C}</td>
</tr>
</tbody>
</table>

**Source-drain diode**

| I_S  | source current          | \(T_{mb} = 25 \,^\circ\mathrm{C}; V_{GS} = 0 \,\mathrm{V}\) | -    | 34.5 | A    |
| I_{SM}| peak source current     | pulsed; \(t_p \leq 10 \,\mu\mathrm{s}; T_{mb} = 25 \,^\circ\mathrm{C}\) | -    | 150  | A    |
5.1. Drain-source voltage, $V_{DS}$

This 650 V rating is the maximum value that will give you the desired product life.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$-55 \degree C \leq T_J \leq 175 \degree C$</td>
<td>-</td>
<td>650</td>
<td>V</td>
</tr>
<tr>
<td>$V_{RDS}$</td>
<td>transient drain to source voltage</td>
<td>pulsed; $t_p = 1 \mu s; \delta_{factor} = 0.01$</td>
<td>-</td>
<td>800</td>
<td>V</td>
</tr>
</tbody>
</table>

As can be seen in Fig. 5 above, GaN FETs do not have an avalanche breakdown mechanism. The Nexperia GaN FET does not typically show any significant leakage current until a $V_{DS}$ greater than 1500 V is reached. So, there is an extra margin in $V_{DS}$ before excess leakage occurs. If the GaN FET is subjected to a voltage greater than 1500 V, then because there is no clamping mechanism damage and or failure will occur. Since GaN FETs do not have an avalanche breakdown mechanism they are very immune to cosmic radiation and so no further de-rating is required.

- $V_{DS}$ is the maximum voltage the device is guaranteed to block between drain and source terminals in the off-state.
- $V_{DS}$ is a DC rating
- $V_{DS}$ not limited by avalanche breakdown; rating can be applied over entire operating range of -55 $\degree$C to 175 $\degree$C in contrast to $V_{DS}$ for Si MOSFET must be de-rated below 25 $\degree$C
5.2. Transient drain-source voltage, $V_{TDS}$

$V_{TDS}$ is the **Maximum** repetitive transient voltage the device is guaranteed to block between drain and source in the off state. This transient rating, applies over the entire operating temperature range.

### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$-55 , ^\circ C \leq T_J \leq 175 , ^\circ C$</td>
<td>-</td>
<td>650</td>
<td>V</td>
</tr>
<tr>
<td>$V_{TDS}$</td>
<td>transient drain to source voltage</td>
<td>pulsed; $t_p = 1 , \mu s$; $\delta_{factor} = 0.01$</td>
<td>-</td>
<td>800</td>
<td>V</td>
</tr>
</tbody>
</table>

**Fig. 6. Duty Cycle Definition**

**Fig. 7. $V_{TDS}$ test circuit**

**Fig. 8. $V_{TDS}$ waveform**
5.3. Gate source voltage, $V_{GS}$ and total power dissipation, $P_{\text{tot}}$

### Table 4. Limiting values

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{DS}}$</td>
<td>drain-source voltage</td>
<td>$-55 , ^\circ\text{C} \leq T_j \leq 175 , ^\circ\text{C}$</td>
<td>-</td>
<td>650</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{TDS}}$</td>
<td>transient drain to source voltage</td>
<td>pulsed; $t_p = 1 , \mu\text{s}; \delta_{\text{factor}} = 0.01$</td>
<td>-</td>
<td>800</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{GS}}$</td>
<td>gate-source voltage</td>
<td></td>
<td>-20</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>$P_{\text{tot}}$</td>
<td>total power dissipation</td>
<td>$T_{\text{mb}} = 25 , ^\circ\text{C}$</td>
<td>-</td>
<td>143</td>
<td>W</td>
</tr>
</tbody>
</table>

$V_{GS}$

Maximum voltage the device is guaranteed to block between the gate and source terminals. This is a **DC rating**, and applies over the entire operating temperature range.

$P_{\text{tot}}$

$P_{\text{tot}}$ is the Total Power dissipation is the maximum for a device with a mounting base temperature of 25 °C.

![Graph of $P_{\text{der}}$ vs $T_{\text{mb}}$](image)

$$P_{\text{der}} = \frac{P_{\text{tot}}}{P_{\text{tot}(25 \, ^\circ\text{C})}} \times 100 \%$$

**Fig. 9. Normalised total power dissipation as a function of mounting base temperature**

Power dissipation is calculated as that which would take the device to the maximum allowed junction temperature while keeping the mounting base at 25 °C.
5.4. Continuous and pulsed currents, $I_D$, $I_{DM}$, $I_S$ and $I_{SM}$.

The 25 °C current ratings are the same for both current directions ($I_D$ and $I_S$).

The maximum current at any $T_{mb}$ is the current which increases $T_j$ to the maximum allowed temperature (175 °C).
6. GaN FET static characteristics

These are the device parameters that explain how the GaN FET behaves in its normal operating conditions.

6.1. Gate-source threshold voltage, $V_{\text{GS(th)}}$

<table>
<thead>
<tr>
<th>Table 6. Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
</tr>
<tr>
<td>---------------</td>
</tr>
<tr>
<td>$V_{\text{GS(th)}}$</td>
</tr>
<tr>
<td>$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \degree C$</td>
</tr>
<tr>
<td>$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \degree C$</td>
</tr>
<tr>
<td>$I_{\text{DSS}}$</td>
</tr>
<tr>
<td>$V_{DS} = 650 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \degree C$</td>
</tr>
<tr>
<td>$I_{\text{GSS}}$</td>
</tr>
<tr>
<td>$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \degree C$</td>
</tr>
</tbody>
</table>

Gate-source threshold voltage for the GaN FET device is the gate-source threshold voltage of the Si MOSFET. This gate threshold is 3.9 V typically, with a negative temperature coefficient.

![GaN FET gate-source threshold voltage](aaa-029304)

$V_{\text{GS(th)}} = 3.9 \text{ V}$

Fig. 10. GaN FET gate-source threshold voltage
6.2. Drain-source on-state resistance, $R_{DSon}$

| $R_{DSon}$ | drain-source on-state resistance | $V_{GS} = 10\, V; I_D = 25\, A; T_j = 25\, ^\circ C$ | - | 50 | 60 | m$\Omega$
| $V_{GS} = 10\, V; I_D = 25\, A; T_j = 175\, ^\circ C$ | - | 120 | - | m$\Omega$

$R_{DSon}$ is the drain-to-source on-state resistance of the GaN FET. This has a dynamic value for GaN FETs. When $R_{DSon}$ is measured immediately after turn-on, following period of blocking high-voltage, this value will be slightly higher than normal. This is due to temporary charge trapping in the device structure. Nexperia have optimised the device so that charge trapping and dynamic $R_{DSon}$ are minimised.

As can be seen in Fig. 13, $R_{DSon}$ is shown as a normalised function of junction temperature.

$$a = \frac{R_{DSon}}{R_{DSon(25\, ^\circ C)}}$$

Fig. 11. Test circuit for dynamic $R_{DSon}$

Fig. 12. Dynamic $R_{DSon}$ waveform

Fig. 13. Normalised drain-source on-state resistance as a function of junction temperature.
7. GaN FET dynamic characteristics

These are the device parameters that explain how the GaN FET behaves in its normal operating conditions.

7.1. Gate charge $Q_{\text{G(tot)}}$, $Q_{\text{GS}}$ and $Q_{\text{GD}}$

<table>
<thead>
<tr>
<th>Dynamic characteristics</th>
<th>$Q_{\text{G(tot)}}$</th>
<th>$Q_{\text{GS}}$</th>
<th>$Q_{\text{GD}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>total gate charge</td>
<td>$I_D = 25,\text{mA}$; $V_{\text{DS}} = 400,\text{V}$; $V_{\text{GS}} = 10,\text{V}$; $T_J = 25,\text{°C}$</td>
<td>-</td>
<td>15</td>
</tr>
<tr>
<td>gate-source charge</td>
<td>$T_J = 25,\text{°C}$</td>
<td>-</td>
<td>6</td>
</tr>
<tr>
<td>gate-drain charge</td>
<td></td>
<td>-</td>
<td>4</td>
</tr>
</tbody>
</table>

Gate charge for GaN FET is defined in the same way as a normal MOSFET, because the cascode arrangement of a GaN FET means that the gate is in fact the gate of a LV MOSFET. Since the LV MOSFET is a relatively small device it has a small gate charge suited to high speed switching.

7.2. Capacitances $C_{\text{iss}}$, $C_{\text{oss}}$ and $C_{\text{rss}}$

<table>
<thead>
<tr>
<th>Capacitance</th>
<th>$V_{\text{DS}} = 400,\text{V}$; $V_{\text{GS}} = 0,\text{V}$; $f = 1,\text{MHz}$; $T_J = 25,\text{°C}$</th>
<th>-</th>
<th>1000</th>
<th>pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{\text{iss}}$</td>
<td>input capacitance</td>
<td>-</td>
<td>130</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{\text{oss}}$</td>
<td>output capacitance</td>
<td>-</td>
<td>8</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{\text{rss}}$</td>
<td>reverse transfer capacitance</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Traditional small signal capacitance is shown in Fig. 14. The discontinuity (step change) in Fig. 14 is where GaN HEMT pinches off. Capacitance relates charge to voltage and energy to voltage. For a linear capacitance, the following fundamental equations apply:

$$Q = CV$$

$$E = \frac{CV^2}{2}$$

![Graph of capacitances vs. drain-source voltage](image)

Fig. 14. Input, output and reverse transfer capacitance as a function of drain-source voltage; typical values.
The capacitances $C_{o(er)}$ and $C_{o(tr)}$ attempt to capture these relationships for a nonlinear capacitance.

### 7.3. Effective output capacitance (energy related), $C_{o(er)}$

<table>
<thead>
<tr>
<th>$C_{o(er)}$</th>
<th>Effective output capacitance, energy related</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$0 \leq V_{DS} \leq 400 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>$C_{o(tr)}$</th>
<th>Effective output capacitance, time related</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$0 \leq V_{DS} \leq 400 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$</td>
</tr>
</tbody>
</table>

The GaN FET capacitance parameter $C_{o(er)}$ is the effective output capacitance (energy-related) dependent on the drain voltage.

Note that $0 \leq V_{DS} \leq 400 \text{ V}$ shown above, means as the voltage rises from 0 V to 400 V.

$$E_{OSS} = \int_0^V V_{DS} \cdot d\text{q} = \int_0^V V_{DS} \cdot C_{DS} \left( V_{DS} \right) \cdot dV_{DS}$$

![Graph showing $E_{OSS}$ as a function of $V_{DS}$]

**Fig. 15. $E_{OSS}$ as a function of $V_{DS}$**

At a specific $V_{DS}$, a unique value of $C_{OSS}$ satisfies the equation:

$$E_{OSS} = \frac{1}{2} \cdot C_{o(er)} \cdot V_{DS}^2$$

E.g.

$$E_{OSS} = \frac{1}{2} \cdot 190 \text{ pF} \cdot 400^2 = 15.2 \mu\text{J}$$

By integrating $C_{OSS}$ with respect to $V_{DS}$, the result will be $Q_{OSS}$. If we then integrate $Q_{OSS}$ with respect to $V_{DS}$, we will then arrive at $E_{OSS}$.

$E_{OSS}$ * switching frequency will give the switching power loss in Watts.
7.4. Effective output capacitance (time related), $C_{o(tr)}$

| $C_{o(er)}$ | effective output capacitance, energy related | 0 V $\leq V_{DS} \leq$ 400 V; $V_{GS} = 0$ V; $T_j = 25$ °C | - | 190 | - pF |
| $C_{o(tr)}$ | effective output capacitance, time related | 0 V $\leq V_{DS} \leq$ 400 V; $V_{GS} = 0$ V; $T_j = 25$ °C | - | 310 | - pF |

The GaN FET capacitance parameter $C_{o(tr)}$ is the equivalent capacitance to give same charging time, as $V_{DS}$ rises from 0 V to 400 V. This can also be described as a constant current being used to charge the output capacitance, giving a time related effective value.

$$Q_{oss} = \int_0^V dq = \int_0^V \left[ V_{DS} \right] C_{o(tr)} \cdot dV_{DS}$$

At a specific $V_{DS}$, a unique value of $C_{oss}$ satisfies the equation:

$$V_{ds} = \frac{Q_{oss}}{C_{o(tr)}} = \frac{1}{C_{o(tr)}} \int_0^t i(t) \cdot dt$$

e.g.

$$400V = \frac{1}{310 \text{pF}} \cdot \int_0^{120 \text{ns}} 1.0A \cdot dt$$

$$Q_{oss} = 12.4nC$$
7.5. Output charge and stored energy, $Q_{OSS}$ and $E_{OSS}$

Rather than using the $C_{o(tr)}$ and $C_{o(er)}$ parameters, it is much easier to use the graphs shown below that are also available in the data sheet. The respective $Q_{OSS}$ and $E_{OSS}$ values can be read directly for the required $V_{DS}$.

![Graph showing typical $Q_{OSS}$ and $E_{OSS}$](image1)

Fig. 16. Typical $Q_{OSS}$  
Fig. 17. Typical $C_{OSS}$ stored energy

7.6. GaN FET switching time characteristics

Nexperia GaN FETs in TO247 package have an integral Ferrite bead in the gate path. This serves to de-“Q” the gate-source loop and improve the switching stability. The Ferrite bead effectively provides damping impedance at frequencies > 100 MHz. The Ferrite bead does introduce a small propagation delay which can be seen in the values for $t_{d(on)}$ and $t_{d(off)}$, however, it does not introduce any additional loss.

![Switching time waveform](image2)

Fig. 18. Switching time waveform

![Internal Ferrite bead](image3)

Fig. 19. Internal Ferrite bead
7.7. Source-drain voltage, $V_{SD}$

<table>
<thead>
<tr>
<th>Source-drain diode</th>
<th>$V_{SD}$ (V)</th>
<th>$I_s$ (A)</th>
<th>$V_{DS}$ (V)</th>
<th>$V_{GS}$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source-drain voltage</td>
<td>$I_s = 25 A; V_{GS} = 0 V; T_j = 25 ^\circ C$</td>
<td>-</td>
<td>1.9</td>
<td>-</td>
</tr>
<tr>
<td>$t_r$</td>
<td>$1.25 V; V_{GS} = 0 V; T_j = 25 ^\circ C$</td>
<td>-</td>
<td>1.35</td>
<td>-</td>
</tr>
</tbody>
</table>

This device parameter source-drain voltage refers to the GaN FET device when it is acting as a two terminal device when not enhanced with the gate $V_{GS} = 0 V$.

![Graph of source-drain voltage vs. source-drain current](image)

**Fig. 20.** Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

**Fig. 21.** Source-drain (diode forward) voltage

$V_{SD}$ is the voltage developed whilst GaN FET conducts in reverse direction (e.g. acting as a rectifier carrying freewheeling current) Here the voltage $V_{SD}$ comprises the forward voltage of the Silicon MOSFET body diode and the voltage drop across the 2 DEG channel of the GaN HEMT.

8. $Q_r$ for GaN FET switches

| Dynamic characteristics | $Q_{SD}(\text{tot})$ | $I_s = 25 A; V_{DS} = 400 V; V_{GS} = 10 V$ | - | 15 | nC
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_{GS}$</td>
<td>gate-source charge</td>
<td>$T_j = 25 ^\circ C$</td>
<td>-</td>
<td>6</td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{GD}$</td>
<td>gate-drain charge</td>
<td>-</td>
<td>4</td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>$Q_{oss}$</td>
<td>output charge</td>
<td>$V_{GS} = 0 V; V_{DS} = 400 V$</td>
<td>-</td>
<td>125</td>
<td>nC</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Source-drain diode</th>
<th>$V_{SD}$ source-drain voltage</th>
<th>$I_s = 25 A; V_{GS} = 0 V; T_j = 25 ^\circ C$</th>
<th>-</th>
<th>1.9</th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_r$</td>
<td>$I_s = 12.5 A; V_{GS} = 0 V; T_j = 25 ^\circ C$</td>
<td>-</td>
<td>1.35</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$Q_r$</td>
<td>recovered charge</td>
<td>$I_s = 25 A; dI_s/dt = -1000 A/\mu s$; $V_{GS} = 0 V; V_{DS} = 400 V$</td>
<td>-</td>
<td>54</td>
<td>ns</td>
</tr>
<tr>
<td>-</td>
<td>recovered charge</td>
<td>$V_{GS} = 0 V; V_{DS} = 400 V$</td>
<td>-</td>
<td>125</td>
<td>nC</td>
</tr>
</tbody>
</table>
The Device Under Test (DUT) is carrying a freewheeling current. The switch in the high side of the test circuit in Fig. 22 will then turn on and force a transition at the switching node from low voltage to high voltage. This will cause the current in the DUT to change from freewheeling current to some negative current up until the point that the DUT is blocking the full DC supply voltage. If you integrate the negative current you will get the minority carrier stored charge plus any output capacitance charge.

For GaN FETs, the charge on the output capacitance $Q_{OSS}$ is the dominant component of the reverse recovery charge $Q_r$. Hence the reason that the datasheet for the Nexperia GaN FET specifies the same value for both $Q_{OSS}$ and $Q_r$.

Some GaN device manufacturers will claim to have zero reverse recovery charge $Q_r$ because they do not have a PN junction body diode. However, they will still have $Q_{OSS}$. 
9. Switching-node snubber

To achieve maximum efficiency and stability when switching high currents, a switching node RC snubber \((R, C_{sn})\) is recommended. For \(I_L < 14\) A, a switching-node snubber is not required.

![Fig. 23. Snubber capacitance as function of Load current](aaa-029603)

\[ R_G = 30\ \Omega; \tau = R_{SN} \times C_{SN} = 1\ \text{ns} \]

**Fig. 23. Snubber capacitance as function of Load current**

**Note:** a DC-link snubber is recommended in all cases. Optimal is 20 nF in series with 4 \(\Omega\), most easily achieved with parallel combination 10 nF and 8 \(\Omega\). This snubber lowers the Q factor of any resonance in the bus. That resonance will act as a load on the high gain amplifier that is the GaN FET and can lead to instability. For very high current, an RC snubber is recommended for the switching node. This will increase switching loss, so this is only recommended at high power levels where the losses are a very small percentage of the total power.

10. Revision history

<table>
<thead>
<tr>
<th>Revision number</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>2019-02-13</td>
<td>Initial version</td>
</tr>
<tr>
<td>1.0</td>
<td>2018-11-09</td>
<td>Preliminary version</td>
</tr>
</tbody>
</table>
11. Legal information

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer’s own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer’s sole responsibility to determine whether the Nexperia product is suitable and fit for the customer’s applications and products planned, as well as for the planned application and use of customer’s third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer’s applications or products, or the application or use by customer’s third party customer(s). Customer is responsible for doing all necessary testing for the customer’s applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer’s third party customer(s). Nexperia does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.
List of Tables

Table 1. Pinning information................................................ 2
Table 2. Limiting values....................................................... 4
Table 3. Revision history....................................................17
List of Figures

Fig. 1. GaN FET Nomenclature................................. 2
Fig. 2. Conventional pin assignment.............................3
Fig. 3. Nexperia pin assignment................................3
Fig. 4. Simplified GaN FET symbol..............................3
Fig. 5. Nexperia GaN FET leakage as a function of
        drain-source voltage........................................5
Fig. 6. Duty Cycle Definition.................................... 6
Fig. 7. VTDS test circuit......................................... 6
Fig. 8. VTDS waveform.......................................... 6
Fig. 9. Normalised total power dissipation as a
        function of mounting base temperature............... 7
Fig. 10. GaN FET gate-source threshold voltage........... 9
Fig. 11. Test circuit for dynamic RDSon....................10
Fig. 12. Dynamic RDSon waveform............................ 10
Fig. 13. Normalised drain-source on-state resistance
        as a function of junction temperature............... 10
Fig. 14. Input, output and reverse transfer capacitance
        as a function of drain-source voltage; typical values..11
Fig. 15. EOSS as a function of VDS............................12
Fig. 16. Typical QOSS........................................... 14
Fig. 17. Typical COSS stored energy......................... 14
Fig. 18. Switching time waveform.............................14
Fig. 19. Internal Ferrite bead................................. 14
Fig. 20. Source-drain (diode forward) current as a
        function of source-drain (diode forward) voltage;
        typical values..............................................15
Fig. 21. Source-drain (diode forward) voltage..............15
Fig. 22. Recovered charge test circuit and
        measurement waveforms..................................16
Fig. 23. Snubber capacitance as function of Load current.17
Fig. 24. DC-link snubber circuit..............................17
Contents

1. Introduction.................................................................2
2. Nomenclature.................................................................2
3. Pinning information.........................................................2
4. Two-chip, integrated, normally-off power switch........3
5. GaN FET limiting values..............................................4
   5.1. Drain-source voltage, $V_{DS}$........................................5
   5.2. Transient drain-source voltage, $V_{TDS}$.........................6
   5.3. Gate source voltage, $V_{GS}$ and total power dissipation, $P_{tot}$.........................................................7
   5.4. Continuous and pulsed currents, $I_D$, $I_{DM}$, $I_S$ and $I_{SM}$....8
6. GaN FET static characteristics....................................9
   6.1. Gate-source threshold voltage, $V_{GS(th)}$.....................9
   6.2. Drain-source on-state resistance, $R_{DSon}$...................10
7. GaN FET dynamic characteristics..............................11
   7.1. Gate charge $Q_{G(tot)}$, $Q_{GS}$ and $Q_{GD}$..................11
   7.2. Capacitances $C_{iss}$, $C_{oss}$ and $C_{rss}$.....................11
   7.3. Effective output capacitance (energy related), $C_{o(er)}$....12
   7.4. Effective output capacitance (time related), $C_{o(tr)}$......13
   7.5. Output charge and stored energy, $Q_{oss}$ and $E_{oss}$......14
   7.6. GaN FET switching time characteristics..................14
   7.7. Source-drain voltage, $V_{SD}$......................................15
8. $Q_r$ for GaN FET switches.............................................15
9. Switching-node snubber................................................17
10. Revision history..........................................................17
11. Legal information........................................................18

© Nexperia B.V. 2019. All rights reserved
For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 13 February 2019