AN50013

Thermal performance of power MOSFETs in copper-clip LFPAK88 packages versus bare die

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Document information

Information	Content
Keywords	MOSFETs, thermal, power dissipation, measurements, simulations
Abstract	Automotive electrification trends are creating new higher power applications. Therefore, power switches are required to be more efficient, both electrically and thermally. At present, power modules consisting of bare die MOSFETs are used for many high power, > 3 kW, applications seeking increasing efficiency in new 48 V mild hybrid systems. The use of bare dies in modules is mainly due to the perceived improvement in thermal performance of bare die over standard packaged MOSFETs. In this application note, we show that packaged copper clip LFPAK88 MOSFETs thermally compete with bare die solutions under equivalent operating conditions for both simulation and measured results. This can open up the high power market for customers without the knowledge of modules.

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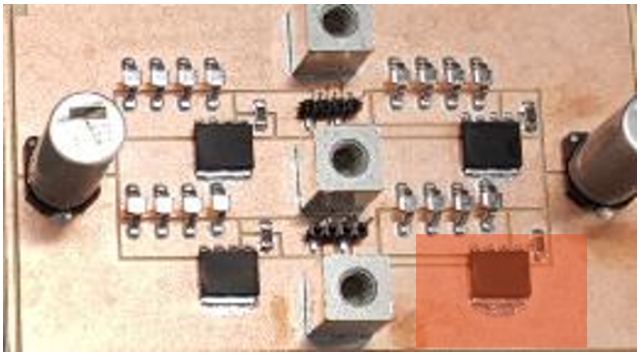
1. Introduction

The evolving technology within the automotive industry necessitates that power electronics are required to be more and more power-dense to accommodate the increasing demands of the market in terms of both safety (dual redundancy systems) and efficiency (regenerative braking etc.). Particularly in the new mild-hybrid 48 V applications the increase in power requirements along with the application size constraints can cause thermal issues which need to be overcome. Power modules and bare dies are commonly used reduce thermal issues, however a discrete component approach will be more cost effective in most cases.

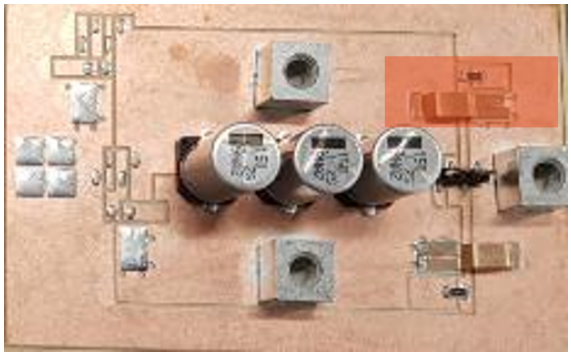
This application note investigates the differences in thermal performance between a copper-clip packaged MOSFET and a bare die MOSFET. The devices used in this comparison are an N-channel 2 mΩ LFPAK88 MOSFET and a bare die N-channel MOSFET with the same R_{DSon} and die area.

The primary method of showing the observed thermal behaviour is a Structure Function (SF) [1]. This is represented by a plot of thermal capacitance (y-axis) versus thermal resistance (x-axis), measured respectively in Ws/K and K/W. To obtain the SF a similar setup to the Transient Dual Interface Method (TDIM) [1],[2] is used to measure the thermal response of the MOSFET to an input electrical power step. The use of SF for feature/object recognition within a stack of elements is an already established method [1],[2],[3].

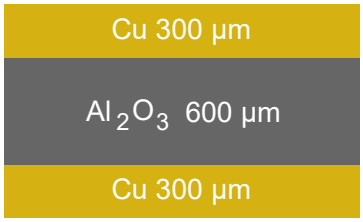
Both the LFPAK88 and the bare die MOSFETs have been mounted on similar boards made of the same substrates, Direct Bonded Copper (DBC). Fig. 1 shows the devices under test (DUT) mounted on the DBC boards as well as the DBC material stack.



LFPAK88 MOSFET



bare die MOSFET



DBC cross-section

Fig. 1. Images of copper-clip LFPAK88 MOSFET and bare die MOSFET on a DBC board (cross-section shown)

2. Thermal theory

Real systems are not 100% efficient and for this reason the input and output power are never equal [5]. Due to this, power loss occurs which translates into heat generation and temperature rise. The heat path starts at the device junction and travels through the inner structure of the device, the PCB and finally reaches the ambient.

Heat propagates due to a temperature difference through the different mediums by three methods: conduction, convection and radiation [4],[5]. In the case of the real and simulated setup discussed in this paper, no forced convection was used and for this reason the main propagation contributor is conduction, followed by natural convection from the device surface into the air and then radiation, which has the least contribution.

Thermal diffusion through solids is governed by Fourier's Law [4] which in one-dimensional form is similar to Ohm's law. Steady-state heat diffusion is given in equation (1) whereas for thermal resistance it is given in equation (2) [4],[5].

One-dimensional conduction:

$$Q = k \cdot \Delta T \cdot A/L \quad (W) \tag{1}$$

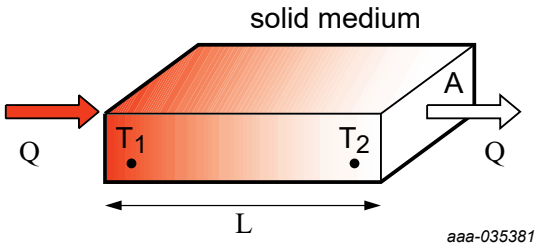


Fig. 2. Heat propagation due to conduction

Conduction thermal resistance:

$$R_{conduction} = \Delta T/Q = L/kA \quad (K/W) \tag{2}$$

where: Q is the rate of heat flow, k is the thermal conductivity of the material, ΔT the temperature difference between any two points in a material, A is the area through which the heat travels and L is the material thickness or the distance heat has to travel or propagate through.

Convection:

Convective heat transfer is dependent on the heat transfer coefficient, h, surface area A, and the surface to fluid temperature difference [3]. The relevant equations may be seen in equations (3) and (4).

$$Q = h \cdot A \cdot (T_{surface} - T_{fluid\ (amb)}) \quad (W) \tag{3}$$

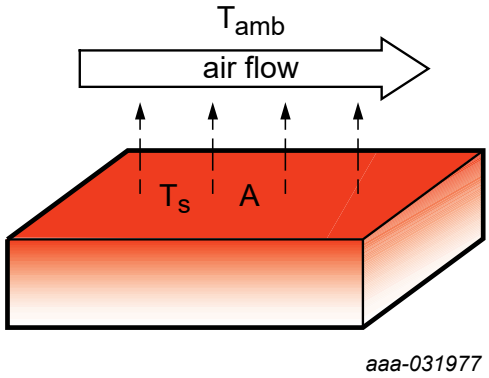


Fig. 3. Heat propagation due to convection

Convection thermal resistance:

$$R_{convection} = 1/hA \quad (K/W) \tag{4}$$

Hence the main factor that improves heat propagation in both cases, conduction and convection, is the area or surface, which is directly proportional to the heat flow rate, *Q*. Moreover thermal resistance in both cases is inversely proportional to the area or surface.

3. Device comparison

In this study the comparison was made between two types of MOSFET, the copper clip LFPAK88 in Fig. 4 a) and the copper clip bare die in Fig. 4 b). In both cases the die area was the same. This allowed observations to focus on the thermal impact of the package. In particular, the thermal impact given by the copper drain tab and the impact of the source clip.

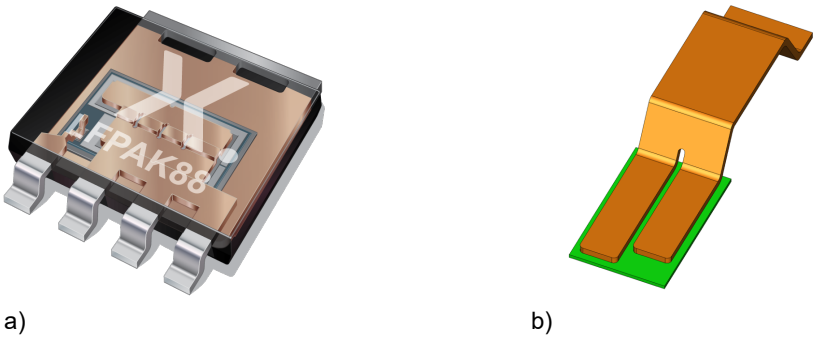


Fig. 4. LFPAK88: a) transparent 3D view, b) copper clip bare die

As may be seen in Fig. 4 b) (copper clip bare die) does not have a drain tab and thus was mounted directly on the PCB. Another difference may be spotted when comparing the source clips. The bare die has a longer and narrower source clip that is approximately 15 mm by 4 mm when compared to the LFPAK88. Also, the die thickness of the bare die is significantly larger than that of the LFPAK88 die. Moreover, the LFPAK88 also features the moulded case whereas the bare die is open. Since the thermal resistance of the case plastic is considerably higher than the junction to mounting base thermal resistance this parallel heat path was not considered.

As it can be seen in Fig. 5, there are 2 parallel heat paths from the junction to the mounting base. This means that heat will mostly flow in the one with the least resistance, through the 3 different methods: conduction, convection and radiation. Conduction effects were the main ones considered in this study as it mainly investigates the heat propagation through the different materials of the MOSFETs, solder and then the PCB, Fig. 6.

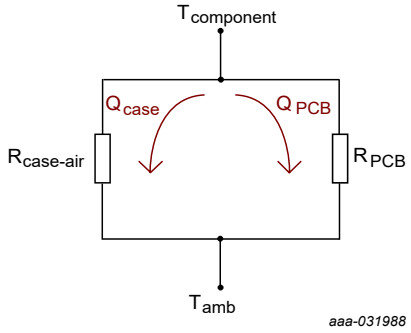


Fig. 5. Heat parallel path from component to ambient

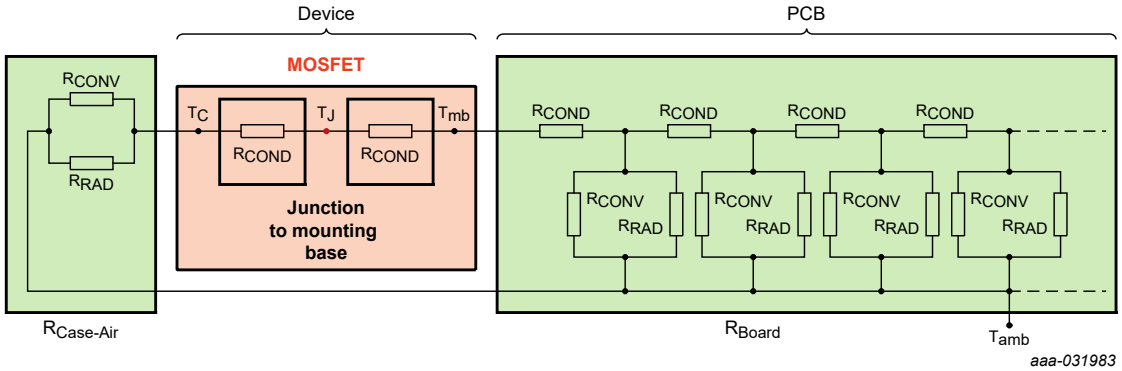
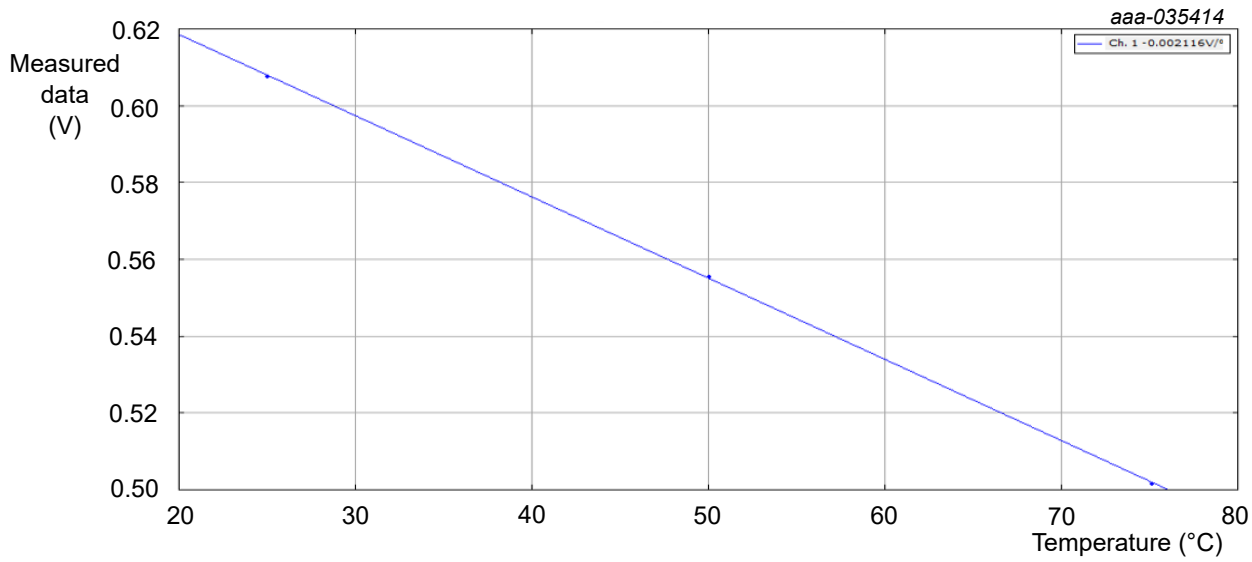


Fig. 6. Thermal circuit of a device on a PCB

Convection was not considered, because there was no forced air cooling and due to the higher thermal resistance from the devices to the air. As mentioned, radiation is also a contributor but its effects are negligible within the operating temperatures of the device.

In both cases the thermal calibration of the devices yielded a similar sensitivity factor. This was found to be approximately 2 mV/K as it may be seen in Fig. 7.



Calibration of temperature coefficient of the body diode bias point

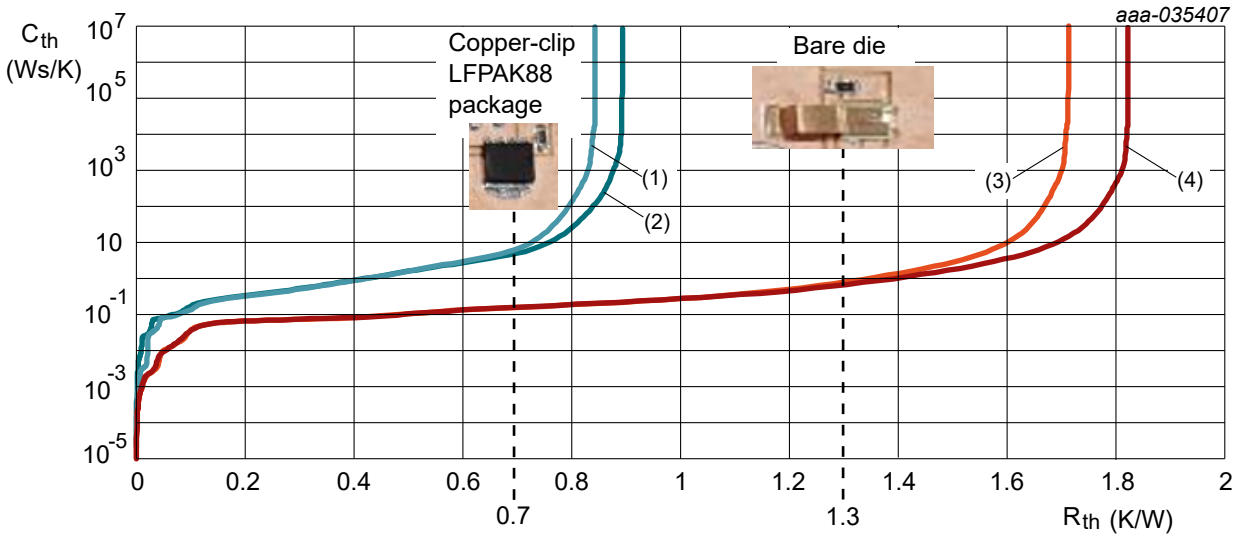
Fig. 7. LFPAK88 and Bare Die – calibration plot and sensitivity factor

The above comparison was offered in order to clearly define the study objective as well as provide some context for the measurement results and simulation results available in the next chapters.

4. Measurement procedure and results

In power electronics the standard for describing, measuring and calibrating power electronics devices from a thermal perspective is given by the JEDEC standards [1],[2]. This paper is based on the Transient Dual Interface Method (TDIM), described in reference [2] and uses this procedure to determine the thermal behaviour of the two MOSFET types. Using a *T3ster* measurement system in conjunction with a glycol cooled heatsink and an adjustable mounting rig, the two boards were pressed onto the heatsink and the SF recorded.

Following the procedures described in references [1],[2], two SF were recorded for each case: one directly mounted onto the heatsink and the other with a carbon pad in between the board and the heatsink. The results are shown in Fig. 8. Under these conditions the LFPAK88 showed a significantly smaller $R_{th(junction\text{-}DBC)}$ than the bare die indicating the better thermal performance of LFPAK88.



(1) LFPAK88 with a carbon pad in between the board and the heatsink
(2) LFPAK88 directly mounted onto the heatsink
(3) Bare die with a carbon pad in between the board and the heatsink
(4) Bare die directly mounted onto the heatsink

Fig. 8. Copper-clip package vs. bare die Structure Functions obtained using the *T3ster* measurement system

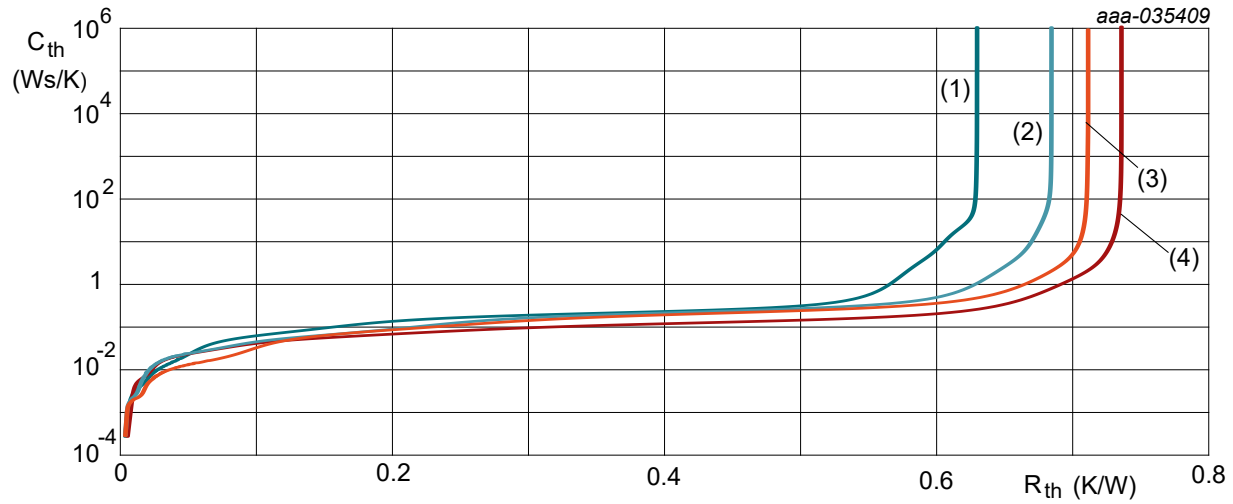
Another observation relates to the thermal capacitance measured in the two cases. For a given thermal resistance, the measurement results of the bare die show a smaller thermal capacitance when compared to the copper-clip packaged device. This is due to the thermal capacity of the LFPAK88 mounting base and source clip. This indicates that the LFPAK88 may better handle power transients such as overcurrent fault conditions and these events will cause a lower temperature rise than would be seen in bare dies.

5. Simulation setup and results

This section is aimed at understanding the behaviour depicted by the measurement results and the reasons behind it. This was facilitated by simulations of a similar set-up used for the measurement procedure.

5.1. Simulation results

The experimental setup was reproduced in the *scSTREAM* simulation environment. By applying a power step to both the copper-clip LFPAK88 packaged device and the bare die MOSFET, their SFs were recorded and plotted in Fig. 9. The LFPAK88 behaved better than the bare die MOSFET - curve (1) vs. curve (4), in agreement with the experimental data. In addition, two further simulations were conducted. The first, placed the bare die device on the copper drain tab of the LFPAK88 device - curve (3). The second, placed the bare die device on the copper drain tab of the LFPAK88 device and also shortened the source clip of the bare die - curve (2). As shown in Fig. 9, the ambient R_{th} improves for the three different simulations of the bare die. The thermal capacitance also increases when adding the copper drain and shortening the bare die source clip.



(1) LFPAK88
(2) Bare die on LFPAK88 drain copper and short source clip
(3) Bare die on LFPAK88 drain copper
(4) Bare die

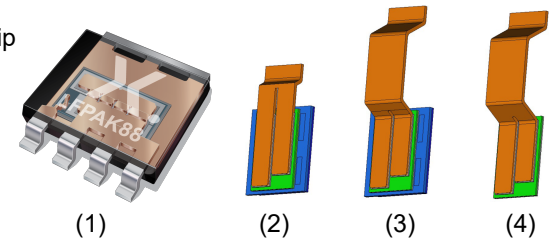


Fig. 9. LFPAK88 and bare die Structure Functions, obtained using the *scSTREAM* simulation environment

6. Results, discussion and reasoning

The measurement results obtained using the *T3ster* apparatus and rig showed that the thermal resistance from junction to ambient and from junction to the PCB bottom are lower in the case of the copper-clip packaged MOSFET when compared to the bare die clip packaged MOSFET, see Fig. 1 and Fig. 4. The same behaviour was shown in Fig. 9 using a very similar setup within the *scSTREAM* simulation environment. On the other hand, the simulation results showed smaller discrepancies between the two packages. The differences between the real and simulated results may have occurred for the following reasons: model fidelity, solder layer voiding in real life vs simulation ideal solder model, heatsink considered ideal, overall domain sizes not as large as the *T3ster* rig and the meshing of the simulation.

Considering that thermal resistance is inversely proportional to the area or surface through which heat passes through (conduction), the results show that the drain tab of the LFPAK88 acts as an extension of the die inside the package and also as the active thermal area thus conducting more heat. Similarly, the short copper-clip of the source pins also add the benefit of extracting the heat through the top of the device and sinking it into the DBC. These effects are seen in Fig. 9, where the bare die behaved better when placed on the copper drain tab of the LFPAK88 and even better when the source clip was shortened.

7. Conclusion and recommendation

The results from the copper clip LFPAK88 versus the bare die MOSFET have been compared, and show that a discrete package can be a viable alternative to bare die and modules, even in higher power applications.

The drain of the packaged device showed that the increased contact area with the PCB is a benefit when it comes to heat transfer and the reduction of the R_{th}. Also, the thickness of the drain tab also provides thermal capacitance which may act as a thermal buffer in switching applications. Another benefit observed in the structure of the packaged device is the source clip which helped with sinking the heat coming from the top of the die. The simulations results showed that by having a shorter and thicker clip also improved the thermal performance and overall R_{th}.

This offers a possible alternative discrete strategy approach, and also will allow engineers who have no power module expertise to still compete in higher power applications, particularly in the high growth Electric Vehicle markets.

8. References

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9. Revision history

Table 1. Revision history

Revision number	Date	Description
1.0	2022-09-21	Initial version.

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