# Abstract

This application note provides a general guideline of Single-Ended Primary Inductance Converter (SEPIC) DC-to-DC converter design using Nexperia Power MOSFET devices.
1. Introduction

In modern automotive applications, electrical systems are widely used in vehicles. They usually powered by lead-acid or Li-ion batteries whose output voltage varies with the State of Charge (SOC), temperature, load dump and other loading operations. This requires DC-to-DC converters to accommodate a wide input voltage and generate a stable regulated output voltage for electrical loads. A Single-Ended Primary Inductance Converter (SEPIC) design can be a good fit for a battery powered system. It can generate output voltage higher or lower than the input voltage with less components comparing to other topologies. Additionally, its AC coupled capacitor inherently separates the output from the input. LED lighting is one example where SEPIC converters can be used in an automotive application.

Fig. 1. Automotive application - LED lighting

In this application note, a general guideline of SEPIC converter design using Nexperia Power MOSFET devices will be described.
2. SEPIC converter design example

A Synchronous SEPIC DC-to-DC converter design example is shown in Fig. 2. One of the features of SEPIC converters is that the currents flowing through the two inductors are proportional to each other \[1\]. Hence, a coupled inductor can be used in the design for reducing PCB footprint size and system cost.

Design specifications:
- Input voltage: 9 ~ 16 V
- Output voltage: 20 V
- Maximum output power: 20 W
- Switching frequency: 380 kHz

Key features:
- Reverse battery protection (RBP)
- Synchronous topology improves converter efficiency
- Configurable light load operation modes:
  - Burst mode improves efficiency but causes higher output ripple and switching noise
  - Forced continuous mode for lower output ripple and switching noise but higher switching loss
  - Pulse-skipping mode comprises of the above two operation modes

Fig. 2. SEPIC converter PCB for LED lighting
3. System design

SEPIC topology is a combined topology consisting of two building blocks as shown in Fig. 3 below.

At the input side, there is a common Boost configuration formed by an inductor and a power switch. This eases the RMS current seen by input capacitor [1].

At the output side, a Buck block is formed by a synchronous MOSFET or diode and an inductor. As these two inductors are being charged and discharged during the whole operation period, a coupled inductor can be used to reduce size and cost.

With this configuration, a SEPIC converter is able to accommodate a wide input voltage range and provide a regulated output.

Fig. 3. SEPIC converter building block

To ensure proper energy transfer and operation of a SEPIC converter, a coupling capacitor with low ESR is required. The RMS current rating of this capacitor is proportional to output power, since all output current is passing through coupling capacitor. And maximum input voltage plus some ripple will determine the voltage rating. This capacitor is also the inter-connection between two building blocks. Please refer to AC coupling capacitor section for more details.
The basic operation of a SEPIC converter is shown in Fig. 4 (a) below. During the period that switch Q1 = ON the coupled inductor (two windings) and coupling capacitor are being charged and energy is stored inside them. Current flow is indicated in Fig. 4 (b). In this period, all output power is provided by output capacitor to maintain regulated output voltage rating. When Q1 = OFF, and synchronous MOSFET Q2 = ON, Fig. 4 (c), energy is released from inductors and delivered to the load.

**Fig. 4.** SEPIC converter phases
3.1. Power MOSFET

Power MOSFET selection plays a critical part for the whole design as it determines the whole system’s thermal design requirements, cost and efficiency. Theoretical analysis can be performed with mathematical equations.

In the SEPIC topology, the voltage stress on the main and synchronous MOSFET is the sum of maximum input voltage and regulated output voltage:

\[ V_{DS(max)} = V_i(max) + V_o \]  \hspace{1cm} (1)

During the main switch on state, both inductor currents will pass through the main control MOSFET \[ I_{L1}(peak) \]. Therefore, the peak and RMS current can be calculated:

\[ I_{M1}(peak) = I_{L1}(peak) + I_{L2}(peak) \]  \hspace{1cm} (2)

\[ I_{M1(RMS)} = \sqrt{(I_{M1(peak)}^2 - I_{M1(peak)} \times (\Delta I_{L1} + \Delta I_{L2}) + \frac{3(\Delta I_{L1} + \Delta I_{L2})^2}{4})} \times D_{max} \]  \hspace{1cm} (3)

During the main switch off state, both inductor current will through the synchronous MOSFET, consequently the peak and RMS current are expressed as:

\[ I_{M2(peak)} = I_{L1}(peak) + I_{L2}(peak) \]  \hspace{1cm} (4)

\[ I_{M2(RMS)} = \sqrt{(I_{M2(peak)}^2 - I_{M2(peak)} \times (\Delta I_{L1} + \Delta I_{L2}) + \frac{3(\Delta I_{L1} + \Delta I_{L2})^2}{4})} \times (1 - D_{max}) \]  \hspace{1cm} (5)

With current and voltage rating known, we can calculate the switching and conduction losses for the main MOSFET:

\[ P_{M1CON} = I_{M1(RMS)}^2 \times R_{ds(on)} \]  \hspace{1cm} (6)

\[ P_{M1SW} = V_i(peak) \times I_{M1(peak)} \times \frac{C_{iss} \times V_g}{I_g} \times 2 \times f_{sw} \]  \hspace{1cm} (7)

Where \( \Delta V_g \) is gate voltage sweeping range, and \( C_{iss} \) is the MOSFET input parasitic capacitance, \( I_g \) is the gate drive sinking and sourcing current.

And for synchronous MOSFET the switching and conduction losses can be obtained by:

\[ P_{M2CON} = I_{M2(RMS)}^2 \times R_{ds(on)} \]  \hspace{1cm} (8)

\[ P_{M2SW} = V_o(peak) \times I_{M2(peak)} \times \frac{C_{iss} \times \Delta V_g}{I_g} \times 2 \times f_{sw} \]  \hspace{1cm} (9)
During converter design, theoretical analysis utilizes complicated mathematical equations. Some of these can be only approximations. For instance, the entire switching process of a MOSFET is non-linear. There is always some discrepancy between theoretical calculation results and the measured ones. In addition, in thermal aspect only steady state junction temperature can be estimated through mathematical equations. It is very difficult to estimate instantaneous junction temperature through theoretical equations since the current profile could be very complex. Several iterations of calculation are usually needed to choose the right MOSFET that meets the system efficiency, cost and size requirement. For initial performance estimation, calculation can be verified by computer simulation. Please refer to Nexperia interactive application note IAN50002 for an example SEPIC converter simulation. In the embedded simulation, any voltage or current waveform can be viewed using the probes available from the toolbar. For thermal estimation using RC models, please refer to Nexperia application note AN11261 RC Thermal Models [2].

3.2. Duty cycle calculation

The following consideration is based on SEPIC converter operating in Continuous Conduction Mode (CCM) [1].

In CCM operation, the duty cycle $D$ of a SEPIC converter can be obtained as:

$$D = \frac{V_o + V_D}{V_i + V_o + V_D} \quad (10)$$

Where $V_D$ is the voltage across the diode or the synchronous MOSFET.

3.3. Inductor Selection

There are several factors affecting the choice of inductance value like RMS current, peak-to-peak current ripple, current to ripple ratio ($r$), maximum input current (at minimum $V_{in}$), and switching frequency. One of the important factors among them is the current ripple ratio ($r$) which is defined as the ratio between inductor ripple current and average current. As a rule of thumb, the $r$ value of 0.4 would be a good starting point [1]. A higher value will bring high stress to the input capacitor (see input capacitor selection in later section.) A lower value will require higher inductor energy handling capability, which means thicker wire and larger physical size. Therefore, an inductor value can be calculated by the following equations:

$$\Delta I_L = I_i \times 0.4 = I_o \times \frac{V_o}{V_{i(min)}} \times 0.4 \quad (11)$$

$$I_1 = I_2 = \frac{V_{i(min)}}{2 \times \Delta L \times f} \quad (12)$$

In practice, inductor RMS and peak current should also be considered to ensure proper operation and design efficiency. They can be obtained by:

$$I_{L1(peak)} = I_o \times \frac{D_{max}}{1 - D_{max}} + \frac{\Delta I_1}{2} \quad (13)$$

$$I_{L2(peak)} = I_o + \frac{\Delta I_2}{2} \quad (14)$$
3.4. Bootstrap circuit design

In order to fully turn-on synchronous high side MOSFET, a floating power supply rail is required to provide at least 5 V above the MOSFET source voltage level. A bootstrap circuit formed by a capacitor, a diode and a series resistor (limiting the capacitor charging inrush current) is often used in practice. The capacitance value should be selected according to MOSFET gate charge requirement. In other words, this capacitor should provide full charge to the MOSFET gate.

\[
I_{L1_{(RMS)}} = \sqrt{\left(I_{L1(peak)}^2 - I_{L1(peak)} \times \Delta I_{L1} + \frac{\Delta I_{L1}^2}{3}\right)}
\] (15)

\[
I_{L2_{(RMS)}} = \sqrt{\left(I_{L2(peak)}^2 - I_{L2(peak)} \times \Delta I_{L2} + \frac{\Delta I_{L2}^2}{3}\right)}
\] (16)

3.5. AC coupling capacitor

One of the distinguishing advantages of a SEPIC converter is that input and output terminal is separated by the AC coupling capacitor. However, the RMS rating of this capacitor is proportional to the output power. Hence, this topology is mainly used in low and medium power application. During main control MOSFET turn-on period, \(I_{L2}\) passes through coupling capacitor [1]. In turned-off period, \(I_{L1}\) goes through coupling capacitor [1]. Therefore, the RMS current and capacitance of AC coupling capacitor can be obtained by following equations:

\[
I_{CS_{(RMS)}} = \sqrt{I_{L1}^2 \times D_{max} + I_{L2}^2 \times (1 - D_{max})}
\] (17)

\[
C_S \geq \frac{I_0 \times D_{max}}{\Delta V_{CS} \times f}
\] (18)

Where \(I_{L1}\) and \(I_{L2}\) are average current of the inductor.

In addition, when the primary control switch is on, this coupling capacitor will be charged to input voltage and some added ESR ripple. Therefore, the voltage rating should be higher than the maximum input voltage.

3.6. Input and output capacitor

The SEPIC is a combined topology which has a BOOST part at input and BUCK configuration at output. The input side has an inductor like a boost converter. Due to the existence of this inductor, the input current is triangular and continuous. Therefore, the RMS current of the input capacitor can be obtained by following equation. The voltage rating should be higher than the maximum input voltage.

\[
I_{CI_{(RMS)}} = \frac{\Delta I_L}{\sqrt{12}}
\] (19)

As the output capacitor is required to provide charge to the load during control MOSFET on state. Large ripple current would be seen by the output capacitor. Hence, RMS current should be calculated:
In practice, any parasitic parameters like ESR or ESL of a bulk capacitor will contribute to output voltage ripple. Thus, the output capacitor should be selected according to converter output ripple requirements. The relationship between output voltage ripple and ESR as well as capacitance is described by the following equations:

\[ ESR \leq \frac{V_{\text{ripple}} \times 0.5}{I_{L1(\text{peak})} + I_{L2(\text{peak})}} \]  
\[ C_o \geq \frac{I_{\text{out}} \times D_{max}}{V_{\text{ripple}} \times 0.5 \times f} \]  

3.7. Output voltage

The output voltage can be set easily through the ratio of a potential divider. The internal feedback reference voltage is 1.2 V.

\[ V_o = V_{\text{ref}} \times (1 + \frac{R_P}{R_A}) \]  

3.8. Soft start-up

A soft start-up operation is realized by using a capacitor connected to SS pin of the controller IC. In this case the controller used is the LTC3769 from Analog Devices. Other control ICs can be used. An internal current charger of 10 μA will continuously charge this capacitor until the voltage reaches the preset feedback threshold value of 1.2 V.

\[ C_{SS} = \frac{t_{SS} \times I_{\text{charge, internal}}}{V_{\text{Feedback}}} \]  

3.9. LED dimming control

The LED dimming control (shown in Fig. 5) is realized by three sub-circuits formed by Nexperia logic and transistor products. PWM generation is done by using a relaxation oscillator consists of U2, RV1, and capacitor C29. The PWM frequency can be obtained by following formula:

\[ f = \frac{1}{T} \approx \frac{1}{RC} \]  

The above equation decides the total duration of capacitor charge and discharge time. However, the charge time and discharge time can be altered by potential meter RV1. With slide more close to pin 1 of RV1, it takes less time to charge capacitor, as charge current will go through diode D17 (PMEG2005EJ) and small portion of RV1. While discharge time will be much longer, since larger...
portion of RV1 resistance appears in the capacitor discharge path. This means lower duty cycle. For increasing the duty cycle, move the slider toward pin 3 of RV1.

A logic AND gate (74AHCT1G08) is added in between output of the oscillator and MOSFET gate driver for two purposes. The first one is increasing the current driving capability and the second one is disabling the gate driver during over current fault event.

A pair of NPN and PNP transistor (in one package, BC846BPN) is used to drive the dimming control MOSFET.

Fig. 5. PWM generation, duty cycle, enable and gate driver circuit

In order to sense current, a shunt resistor is connected in series with PWM controlled MOSFET. The current through LEDs will convert to voltage signal and amplified by a factor of 33. A comparator will compare amplified voltage signal with reference value 4 V. Once the amplified voltage signal exceed threshold, signal ‘EN’ is pull down and disabling the gate driver. This state will be held until a button is pressed.

Fig. 6. Dimming MOSFET, current sense, and latch circuit
4. Schematics

Fig. 7. Overview schematic

Fig. 8. PWM, duty cycle, current sense and latch circuits
4.1. SEPIC converter schematic

When OVMODE is tied to INTVCC overvoltage protection is disabled and top MOSFET gate (TG) is not forced on during an overvoltage event

When OVMODE is tied to ground, overvoltage protection is enabled and TG is turned on continuously until the overvoltage event is cleared.

Note: NP = not plated

At light load:
- PLLIN_MODE = floating, Burst mode
- PLLINMODE = GND, Burst mode
- PLLINMODE = 1.2V_INTVcc-1.3V, Pulse-skipping mode
- PLLINMODE = INTVcc, Force current continuous mode

ILIM = INTVcc, Vsense = 100mV
ILIM = floating, Vsense = 75mV
ILIM = GND, Vsense = 50 mV

Fig. 9. SEPIC converter schematic diagram
5. Printed Circuit Board

A 4-layer PCB has been designed to demonstrate and verify the Nexperia SEPIC LED converter circuit.

![PCB Image]

Fig. 10. SEPIC DC-to-DC converter PCB

Fig. 11, Fig. 12, Fig. 13, Fig. 14 and Fig. 15 show the PCB layers.
Fig. 11. PCB front silk screen layer

Fig. 12. PCB front copper layer
Fig. 13. PCB ground copper layer

Fig. 14. PCB power copper layer
Fig. 15. PCB bottom copper layer
6. Bill of Materials

Table 1. BOM (Nexperia part)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Qty</th>
<th>Value</th>
<th>Part Number</th>
<th>Footprint</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1, D2</td>
<td>2</td>
<td>PTVS40VS1UR</td>
<td>PTVS40VS1UR</td>
<td>Diode_SMD: D_SOD123W</td>
</tr>
<tr>
<td>D3, D4</td>
<td>2</td>
<td>BZX84J-B10</td>
<td>BZX84J-B10</td>
<td>Diode_SMD: D_SOD-323F</td>
</tr>
<tr>
<td>D5</td>
<td>1</td>
<td>PMEG6010CEH</td>
<td>PMEG6010CEH</td>
<td>Diode_SMD: D_SOD-123F</td>
</tr>
<tr>
<td>D6</td>
<td>1</td>
<td>TDZ13J</td>
<td>TDZ13J</td>
<td>Diode_SMD: D_SOD-323F</td>
</tr>
<tr>
<td>D10</td>
<td>1</td>
<td>PMEG060V030EPD/NP</td>
<td>PMEG060V030EPD</td>
<td>Package_TO_SOT_SMD: SOT1289</td>
</tr>
<tr>
<td>D15, D18</td>
<td>2</td>
<td>TDZ5V1J</td>
<td>TDZ5V1J</td>
<td>Diode_SMD: D_SOD-323F</td>
</tr>
<tr>
<td>D8, D16</td>
<td>2</td>
<td>PMEG1030EJ</td>
<td>PMEG1030EJ</td>
<td>Diode_SMD: D_SOD-323F</td>
</tr>
<tr>
<td>D13, D17</td>
<td>2</td>
<td>PMEG2005EJ</td>
<td>PMEG2005EJ</td>
<td>Diode_SMD: D_SOD-323F</td>
</tr>
<tr>
<td>Q1, Q2</td>
<td>2</td>
<td>BUK6Y14-40P</td>
<td>BUK6Y14-40P</td>
<td>LFPAK56</td>
</tr>
<tr>
<td>Q3, Q9</td>
<td>2</td>
<td>BC817K-40H</td>
<td>BC817K-40H</td>
<td>Package_TO_SOT_SMD: SOT-23</td>
</tr>
<tr>
<td>Q4, Q7, Q8</td>
<td>3</td>
<td>BUK9M20-40H</td>
<td>BUK9M20-40H</td>
<td>LFPAK33</td>
</tr>
<tr>
<td>Q10</td>
<td>1</td>
<td>BC858B</td>
<td>BC858B</td>
<td>Package_TO_SOT_SMD: SOT-23</td>
</tr>
<tr>
<td>Q11</td>
<td>1</td>
<td>BC846BPN</td>
<td>BC846BPN</td>
<td>Package_TO_SOT_SMD: SOT-363_SC-70-6_ Handsoldering</td>
</tr>
<tr>
<td>U2</td>
<td>1</td>
<td>74LVC1G58GW-Q100</td>
<td>74LVC1G58GW-Q100</td>
<td>Package_TO_SOT_SMD: SOT-363_SC-70-6_ Handsoldering</td>
</tr>
<tr>
<td>U4</td>
<td>1</td>
<td>74AHCT1G08</td>
<td>74AHCT1G08GW-Q100</td>
<td>Package_TO_SOT_SMD: SOT-353_SC-70-5_ Handsoldering</td>
</tr>
</tbody>
</table>

Table 2. BOM (non-Nexperia)

<table>
<thead>
<tr>
<th>Reference</th>
<th>Qty</th>
<th>Value</th>
<th>Part Number</th>
<th>Footprint</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>1</td>
<td>LTC3769</td>
<td>LTC3769</td>
<td>TSSOP20</td>
</tr>
<tr>
<td>U3</td>
<td>1</td>
<td>AD8552ARZ</td>
<td>AD8552ARZ</td>
<td>Package_SO: SOIC-8_3.9x4.9mm_P1.27mm</td>
</tr>
<tr>
<td>C6</td>
<td>1</td>
<td>47nF</td>
<td>06033C473KAT2A</td>
<td>Capacitor_SMD: C_0603_1608Metric</td>
</tr>
<tr>
<td>C11</td>
<td>1</td>
<td>10nF</td>
<td>06033C103K4T2A</td>
<td>Capacitor_SMD: C_0603_1608Metric</td>
</tr>
<tr>
<td>RV1</td>
<td>1</td>
<td>PRS11S-N20K-503B1</td>
<td>PRS11S-N20K-503B1</td>
<td>PRS11S</td>
</tr>
<tr>
<td>L1</td>
<td>1</td>
<td>MSD1278-103ML</td>
<td>MSD1278-103ML</td>
<td>Coupled_Inductor</td>
</tr>
<tr>
<td>C9, C38</td>
<td>2</td>
<td>100pF</td>
<td>C0603C101J3GAUTO</td>
<td>Capacitor_SMD: C_0603_1608Metric</td>
</tr>
<tr>
<td>C22, C23, C24</td>
<td>3</td>
<td>10uF</td>
<td>GRT31CR61H106ME1L</td>
<td>Capacitor_SMD: C_1206_3216Metric</td>
</tr>
<tr>
<td>C7</td>
<td>1</td>
<td>15nF</td>
<td>GCJ188R71E153KA1D</td>
<td>Capacitor_SMD: C_0603_1608Metric</td>
</tr>
<tr>
<td>C29</td>
<td>1</td>
<td>2.7nF</td>
<td>GCD188R71H272KA1D</td>
<td>Capacitor_SMD: C_0603_1608Metric</td>
</tr>
<tr>
<td>C20, C21</td>
<td>2</td>
<td>150uF</td>
<td>EEE-FK1H151GV</td>
<td>CP_Elec_10.5x12</td>
</tr>
</tbody>
</table>
7. Conclusions

A battery supplied electrical system e.g. for LED lighting, requires a DC-to-DC converter to accommodate wide input voltage range. A Single-Ended Primary Inductance Converter (SEPIC) is suitable for this kind of application. In this application note, a general design approach of SEPIC DC-to-DC converter is presented. Mathematical equations should be used for initial components sizing. During this process, several iterations are required for optimal system performance. With aid of computer simulation tools and Nexperia device SPICE and RC thermal model, a more accurate initial estimation can be obtained.
8. References

2. RC Thermal Models – Nexperia

9. Revision history

<table>
<thead>
<tr>
<th>Revision number</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0</td>
<td>2021-05-10</td>
<td>Correction to Equation 6 and Equation 8.</td>
</tr>
<tr>
<td>1.0</td>
<td>2021-02-01</td>
<td>Initial version</td>
</tr>
</tbody>
</table>
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List of Tables

Table 1. BOM (Nexperia part) ............................................ 17
Table 2. BOM (non-Nexperia) ............................................ 17
Table 3. Revision history ................................................... 19
List of Figures

Fig. 1. Automotive application - LED lighting......................... 2
Fig. 2. SEPIC converter PCB for LED lighting......................... 3
Fig. 3. SEPIC converter building block.................................. 4
Fig. 4. SEPIC converter phases......................................... 5
Fig. 5. PWM generation, duty cycle, enable and gate driver circuit................................................................. 10
Fig. 6. Dimming MOSFET, current sense, and latch circuit 10
Fig. 7. Overview schematic............................................... 11
Fig. 8. PWM, duty cycle, current sense and latch circuits.... 11
Fig. 9. SEPIC converter schematic diagram......................... 12
Fig. 10. SEPIC DC-to-DC converter PCB......................... 13
Fig. 11. PCB front silk screen layer.................................. 14
Fig. 12. PCB front copper layer................................. 14
Fig. 13. PCB ground copper layer................................. 15
Fig. 14. PCB power copper layer................................. 15
Fig. 15. PCB bottom copper layer................................. 16
## Contents

1. Introduction ................................................................. 2  
2. SEPIC converter design example .............................. 3  
3. System design ............................................................. 4  
   3.1. Power MOSFET .................................................... 6  
   3.2. Duty cycle calculation ....................................... 7  
   3.3. Inductor Selection ............................................... 7  
   3.4. Bootstrap circuit design .................................... 8  
   3.5. AC coupling capacitor ...................................... 8  
   3.6. Input and output capacitor .................................. 8  
   3.7. Output voltage ................................................... 9  
   3.8. Soft start-up ...................................................... 9  
   3.9. LED dimming control ....................................... 9  
4. Schematics ................................................................. 11  
   4.1. SEPIC converter schematic ................................ 12  
5. Printed Circuit Board .............................................. 13  
6. Bill of Materials ...................................................... 17  
7. Conclusions .............................................................. 18  
8. References .............................................................. 19  
9. Revision history ..................................................... 19  
10. Legal information ................................................... 20