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APPLICATION NOTE

AN252
Live Insertion Aspects of Philips Logic Families

Author: Mike Magdaluyo

July 1999

Philips
Semiconductors

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Live Insertion Aspects of Philips Logic Families AN252

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INTRODUCTION

There is a growing demand for circuit boards in electronics systems to be inserted or extracted without switching off the power. Systems for telecom switching equipment, real-time transaction processing, air traffic controllers, and fault tolerant-computing must have minimum down time, and the capability to exchange hardware without affecting the system is important. This capability is known as live insertion, hot plugging, or hot swapping and can be implemented by careful design of hardware and software in a system.

This paper describes the events that occur during live insertion and considerations when using Philips logic products.

BUS ISOLATION

During hot swapping, the goal is to perform card insertion or extraction and maintain data integrity on the system bus, while preventing damage to components on the host system or on the inserted/extracted card. Hot swapping can be done with components that provide different levels of bus isolation. In the first level, powered-down components should be constructed such that they will not be damaged in an unpowered module while connected to a live bus. The component's input or output pins connected to the interface must not load down the system bus, and the outputs must remain high impedance and have a "power-off disable" feature. This feature is shown in data sheets as an I_{OFF} specification to support partial power-down modes. I_{OFF} circuitry eliminates current paths to V_{CC} resulting from diodes and parasitic elements.

The second level of isolation supports power-down mode and includes circuitry to keep outputs 3-State during power-up or power-down. A power-up/power-down 3-State circuit is required to prevent loading and conflicts on a live bus. This feature is found in data sheets shown as an I_{PU}/I_{PD} or I_{OZPU}/I_{OZPD} specification. System software must be able to detect the live insertion event, detect and correct any bus errors, and re-initialize the bus as needed.

The third level of isolation meets the previous two levels and includes circuitry to precharge the bus to a chosen voltage level. The precharge voltage helps reduce glitches caused by the bus impedance and capacitance at the live insertion interface. The precharge circuitry is shown in data sheets as a BIAS V pin on a device. This level of isolation supports the concept of "full" live insertion/extraction on an active bus, producing no data errors and requiring no software intervention.

A further discussion of how these Philips logic families support the different levels of isolation can be better understood by an examination of the construction of logic IC's and bus glitches discussed in the upcoming topics.

INTEGRATED CIRCUIT CONSTRUCTION

To prevent problems during live insertion it is necessary to understand the construction of integrated circuits at the insertion/extraction interface. For example, circuits with protection diodes on inputs and outputs can present a problem during insertion into a live bus. Figure 1 shows a simplified construction of an integrated circuit:

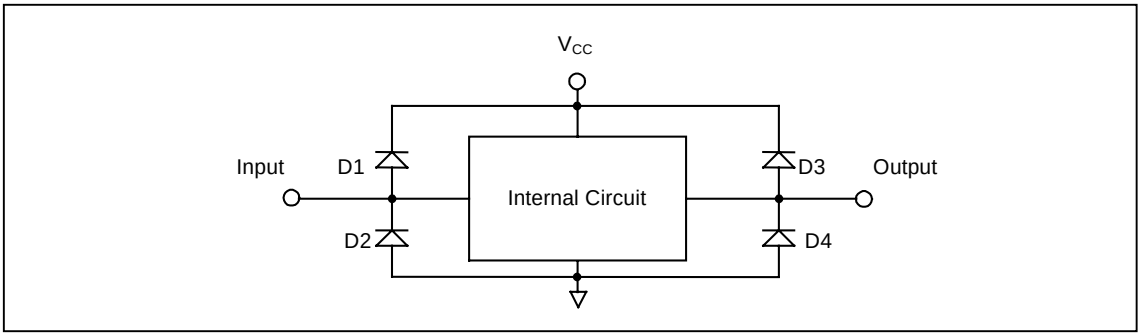

Figure 1. Diodes on inputs and outputs

D1 is used in classic CMOS circuits as an overshoot clamp. It is not present in bipolar and BiCMOS circuits. D2 is implemented in most circuits to limit undershoot or provide ESD protection. D3 is a parasitic diode found in CMOS outputs. D4 is a collector to substrate or drain to substrate parasitic diode. In bipolar devices an additional Schottky diode may be added to limit undershoot.

If the device in Figure 1 is unpowered and if either the input or output is plugged into an active bus, current will flow through D1 or D3, possibly damaging them or the active system. The bus voltage will be disrupted by being momentarily pulled down to the inactive V_{CC}. Likewise, during extraction or power-down, those diodes present a path to V_{CC} and can pull down the bus voltage to the decaying V_{CC} level. The diodes or current path must be eliminated to facilitate live insertion. Output circuits present another issue also. They must remain high impedance during power-up or power-down so that they don't drive or pull down the active bus.

Philips' newer CMOS and BiCMOS logic families have addressed these issues by modifying CMOS designs on I/O circuitry. V_{CC} clamp diodes have been removed on input circuits. Output parasitic diodes to V_{CC} are protected by power-off disable circuitry during power-down. Shown as I_{OFF} in the DC characteristics section of the data sheet, the power-off disable feature is available on the ABT, LVC, LVT, ALVT, and AVC product families. These families meet the first level of isolation required for hot swapping.

In addition to power-off isolation on inputs and outputs, Philips' BiCMOS families employ a power-up/power-down 3-State circuit to keep the outputs high impedance during power sequencing. Shown as I_{PU}/I_{PD} in the DC characteristics section of the data sheet, the power-up/power-down 3-State feature provides the second level of isolation required for hot swapping. This feature is available on the ABT, LVT, and ALVT product families. Figure 2 shows the circuit used for this:

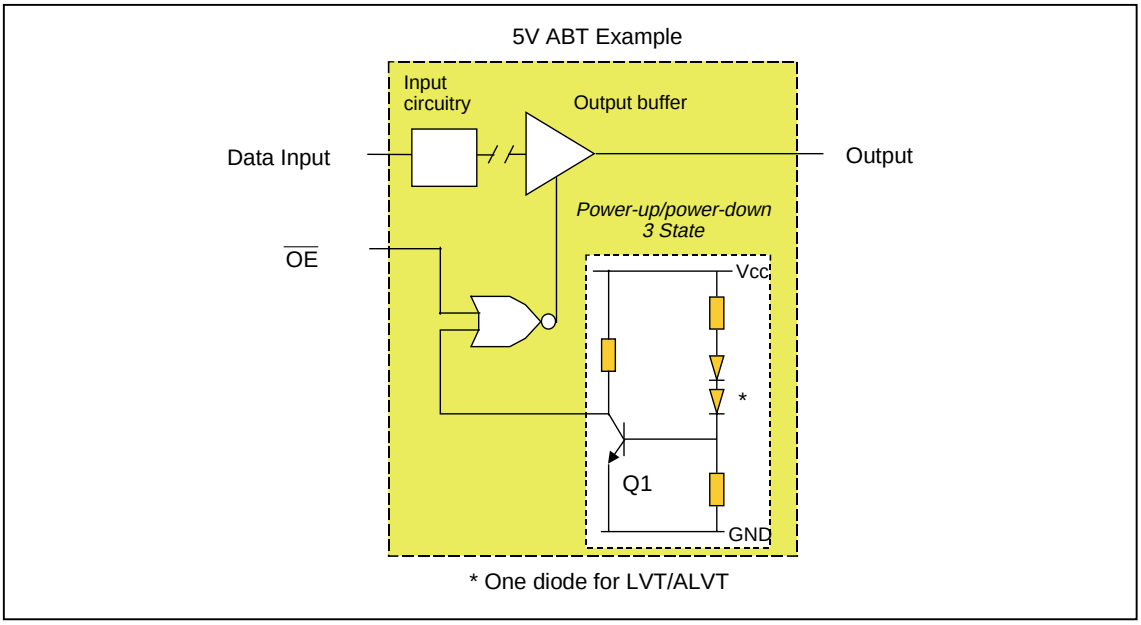

Figure 2. Power-up/power-down 3-State circuit

During power-up, the collector of Q1 follows V_{CC} which is interpreted as a logic HIGH at the input of the NOR gate. This disables the output buffer regardless of the voltage on the enable or data pins. As V_{CC} continues to rise, the Q1 base-to-emitter junction becomes forward biased. This turns on Q1 and pulls the collector of Q1 LOW and the input of the NOR gate LOW. Depending on the level of the enable pin, the output buffer can now be enabled or disabled. The V_{CC} threshold voltage to turn Q1 on or off is 2.1 V for ABT and 1.2 V for LVT and ALVT. Above those voltages, 3-State control is relinquished to the OE pin, and the end user must now control this pin to guarantee high impedance outputs.

During power-down, Q1 remains on to keep one input of the NOR gate LOW, keeping control of the output buffer to the OE pin. When V_{CC} drops below the specified thresholds discussed above, Q1 turns off, and the power-up/power-down circuit keeps the output buffer disabled.

To guarantee 3-State outputs during the full ramp up or ramp down of V_{CC}, the enable pin can be connected through an external pullup resistor to V_{CC}. For positively asserted enable pins, use a pulldown resistor to ground. These methods can also be used to implement a power-up or power-down 3-State function on LVC devices if that family is used for live insertion.

Table 1 summarizes the device characteristics of various Philips families with regards to the issues discussed in this section:

	HC/ HCT	AHC/ AHCT	ALS/ FAST	ABT	LV	LVC	ALVC	LVT/ ALVT	AVC
Inputs have no current path to V_{CC}		✓	✓	✓		✓	✓	✓	✓
Outputs have no current path to V_{CC}			✓	✓		✓		✓	✓
Lowest V_{CC} which the device will typically function[1]	1.5 V	1.5 V	3.5 V	2.1 V	1.0 V	1.2 V	1.2 V	1.2 V	1.2 V
Outputs will be 3-State below the above voltages[2]				✓				✓	

1. Devices may function at these V_{CC}'s, but speeds are degraded
2. On 3-State bus interface functions only

Table 1. Live insertion aspects of Philips' logic families

PIN CONNECTIONS

When a card is inserted into a connector, ground pins need to make the first connection. This prevents current from flowing from the powered module through unexpected return paths in the unpowered module. In Figure 3, the unpowered module shows a device output going to the connector.

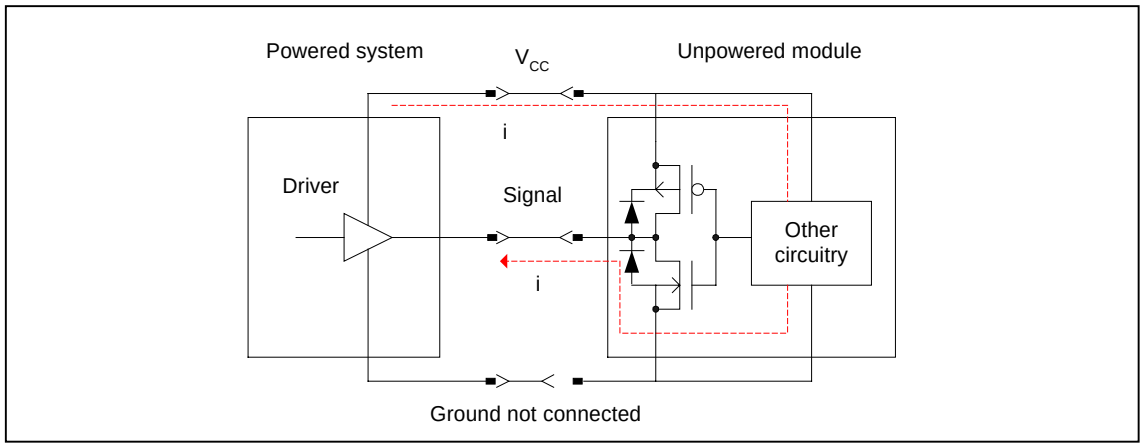

Figure 3. Current path with ground disconnected

Devices that have output clamp diodes to ground can present a return path to the powered device. Excessive current may flow through the diode, therefore, make sure that ground makes the first connection.

One way to implement a leading ground connection is to use a staggered pin arrangement on edge connectors. To have control of disabling the outputs, the output enable pin should make connection next, followed by V_{CC}, and finally the signal and other pins. An example of implementation is shown in Figure 4.

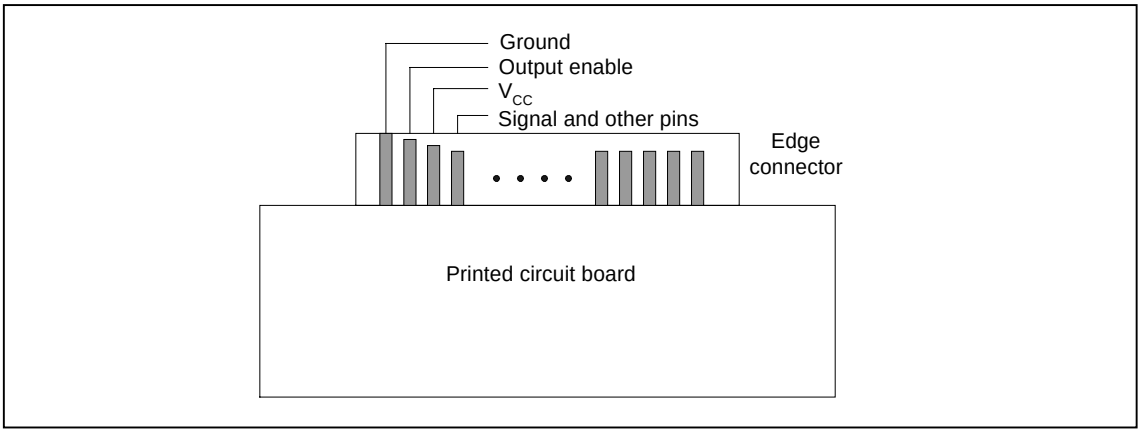

Figure 4. Staggered pin arrangement

Bus Glitches

When an unpowered module is inserted into an active backplane, a glitch is caused by the module's capacitance charging through the line impedance of the backplane's bus. This happens even though an unpowered driver's output is off and high impedance. If the amplitude and width of the glitch is sufficient, a receiver can interpret the glitch as a valid signal, and bus errors can occur. The live insertion event can be modeled using a capacitive approximation model shown in Figure 5:

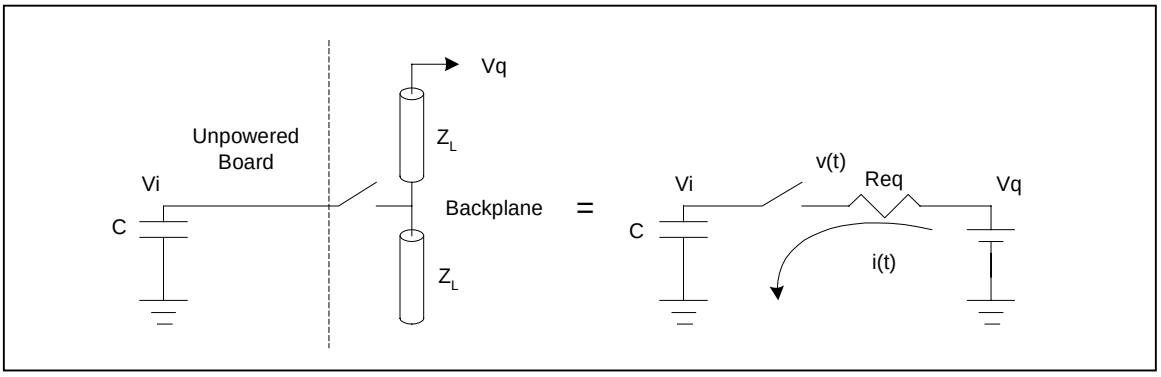

Figure 5. RC model of an unpowered module inserted into backplane

C is the capacitance of the unpowered module's driver, traces, and connector. Vi is the initial voltage of the module connector pin. Vq is the quiescent voltage on the backplane prior to live insertion. Req is the effective backplane impedance with other cards inserted. The glitch amplitude at the backplane is:

$$v(t) = Vq - (Vq - Vi)\, e^{\frac{-t}{ReqC}} \qquad \text{Eq. 1}$$

The glitch pulse width in the receiver's threshold input threshold region is

$$t = -\ln\left(\frac{Vq - Vth}{Vq - Vi}\right)ReqC \qquad \text{Eq. 2}$$

Figure 6 shows the waveform from the live insertion event:

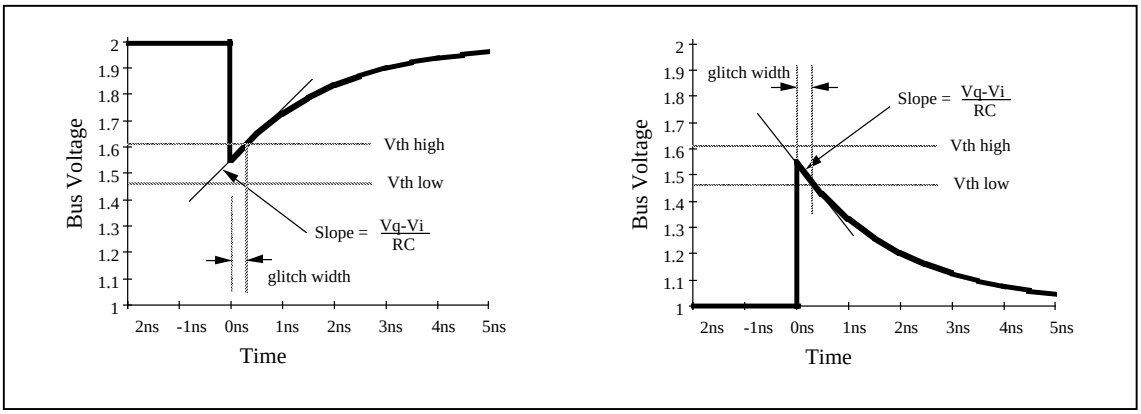

Figure 6. Capacitive approximation of glitch during board insertion

Another model for the glitch uses an RLC approximation and is represented in Figure 7. The response is shown in Figure 8.

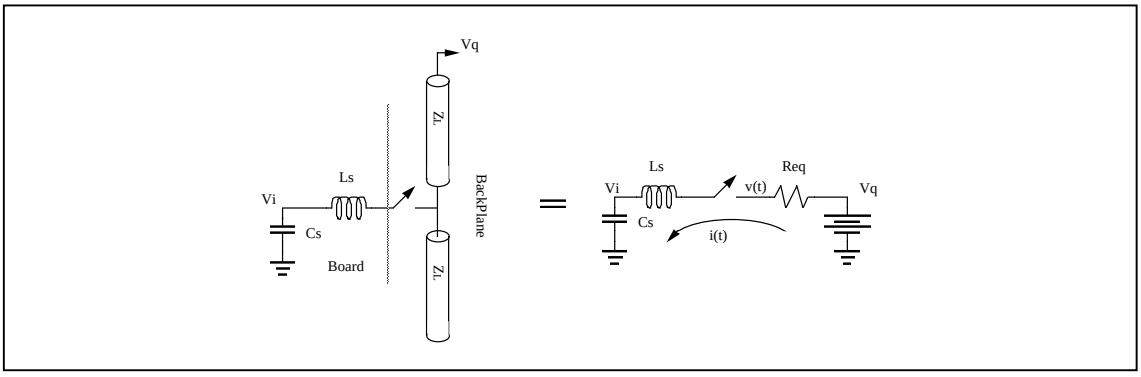

Figure 7. RLC model of live insertion event

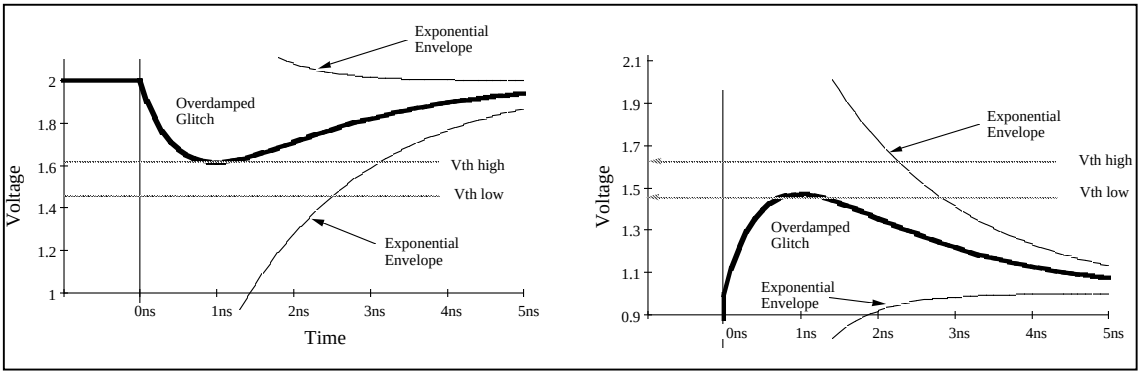

Figure 8. Glitch from RLC approximation

The size and duration of the glitch partially depends on the voltage difference between the backplane and module pin. To minimize this difference, a precharge voltage can be applied to the backplane side of the bus as the board is inserted into the active bus. Since the backplane's voltage level, Vq, can be either a HIGH or a LOW, a precharge voltage somewhere near the middle of those levels is chosen.

The glitch width is also dependent on the RC time constant of the backplane impedance and the combined capacitance of the driver, traces, and connector. By keeping the driver's output capacitance low, the glitch width can be reduced. Both of these issues are explored further in the next section on FBL.

LIVE INSERTION WITH FBL

Philips offers 3-volt BTL products that support live insertion. Used for BTL backplane drivers, these products are designated with the family name FBL, and they are constructed such that BTL outputs will minimize disturbance to the bus. FBL products translate TTL level signals to BTL levels and have two ports. One side of the device has TTL I/O's and the other side has BTL I/O's. An FBL I/O circuit is shown below:

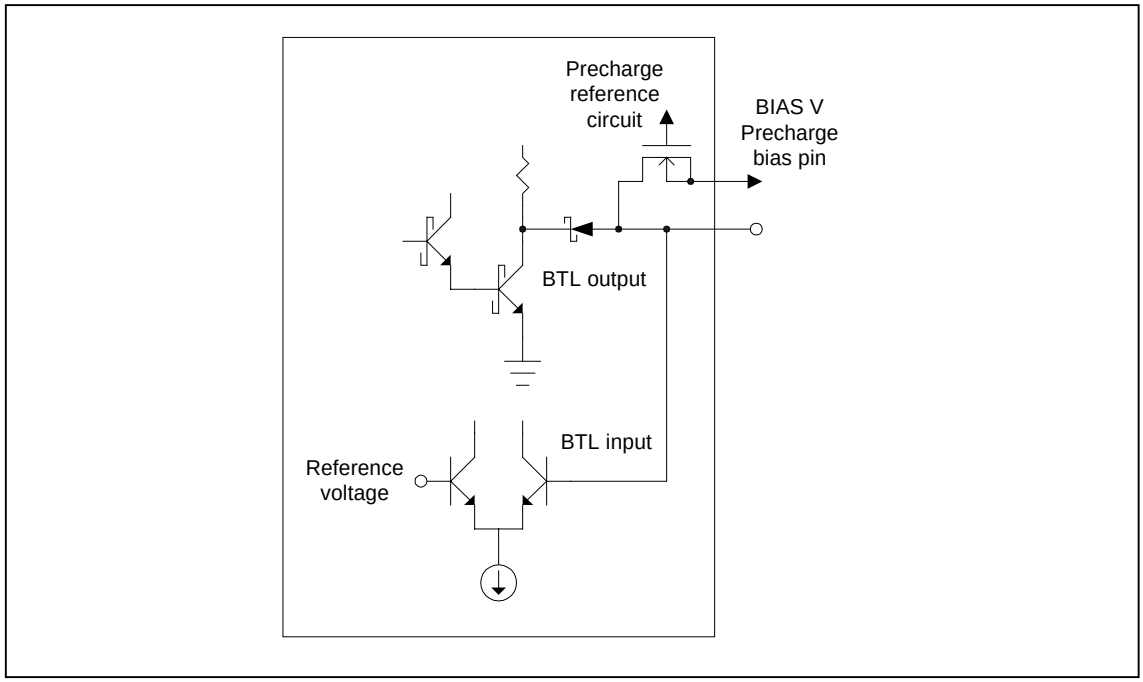

Figure 9. Simplified FBL I/O circuit

FBL devices feature low capacitance I/O's around 6 pF. This is lower than some typical I/O structures that can have values around 9-12 pF. FBL devices have a BIAS V precharge pin that needs to be connected to 3.3 V. When the device is plugged into a backplane, a precharge circuit biases the output pin to roughly 1.6 V, which is midway between the logic LOW and HIGH output levels of 1.1 V and 2.1 V respectively. This minimizes the difference between the initial voltage on the unpowered module and backplane voltage during live insertion. During power-up, when the device's V_{CC} is within 0.5 V of the BIAS V pin, the precharge circuit turns off and does not affect the output pin. To further isolate the BTL output, the BTL output enable pin, OEB0, must be de-asserted by connecting it to ground through a pulldown resistor. This ensures that the BTL output is disabled and high impedance during power sequencing. The resistor value is chosen based on the driver source current capability.

As previously discussed, the low output capacitance and the precharge voltage help minimize the amplitude and duration of glitches during live insertion. To illustrate this, SPICE simulations were used to examine the effects of having a precharge voltage versus no precharge voltage. Figure 10 shows a simulation test circuit of a module plugged into a BTL backplane.

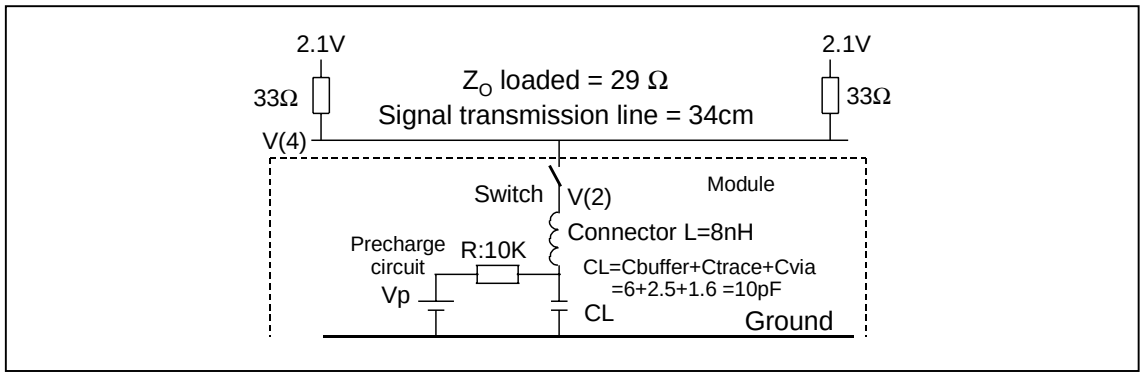

Figure 10. Simulation circuit of FBL device plugged into backplane

The simulations were done with no precharge voltage and with a 1.5 V precharge voltage applied. Capacitance and inductance from the connector, board, and driver were taken into account. In Figure 10, the BTL output is disabled and is pulled up to the termination voltage through the termination resistors. In Figure 11, note that no precharge voltage produces a glitch that dips into the switching threshold region of the receiver. Depending on the line impedance and cumulative capacitance, the glitch width and amplitude can become worse and cause a falsely recognized signal.

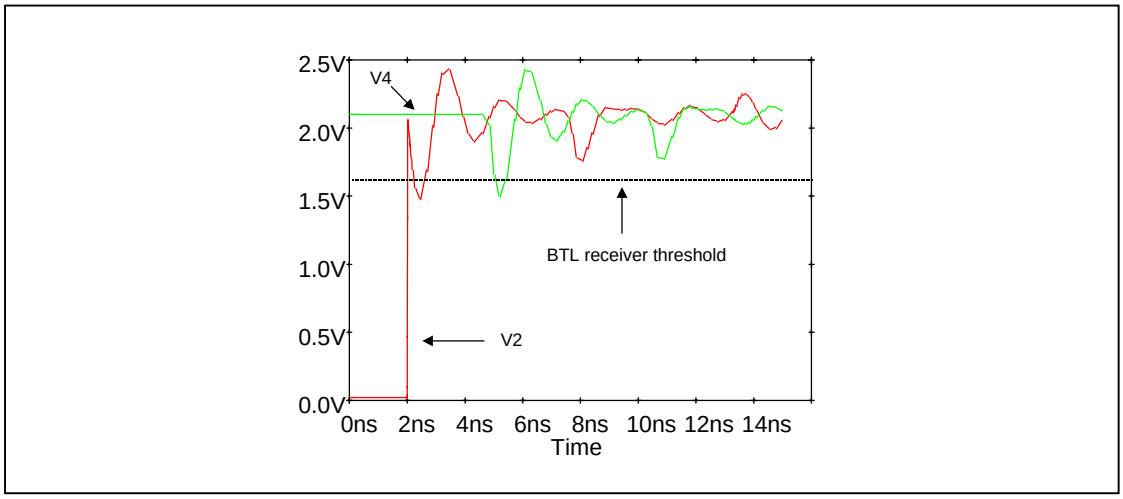

Figure 11. Glitch with no precharge

In Figure 12, you can see that a precharge voltage applied to the output pin produces a smaller glitch and it does not drop into the threshold region of the receiver.

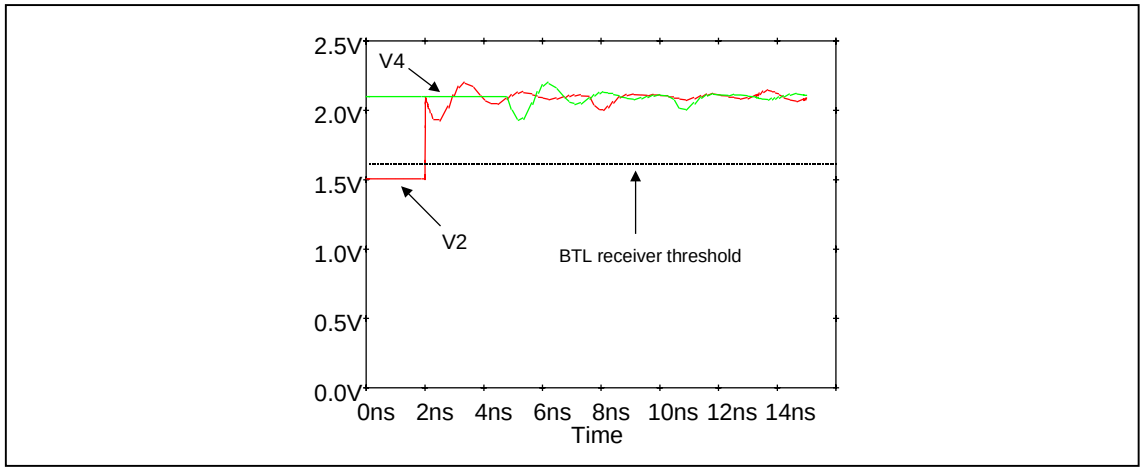

Figure 12. 1.5 V precharge applied to output

To ensure the proper sequencing of pins during live insertion, the sequence of pin connections should be as follows:

1. Ground
2. BIAS V precharge pin and enables
3. V_{CC}
4. Signal and other pins

With the combination of the BTL side output enable pin de-asserted and the use of the precharge BIAS V pin to reduce glitches, Philips FBL family support the third level of isolation required or hot swapping. Also on the receiver end, FBL inputs are designed with glitch filters to ignore glitches of 1 ns or less. This ensures minimum disturbance during hot swapping.

CONCLUSION

Hot swapping of circuit boards is a necessary feature in systems requiring board exchange in live systems to minimize down time. Hot swapping can be implemented by the proper choice of components, connector design, and system software that detects and corrects bus errors. The interfacing properties of IC's must also be understood. Different families of IC's provide different levels of bus isolation. An inactive component should provide minimal disruption to an active bus, and the I/O pins should remain high impedance to provide bus isolation. Bus glitches should be kept to a minimum to ensure data integrity. Philips provides solutions to these issues by offering logic families such as ABT, LVT, LVC, ALVT, and FBL that meet these needs.

REFERENCES

1. Jeffrey A. West, *Live Insertion.* FUTUREBUS+ DESIGN, No. 3: January/February 1992.

2. Yong-in Shin, *Live Insertion Considerations.* Technical Brief, Philips Semiconductors: 1993.

Definitions

Short-form specification – The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant datasheet or data handbook.

Limiting values definition – Limiting values given are in accordance with the Absolute Maximum Rating System (IEC134). Stess above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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