Abstract

Nexperia’s logic product data sheets describe the device function, and provide electrical and mechanical specifications including available package types and footprints. These specifications include acronyms, numerical limits, test conditions and data that can be confusing at times for the user to understand. In order to correctly use these devices in a system design and to build robust products, it is critical to fully understand and interpret their specifications and parameters. This application note explains logic device parameters such as absolute maximum, recommended operating conditions, static and dynamic characteristics, timing and noise characteristics, etc., as specified in the data sheets. With the data sheet parameters clearly explained, system designers can use the logic devices within Nexperia’s recommended specifications and ensure maximum system reliability.
1. Electrical characteristics

1.1. Currents

Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

- **I<sub>CC</sub> / I<sub>DD</sub> (supply current):** the current flowing into the V<sub>CC</sub> / V<sub>DD</sub> supply terminal.

- **ΔI<sub>CC</sub> (additional supply current):** the increase in supply current per input pin at the specified input voltage and V<sub>CC</sub>.

- **I<sub>GND</sub> (ground current):** the current flowing into the GND terminal.

- **I<sub>I</sub> (input leakage current):** the current flowing into a device at a specified input voltage and V<sub>CC</sub>.

- **I<sub>IK</sub> (input clamping current):** the current flowing into a device at a specified input voltage.

- **I<sub>O</sub> (output current):** the current flowing into a device at a specified output voltage.

- **I<sub>OFF</sub> (power-off leakage current):** the current flowing into a device at a specified voltage when V<sub>CC</sub> = 0 V.

- **I<sub>OZ</sub> (OFF-state output current):** the current flowing into a 3-state output in the OFF-state at a specified output voltage and V<sub>CC</sub>.

- **I<sub>OH</sub> (HIGH-level output current):** the current flowing into an output that is driving HIGH at a specified output voltage and V<sub>CC</sub>.

- **I<sub>OL</sub> (LOW-level output current):** the current flowing into an output that is driving LOW at a specified output voltage and V<sub>CC</sub>.

- **I<sub>BHLO</sub> (bus hold LOW overdrive current):** the current required to switch a bus hold input from a LOW to HIGH at a specified V<sub>CC</sub>.

- **I<sub>BHHO</sub> (bus hold HIGH overdrive current):** the current required to switch a bus hold input from a HIGH to LOW at a specified V<sub>CC</sub>.

- **I<sub>O(pu/pd)</sub> (power-up/power-down output current):** the current flowing into an output during power-up or power-down at a specified output voltage and V<sub>CC</sub>. 
1.2. Voltages

All voltages are referenced to GND or $V_{\text{SS}}$, the most negative potential applied to the device.

- **GND / $V_{\text{SS}}$ (supply voltage)**: for a device with a single negative power supply, the most negative power supply. Used as the reference level for other voltages; typically ground.
- **$V_{\text{CC}} / V_{\text{DD}}$ (supply voltage)**: the most positive potential on the device.
- **$V_{\text{EE}}$ (supply voltage)**: one of two (GND and $V_{\text{EE}}$) negative power supplies. For a device with dual negative power supply, the most negative power supply.
- **$V_I$ (input voltage)**: the range of voltages that can be applied to an input pin.
- **$V_O$ (output voltage)**: the range of voltages that can be applied to an output pin.
- **$V_{\text{IH}}$ (HIGH-level input voltage)**: the range of input voltages that represents a logic HIGH level in the system.
- **$V_{\text{IL}}$ (LOW-level input voltage)**: the range of input voltages that represents a logic LOW level in the system.
- **$V_{\text{OH}}$ (HIGH-level output voltage)**: the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.
- **$V_{\text{OL}}$ (LOW-level output voltage)**: the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.
- **$V_{\text{T+}}$ (positive-going threshold)**: the input voltage threshold that represents a logic HIGH level in the system.
- **$V_{\text{T-}}$ (negative-going threshold)**: the input voltage threshold that represents a logic LOW level in the system.
- **$V_H$ (hysteresis)**: the difference between the positive-going and negative-going thresholds.

![Diagram](attachment://diagram.png)

**Fig. 1. Definition of $V_{\text{T+}}$, $V_{\text{T-}}$, and $V_H$**

Built in DC hysteresis in logic devices is useful in systems where inputs have some noise due to electromagnetic induction, or cross talk etc. Each input has immunity against noise depending on the amount of hysteresis voltage present.
2. Typical data sheet view

2.1. Recommended operating conditions

### Table 1. Recommended operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ [1]</th>
<th>Max</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>supply voltage</td>
<td>$1.65$ to $5.5$ V</td>
<td>$1.65$</td>
<td>-</td>
<td>$5.5$</td>
<td>-</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_{I}$</td>
<td>input voltage</td>
<td>$0$</td>
<td>-</td>
<td>-</td>
<td>$5.5$</td>
<td>-</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_{O}$</td>
<td>output voltage</td>
<td>Active mode</td>
<td>$0$</td>
<td>$V_{CC}$</td>
<td>-</td>
<td>$V$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CC} = 0$ V; Power-down mode</td>
<td>$0$</td>
<td>-</td>
<td>$5.5$</td>
<td>-</td>
<td>$V$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{amb}$</td>
<td>ambient temperature</td>
<td>$-40$</td>
<td>-</td>
<td>$+125$</td>
<td>°C</td>
<td>$-20$</td>
<td>-</td>
<td>$V$</td>
</tr>
<tr>
<td>$\Delta t/\Delta V$</td>
<td>input transition rise and fall rate</td>
<td>$V_{CC} = 1.65$ V to $2.7$ V</td>
<td>-</td>
<td>$20$</td>
<td>ns/V</td>
<td>$V_{CC} = 2.7$ V to $5.5$ V</td>
<td>-</td>
<td>$10$</td>
</tr>
</tbody>
</table>

2.2. Static characteristics

### Table 2. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>$T_{amb} = -40$ °C to $+85$ °C</th>
<th>$T_{amb} = -40$ °C to $+125$ °C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>HIGH-level input voltage</td>
<td>$V_{CC} = 1.65$ V to $1.95$ V</td>
<td>$0.65V_{CC}$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$V_{CC} = 2.3$ V to $2.7$ V</td>
<td>$1.7$</td>
<td>-</td>
<td>-</td>
<td>$1.7$</td>
<td>-</td>
</tr>
<tr>
<td>$V_{CC} = 2.7$ V to $3.6$ V</td>
<td>$2.0$</td>
<td>-</td>
<td>-</td>
<td>$2.0$</td>
<td>-</td>
</tr>
<tr>
<td>$V_{CC} = 4.5$ V to $5.5$ V</td>
<td>$0.7V_{CC}$</td>
<td>-</td>
<td>-</td>
<td>$0.7V_{CC}$</td>
<td>-</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>LOW-level input voltage</td>
<td>$V_{CC} = 1.65$ V to $1.95$ V</td>
<td>-</td>
<td>-</td>
<td>$0.35V_{CC}$</td>
</tr>
<tr>
<td>$V_{CC} = 2.3$ V to $2.7$ V</td>
<td>-</td>
<td>-</td>
<td>$0.7$</td>
<td>-</td>
<td>$0.7$</td>
</tr>
<tr>
<td>$V_{CC} = 2.7$ V to $3.6$ V</td>
<td>-</td>
<td>-</td>
<td>$0.8$</td>
<td>-</td>
<td>$0.8$</td>
</tr>
<tr>
<td>$V_{CC} = 4.5$ V to $5.5$ V</td>
<td>-</td>
<td>-</td>
<td>$0.3V_{CC}$</td>
<td>-</td>
<td>$0.3V_{CC}$</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>LOW-level output voltage</td>
<td>$V_{I} = V_{IH}$ or $V_{IL}$</td>
<td>$I_{O} = 100$ μA; $V_{CC} = 1.65$ V to $5.5$ V</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$I_{O} = 4$ mA; $V_{CC} = 1.65$ V</td>
<td>-</td>
<td>-</td>
<td>$0.45$</td>
<td>-</td>
<td>$0.70$</td>
</tr>
<tr>
<td>$I_{O} = 8$ mA; $V_{CC} = 2.3$ V</td>
<td>-</td>
<td>-</td>
<td>$0.3$</td>
<td>-</td>
<td>$0.45$</td>
</tr>
<tr>
<td>$I_{O} = 12$ mA; $V_{CC} = 2.7$ V</td>
<td>-</td>
<td>-</td>
<td>$0.4$</td>
<td>-</td>
<td>$0.60$</td>
</tr>
<tr>
<td>$I_{O} = 24$ mA; $V_{CC} = 3.0$ V</td>
<td>-</td>
<td>-</td>
<td>$0.55$</td>
<td>-</td>
<td>$0.80$</td>
</tr>
<tr>
<td>$I_{O} = 32$ mA; $V_{CC} = 4.5$ V</td>
<td>-</td>
<td>-</td>
<td>$0.55$</td>
<td>-</td>
<td>$0.80$</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>HIGH-level output voltage</td>
<td>$V_{I} = V_{IH}$ or $V_{IL}$</td>
<td>$I_{O} = -100$ μA; $V_{CC} = 1.65$ V to $5.5$ V</td>
<td>$V_{CC} = 0.1$</td>
<td>-</td>
</tr>
<tr>
<td>$I_{O} = -4$ mA; $V_{CC} = 1.65$ V</td>
<td>$1.2$</td>
<td>-</td>
<td>-</td>
<td>$0.95$</td>
<td>-</td>
</tr>
<tr>
<td>$I_{O} = -8$ mA; $V_{CC} = 2.3$ V</td>
<td>$1.9$</td>
<td>-</td>
<td>-</td>
<td>$1.7$</td>
<td>-</td>
</tr>
<tr>
<td>$I_{O} = -12$ mA; $V_{CC} = 2.7$ V</td>
<td>$2.2$</td>
<td>-</td>
<td>-</td>
<td>$1.9$</td>
<td>-</td>
</tr>
<tr>
<td>$I_{O} = -24$ mA; $V_{CC} = 3.0$ V</td>
<td>$2.3$</td>
<td>-</td>
<td>-</td>
<td>$2.0$</td>
<td>-</td>
</tr>
<tr>
<td>$I_{O} = -32$ mA; $V_{CC} = 4.5$ V</td>
<td>$3.8$</td>
<td>-</td>
<td>-</td>
<td>$3.4$</td>
<td>-</td>
</tr>
</tbody>
</table>
### Logic data sheet parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>$T_{\text{amb}} = -40 , ^\circ\text{C} \text{ to } +85 , ^\circ\text{C}$</th>
<th>$T_{\text{amb}} = -40 , ^\circ\text{C} \text{ to } +125 , ^\circ\text{C}$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_I$</td>
<td>input leakage current</td>
<td>$V_I = 5.5 , \text{V or GND}; \ V_{\text{CC}} = 0 , \text{V to } 5.5 , \text{V}$</td>
<td>-</td>
<td>±0.1</td>
<td>±1</td>
</tr>
<tr>
<td>$I_{OZ}$</td>
<td>OFF-state output current</td>
<td>$V_I = V_{\text{IL}}$; \ $V_O = 5.5 , \text{V or GND}; \ V_{\text{CC}} = 3.6 , \text{V}$</td>
<td>-</td>
<td>±0.1</td>
<td>±2</td>
</tr>
<tr>
<td>$I_{OFF}$</td>
<td>power-off leakage current</td>
<td>$V_I \text{ or } V_O = 5.5 , \text{V}; \ V_{\text{CC}} = 0 , \text{V}$</td>
<td>-</td>
<td>±0.1</td>
<td>±2</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>supply current</td>
<td>$V_I = 5.5 , \text{V or GND}; \ V_{\text{CC}} = 1.65 , \text{V to } 5.5 , \text{V}; \ I_O = 0 , \text{A}$</td>
<td>-</td>
<td>0.1</td>
<td>4</td>
</tr>
<tr>
<td>$\Delta I_{CC}$</td>
<td>additional supply current per pin; $V_I = V_{\text{CC}} - 0.6 , \text{V}; \ I_O = 0 , \text{A}; \ V_{\text{CC}} = 2.3 , \text{V to } 5.5 , \text{V}$</td>
<td>-</td>
<td>5</td>
<td>500</td>
<td>-</td>
</tr>
<tr>
<td>$C_I$</td>
<td>input capacitance</td>
<td>-</td>
<td>2</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

---

[1] Typical values are measured at $V_{\text{CC}} = 3.3 \, \text{V}$ and $T_{\text{amb}} = 25 \, ^\circ\text{C}$. 

---

© Nexperia B.V. 2019. All rights reserved.
3. Analog switches

**R\text{ON}** (ON resistance): the effective ON state resistance of an analog switch, at a specified voltage across the switch, output load and V\text{CC}.

**R\text{ON}(\text{peak})** (ON resistance (peak)): the maximum ON state resistance of an analog switch, over the allowed input voltage range.

**R\text{ON}(\text{rail})** (ON resistance (rail)): the ON state resistance of an analog switch, at an input voltage equal to supply voltage or ground.

**ΔR\text{ON}** (ON resistance mismatch between channels): the difference in ON resistance between any two analog switches within a device.

**R\text{ON}(\text{flat})** (ON resistance (flatness)): the difference in ON resistance of an analog switch over the allowed input voltage range.

**C\text{S(ON)}** (ON-state capacitance): the internal capacitance seen at an analog switch terminal when the switch is closed or ON.

**C\text{S(OFF)}** (OFF-state capacitance): the internal capacitance seen at an analog switch terminal when the switch is open or OFF.

**V\text{ct}** (crosstalk voltage): crosstalk between digital inputs and an analog switch terminal, at a specified input signal and load.

**X\text{talk}** (crosstalk): crosstalk between different analog switch terminals, at a specified input signal and load.

**f\text{(3DB)}** (-3 dB frequency response): bandwidth of an analog switch, at a specified input signal and load.

**THD** (total harmonic distortion): total harmonic distortion of a signal due to an analog switch, at a specified input signal and load.

**α\text{iso}** (isolation (OFF-state)): OFF-state isolation between terminals of a disabled analog switch, at a specified input voltage and load.

**Q\text{inj}** (charge injection): charge injected from a digital control pin to the path of an analog switch, at a specified input voltage and load.

![Fig. 2. OFF isolation test circuit](image)

**Charge injection:** As the switch turns ON or OFF, small amounts of charge can be injected from digital control signal in the path of analog control signals. It can also be seen as enable to output cross talk i.e. changing the state on control pin causes a charge to be coupled on the channel of transistor introducing signal noise.

**Total Harmonic Distortion:** When a signal passes through a non-ideal, non-linear device, additional content is added at the harmonics of the original frequencies. THD is a measurement of the extent of that distortion. Mathematically, THD can be defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

Lesser THD allows the components in a loudspeaker, amplifier or microphone or other equipment to produce a more accurate reproduction by reducing harmonics added by electronics and audio media. A THD rating < 1% is considered to be in high-fidelity and inaudible to the human ear.
4. AC switching parameters

\(\Delta t/\Delta V\) (input transition rise and fall rate): the rate at which the inputs are permitted to change from LOW to HIGH or HIGH to LOW.

\(t_r\) (rise time): the time taken for a signal to rise, usually measured from 10% to 90% of final level.

\(t_f\) (fall time): the time taken for a signal to fall, usually measured from 90% to 10% of final level.

\(t_{pd}\) (propagation delay): the time taken for a signal to rise, usually measured from 10% to 90% of final level.

\(t_{PLH}\) (LOW to HIGH propagation delay): the time required for a transition of an input to produce a LOW to HIGH transition on an output, at a specified output load and \(V_{CC}\).

\(t_{PHL}\) (HIGH to LOW propagation delay): the time required for a transition of an input to produce a HIGH to LOW transition on an output, at a specified output load and \(V_{CC}\).

\(t_{TLH}\) (LOW to HIGH output transition time): the time required for an output signal to rise, usually measured from 10% to 90% of the final level.

\(t_{THL}\) (HIGH to LOW output transition time): the time required for an output signal to fall, usually measured from 10% to 90% of the final level.

\(t_w\) (pulse width): the time between the leading and trailing edges of a pulse, at specified levels and \(V_{CC}\).

\(t_h\) (hold time): the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input in order to ensure continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

\(t_{su}\) (set-up time): the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input in order to ensure recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

\(t_{PHZ}\) (HIGH to OFF-state propagation delay): the time required for a transition of an input to produce a HIGH to OFF-state transition on an output, at a specified output load and \(V_{CC}\).

\(t_{PLZ}\) (LOW to OFF-state propagation delay): the time required for a transition of an input to produce a LOW to OFF-state transition on an output, at a specified output load and \(V_{CC}\).

\(t_{PZH}\) (OFF-state to HIGH propagation delay): the time required for a transition of an input to produce an OFF-state to HIGH transition on an output, at a specified output load and \(V_{CC}\).

\(t_{PZL}\) (OFF-state to LOW propagation delay): the time required for a transition of an input to produce an OFF-state to LOW transition on an output, at a specified output load and \(V_{CC}\).

\(t_{en}\) (enable time): the time required for a transition of an input to produce an OFF-state to LOW transition or an OFF-state to HIGH transition on an output, at a specified output load and \(V_{CC}\).

\(t_{dis}\) (disable time): the time required for a transition of an input to produce a LOW to OFF-state transition or a HIGH to OFF-state on an output, at a specified output load and \(V_{CC}\).

\(t_{rec}\) (recovery time): the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input.

\(t_{sko}\) (output skew time): the difference in propagation delay of outputs of a single device with all inputs switching simultaneously, under identical load conditions.

\(f_i\) (input frequency): the frequency of a signal applied to an input.

\(f_o\) (output frequency): the frequency of an output signal.

\(f_{max}\) (maximum frequency): the maximum frequency of operation. Outputs should switch between 10% and 90% of \(V_{CC}\).

\(C_i\) (input capacitance): the internal capacitance of an input pin.

\(C_o\) (output capacitance): the internal capacitance of an output pin.
$C_{pd}$ (power dissipation capacitance): equivalent capacitance value of a device or channel of a device for calculating dynamic power dissipation.
5. Revision history

<table>
<thead>
<tr>
<th>Revision number</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0</td>
<td>2019-01-31</td>
<td>This document is updated to the latest Nexperia publication standards</td>
</tr>
<tr>
<td>2.0</td>
<td>2015-10-15</td>
<td>Release version of the document</td>
</tr>
<tr>
<td>1.0</td>
<td>2015-09-23</td>
<td>Draft version of the document</td>
</tr>
</tbody>
</table>
6. Legal information

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer’s own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer’s sole responsibility to determine whether the Nexperia product is suitable and fit for the customer’s applications and products planned, as well as for the planned application and use of customer’s third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer’s applications or products, or the application or use by customer’s third party customer(s). Customer is responsible for doing all necessary testing for the customer’s applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer’s third party customer(s). Nexperia does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translators — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.
List of Tables

Table 1. Recommended operating conditions......................4
Table 2. Static characteristics.............................................. 4
Table 3. Revision history......................................................9
List of Figures

Fig. 1. Definition of VT+, VT- and VH.................................3
Fig. 2. OFF isolation test circuit...........................................6
Contents

1. Electrical characteristics ............................................. 2
  1.1. Currents .............................................................. 2
  1.2. Voltages ............................................................. 3
2. Typical data sheet view .................................................. 4
  2.1. Recommended operating conditions ........................... 4
  2.2. Static characteristics ............................................ 4
3. Analog switches .......................................................... 6
4. AC switching parameters ............................................... 7
5. Revision history ........................................................ 9
6. Legal information ........................................................ 10

© Nexperia B.V. 2019. All rights reserved

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 31 January 2019