AN11304

MOSFET load switch PCB with thermal measurement

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Document information

Info	Content
Keywords	Load switch, MOSFETs, DFN2020MD-6 (SOT1220), DFN2020-6 (SOT1118); DFN3333-8 (SOT873-1), thermal resistance
Abstract	This document describes a demonstration Printed-Circuit Board (PCB) with identical load switch MOSFET crystals in a DFN2020, DFN3333 and an SO-8 package which can be compared depending on their thermal performance. A sensor measures the temperature of the drain pad. A microcontroller calculates a solder point temperature from this measurement result. Finally this value is displayed on an LCD display. With increasing space constraints in compact applications like tablet PCs, ultralight PCs and smartphones, smaller packages are requested to raise the power density.

Revision history

Rev	Date	Description
1	20130125	Initial version

Contact information

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1. Introduction

Modern electronic systems consist of separate functional blocks, which can be activated and deactivated independently. Many systems need a specific turn-on and turn-off sequence for a proper system start and shutdown. In order to save energy and to extend battery life time, some blocks can be activated only if necessary. MOSFETs are used as load path switching element in so-called load switch applications to support this function.

In line with the industry trend towards smaller electronic devices like tablet PCs, ultralight PCs and smartphones, MOSFETs in smaller packages are used in the designs. Modern MOSFETs can combine a low turn-on resistance with small space requirements paving the road towards a higher power density, measured in Watts per mm^2.

This document describes a demonstration PCB with identical MOSFET crystals in a DFN2020, a DFN3333 and an SO-8 package which can be compared depending on their thermal performance. A sensor measures the temperature of each drain pad. A microcontroller calculates a solder point temperature from this measurement result. Finally this value is displayed on an LCD display.

2. Load switch topologies

2.1 High-side switch

In many applications, the positive supply voltage shall be switched. A load switch usually consists of a switching element in the load path itself and a second electronic part as control element. Figure 1 shows the general structure of a high-side load switch.

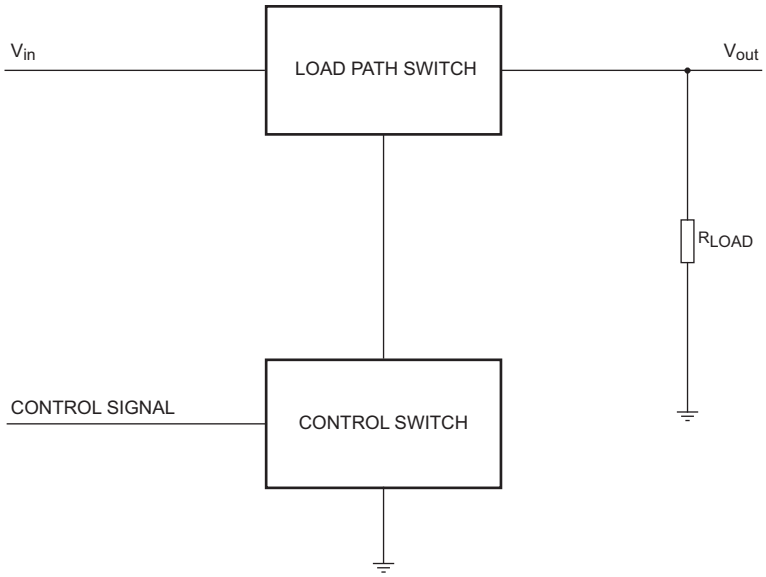


Fig 1. General structure of a high-side load switch

For the switches, MOSFETs are the most efficient solution because they are controlled by a voltage only: they do not generate static control losses. In a bipolar transistor, a permanent base current must be provided in the ON-state. The most simple circuit for a

MOSFET-based high-side load switch is depicted in Figure 2. The schematic shows body diodes which are part of every MOSFET reminding that MOSFETs cannot provide a reverse current protection.

A P-channel FET is applied in the load path. It switches on if the gate is pulled down to ground via the N-channel control FET. The resistor R1 is required to get the load path FET properly switched off and to get the parasitic capacitors of the transistor discharged. A complete resistor divider built by the resistors R1 and R2 is only needed if the input voltage V_{in} is higher than the maximum allowed gate-source voltage V_{GS} of the P-channel FET. The usage of a control FET has the advantage, that the load switch can handle rather high voltages in the load path. Moreover the control voltage of the control FET can be in the range of output voltages of logic ICs and processors. For a direct control of the P-channel FET, the high level of the control signal must be as high as V_{in}. This is not possible in many cases. The control FET works as a level translator and the complete load switch works with a positive control logic. So a high signal at the control input switches on the load path.

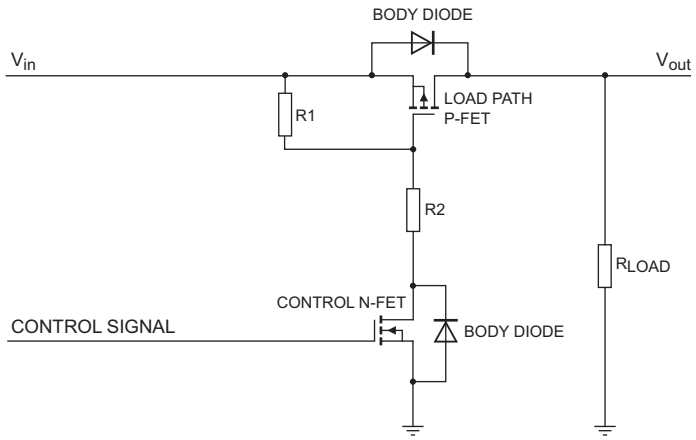


Fig 2. High-side load switch based on a P-channel FET in the load path and an N-channel FET in the control path

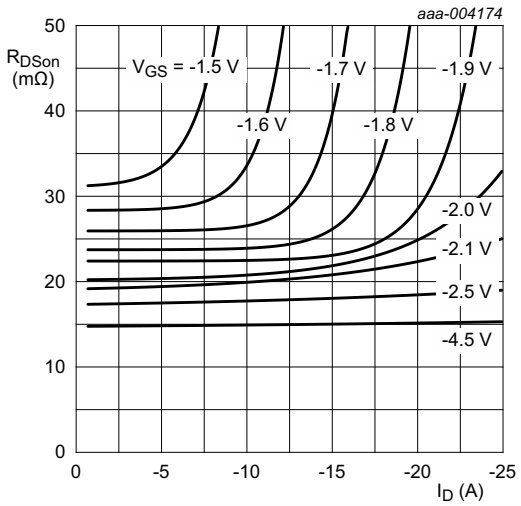
The calculation of the losses of this application is rather simple. There are the drain-source on-state resistance R_{DSon} losses of the P-channel FET and very small losses in the control path in the resistors R1 and R2.

$$P_{tot} = (I_{load})^2 \times R_{DSon} + (V_{in})^2 / (R1 + R2) \quad (1)$$

The second term of Equation 1 can be neglected in most cases because there is no significant current needed in the gate path. A standard load switch is operated in a quasi-static scenario without tough requirements for switching times.

A very important aspect for the dimensioning of the resistor divider is a suitable target for the gate-source voltage of the P-channel FET. Figure 3 shows the R_{DSon} curves versus the drain current I_D for PMPB15XP as an example. This diagram shows clearly that it is not sufficient to apply a gate voltage close to the gate-source threshold voltage $V_{GS(th)}$ to switch a higher load current. $V_{GS(th)}$ typical value is 0.68 V for PMPB15XP. This threshold voltage is defined for a rather low drain current (I_D = 250 μA for PMPB15XP). The consideration of the data sheet curves in Figure 3 and the worst case tolerances are

mandatory for a safe design of a load switch. The circuit topology on Figure 2 has a limitation in case that very small voltages have to be switched because V_{GS} cannot exceed V_{in} for the load path P-channel FET.



T_j = 25 °C

Fig 3. PMPB15XP P-channel FET: Drain-source on-state resistance as a function of drain current; typical values

Figure 4 shows a high-side load switch topology supporting switching of low input voltages. An auxiliary voltage V_{aux} higher than V_{in} provides enough headroom to activate the N-channel FET in the load path. In most of the computing and consumer applications, higher voltages of 5 V or 3.3 V are available in the system. In case a positive control logic is required, two N-channel FETs are implemented in the control path. The first FET operates as an inverter. With a dual FET, the package count is not increased. Dual FETs like NX3020NAKS (SOT363) and NX3020NAKV (SOT666) with a $V_{DS(max)}$ of 30 V or NX7002AKS (SOT363) and 2N7002BKV (SOT666) with a $V_{DS(max)}$ of 60 V are suitable components for this purpose.

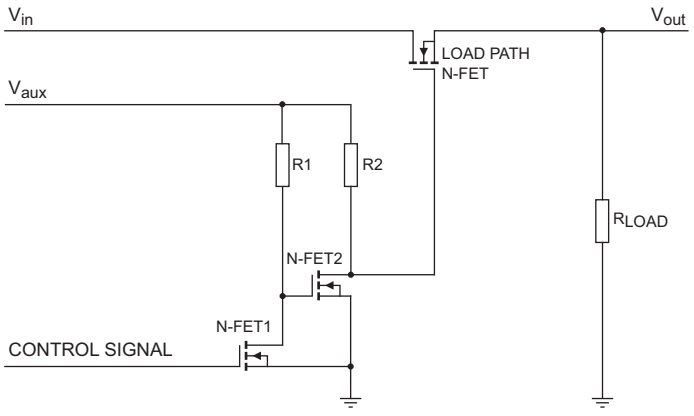


Fig 4. High-side load switch based on an N-channel FET in the load path

2.2 Low-side switch

If the load path switching element is placed into the ground connection of the load, the topology is called low-side switch. The control is getting even more simple compared to the high-side switch because in most cases an N-channel FET can be controlled directly from a driving device. Figure 5 depicts the schematic diagram.

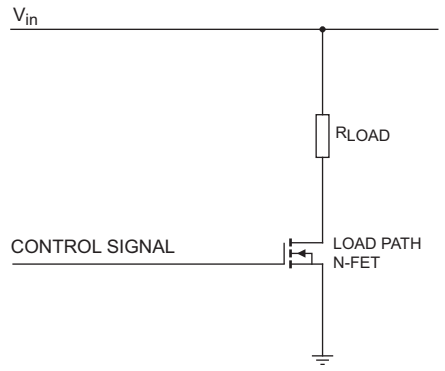


Fig 5. Low-side load switch based on an N-channel FET in the load path

3. Demonstration PCB for the evaluation of the thermal performance of MOSFETs in DFN2020, DFN3333 and SO-8

3.1 Hardware of the demonstration PCB

The demo board is designed to allow a comparison of the thermal performance of MOSFETs in the three packages DFN2020MD-6 (SOT1220), DFN3333-8 (SOT873-1) and SO-8 (SOT96). All three FETs are attached to a 1 cm^2 drain pad. Beside these identical mounting conditions, the same crystals are assembled into the packages. The MOSFETs work as low-side switches as shown in the schematic diagram on Figure 6. LEDs indicate the active channel. The load switch FETs are driven by BSS138PW drivers which work as level converters from the microcontroller runing at 3.3 V. Behind the BSS138PW stage, a 5 V drive voltage for the load switches is provided and ensures that the FETs can be switched on properly.

The load must be connected to the output connector of the active FET or FET under test (for example, the output pin DFN2020-OUT). The other side of the load must be connected to the positive pole of a power supplying the load. The negative poles of the power supplies are connected to the connector LOAD_GND on the PCB, so that a loop for the load current is closed once the FET is switched on.

In the center of each drain pad, there is a PMBT3904MB NPN-transistor in a DFN1006B-3 (SOT883B) package. These bipolar transistors work as temperature sensors. The temperature measurement is based on the forward voltage variation ΔV_F of a silicon PN-diode versus temperature. The thermal coefficient of V_F (typical) for a silicon diode at an operation point with a small current is approximately:

$$\Delta V_F / \Delta T = -1,7 \frac{mV}{K} \quad (2)$$

It means that the voltage across a diode decreases the higher the temperature gets. On the demo board, an NE1617ADS temperature monitor IC converts the input voltage into a readable temperature value. The NE1617ADS has an internal sensor and one interface towards an external temperature sensor. In the application, the temperature of three drain pads must be measured independently via the single input of NE1617ADS. Therefore three separate sensors are required. A selection circuit choses then one of the three load path FETs.

On Figure 6 the FETs Q1, Q3 and Q5 (NX3008NBKT in SOT416 package) can select one sensor out of three. The corresponding selection signals are generated by the microcontroller IC2. The temperature data of the NE1617ADS is read by the microcontroller. The temperature measured in the center of the pad is calculated towards the solder-point temperature T_{sp}. A specific correction factor was defined based on infrared photographs taken from the board.

The software of the demo PCB has 5 states or modes. These modes can be toggled with the center push-button SW1. The first mode is the reset status. In this mode, a ticker message appears on the display and no output is active. After button SW1 is pushed, the LCD display shows the message ‘All Off’. In the next states, the three load switch stages are activated, starting with the SO-8 (SOT96), followed by the DFN3333-8 (SOT873-1) and finally the DFN2020MD-6 stage. The last 4 states (All Off, SO-8, DFN3333, DFN2020) are circling around if the button is pushed further. In the states where an output is activated, T_{sp} of the chosen channel is displayed in the second row of the LCD display. The right button on the PCB (SW2) is a reset button and puts the hardware into the reset state. A MAX811-T voltage monitor (manufactured by Maxim Integrated) generates a reset pulse whenever the supply of the microcontroller falls below a critical level. It also removes bouncing of the signal from the reset button.

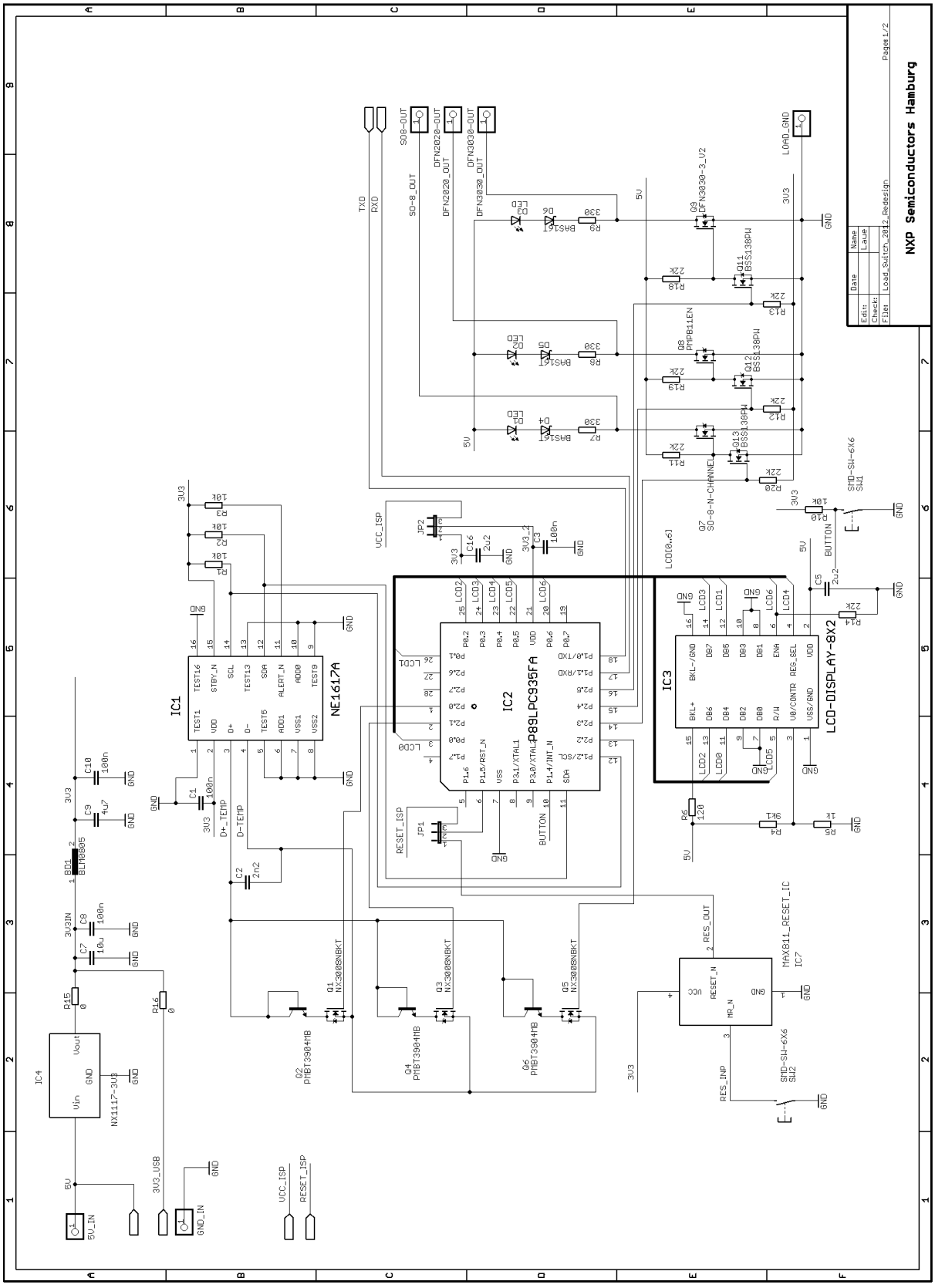


Fig 6. Circuit diagram load switch demo PCB part 1: load switches, microcontroller, temperature measurement

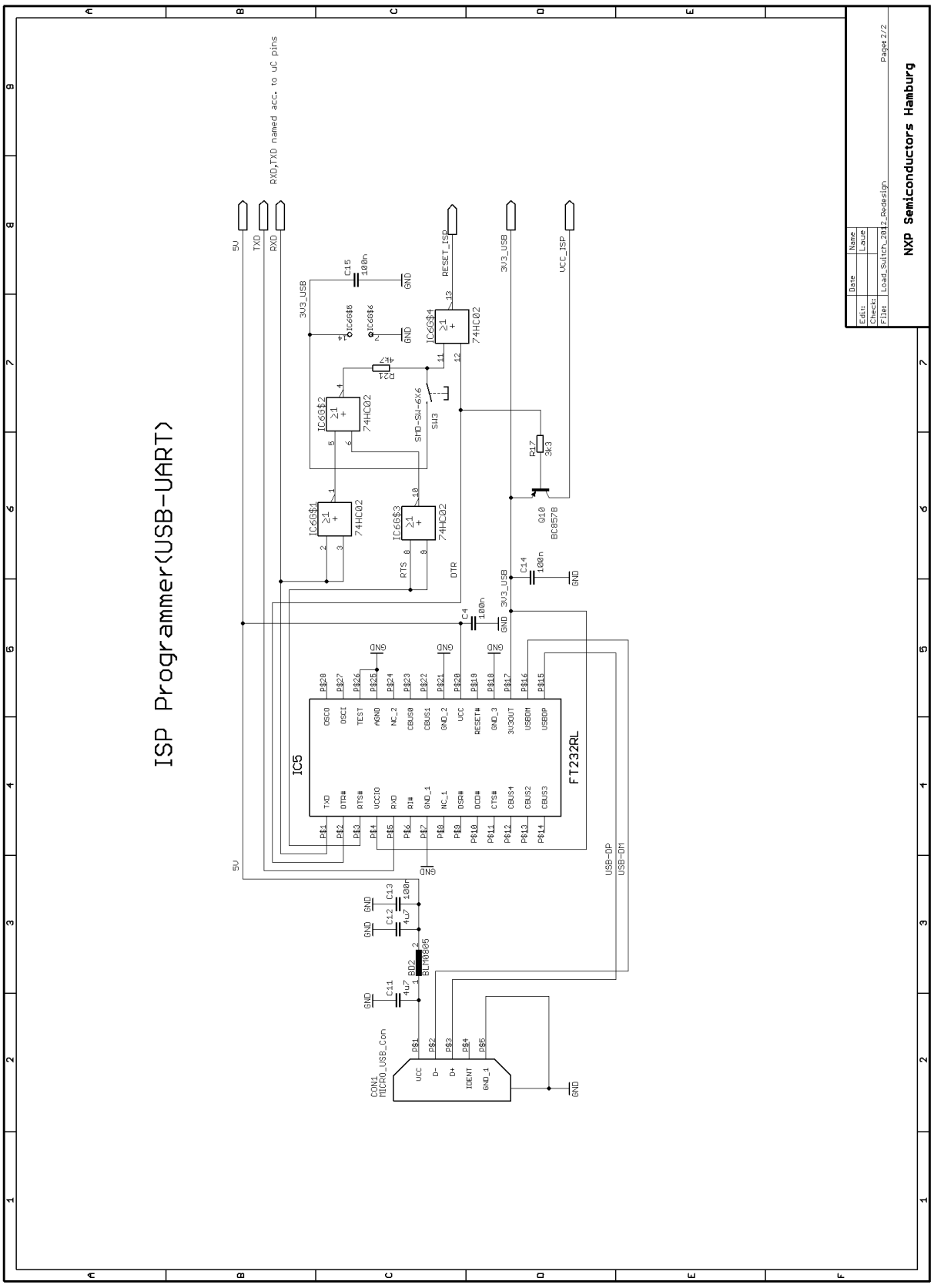


Fig 7. Circuit diagram load switch demo PCB part 2: USB-port and programming interface

The demo board does not need any specific power supply. An external connection micro-USB is sufficient. The 5 V supply from the USB connector powers the microcontroller P89LPC935, the NE1617ADS, the LCD display with its LED backlight and the USB to serial Universal Asynchronous Receiver and Transmitter (UART) interface circuit FT232RL (manufactured by Future Technology Devices International Ltd.).

From the 5 V-USB a 3.3 V supply can either be generated by a NX1117C33Z LDO or via an integrated LDO in the FT232RL. The desired path can be chosen via the assembly of R15 or R16.

The P89LPC935 microcontroller can be programmed easily on the board. Figure 7 shows the schematic diagram with the USB port and the interface chip FT232RL. For flashing of the microcontroller, both jumpers (JP1 and JP2) have to be located in the upper position in order to put the hardware into the In-System Programming (ISP) mode. Afterwards a new software can be flashed using for example, the NXP Semiconductors freeware programming tool 'Flash Magic' (Ref. 1 "AN11248") which can be downloaded from the Internet. After flashing, the jumpers must be put back into the lower position (away from the display). Figure 8 shows the placement of the components on the PCB.

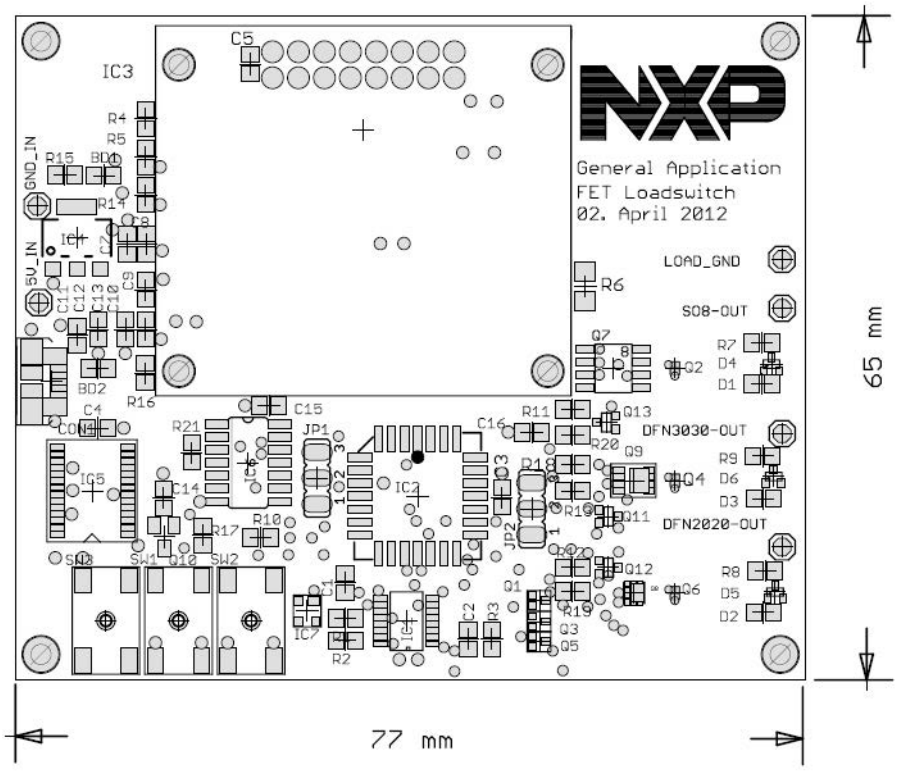


Fig 8. Load switch board, component placement

3.2 MOSFET portfolio in DFN2020 suitable for load switching

Table 1 shows an overview of the NXP Semiconductors single P-channel MOSFETs in the DFN2020MD-6 (SOT1220) package. Types can be provided with a maximum V_{DS} rating of 30 V, 20 V and 12 V. Furthermore a gate specification with a maximum V_{GS} of ±12 V and ±20 V can be supported. For switching of lower input voltages, the products with the lower V_{GS} limits are recommended because of the lower gate-source voltage threshold. The lowest R_{DSon} value is typically 15 mΩ for PMPB15XP.

Table 1. Single P-channel MOSFET in DFN2020MD-6 (SOT1220)

Type number	Drain-source voltage V_{DS} (V)	Gate-source voltage V_{GS} (V)	Drain-source on-state resistance R_{DSon} (mΩ) V_{GS} = 4.5 V		Gate-source threshold voltage $V_{GS(th)}$ (V) I_D = 250 µA; V_{DS} = V_{GS}			ESD protection [1]
			Typ	Max	Min	Typ	Max	
PMPB15XP	–12	±12	15	19	–0.47	–0.68	–0.9	-
PMPB19XP	–20	±12	19	22.5	–0.47	–0.68	–0.9	-
PMPB33XP	–20	±12	30	37	–0.47	–0.68	–0.9	-
PMPB47XP	–30	±12	47	58	–0.47	–0.68	–0.9	-
PMPB27EP	–30	±20	32	43	–1	–1.5	–2.5	-
PMPB48EP	–30	±20	55	76	–1	–1.5	–2.5	-
PMPB20XPE	–20	±12	19	23.5	–0.47	–0.68	–0.9	2.4 kV
PMPB29XPE	–20	±12	28	32.5	–0.47	–0.68	–0.9	2.3 kV
PMPB43XPE	–20	±12	39	48	–0.47	–0.68	–0.9	2.3 kV

[1] ESD: ElectroStatic Discharge

Table 2 shows the list of available N-channel MOSFETs in DFN2020MD-6 (SOT1220). The V_{DS} maximum ratings range from 60 V to 20 V. The PMPB10XNE provides an R_{DSon} of 10 mΩ only at V_{GS} = 4.5 V.

Table 2. Single N-channel MOSFET in DFN2020MD-6 (SOT1220)

Type number	Drain-source voltage V_{DS} (V)	Gate-source voltage V_{GS} (V)	Drain-source on-state resistance R_{DSon} (mΩ) V_{GS} = 4.5 V		Gate-source threshold voltage $V_{GS(th)}$ (V) I_D = 250 µA; V_{DS} = V_{GS}			ESD protection
			Typ	Max	Min	Typ	Max	
PMPB40SNA	60	±16	40	50	1	1.7	3	-
PMPB11EN	30	±20	14	16.5	1	1.5	2	-
PMPB20EN	30	±20	20.5	24.5	1	1.5	2	-
PMPB16XN	30	±12	16	21	0.5	1	1.5	-
PMPB33XN	30	±12	37	47	0.45	0.8	1.2	-
PMPB15XN	20	±12	18	21	0.4	0.65	0.9	-
PMPB12UN	20	±8	14	18	0.4	0.7	1	-
PMPB20UN	20	±8	19	25	0.4	0.7	1	-
PMPB13XNE	30	±12	13	16	0.4	0.65	0.9	2.2 kV
PMPB29XNE	30	±12	28	33	0.4	0.65	0.9	2.1 kV
PMPB10XNE	20	±12	10	14	0.4	0.65	0.9	2.2 kV
PMPB23XNE	20	±12	19	22	0.4	0.65	0.9	2.1 kV

In many cases load switches are supposed to provide a reverse protection. It is the case for charger applications where the battery shall not be able to drive back a current towards the charger input plug. Other common use cases are switches for AC loads, where the switch must be in a high impedance condition for both polarities across the deactivated switch. As already depicted in Figure 2, MOSFETs do not provide a reverse blocking due to the inherent body diode. This problem can be solved by using two MOSFETs in a so-called back-to-back configuration; see Figure 9.

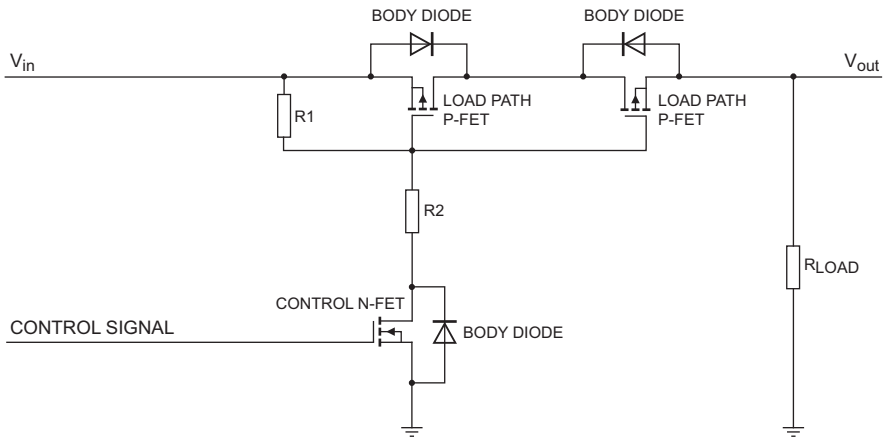


Fig 9. Load switch with back-to-back configuration for MOSFETs providing a reverse current protection

If the thermal requirements and R_{DSon} requirements advice such a design, the back-to-back configuration can be realized using two single MOSFETs in separate packages. However NXP Semiconductors offers a large variety of dual MOSFETs in 2 mm × 2 mm packages. They allow a very compact realization of a reverse current protected load switch. Table 3 shows a list of these products.

Table 3. Dual MOSFET in DFN2020-6 (SOT1118)

Type Name	Configuration	Polarity	Drain-source voltage V_{DS} (V)	Gate-source voltage V_{GS} (V)	Drain-source on-state resistance R_{DSon} (mΩ) V_{GS} = 4.5 V		ESD protection
					Typ	Max	
PMDPB58UPE	dual	P-channel	−20	±8	58	67	2.0 kV
PMDPB70XPE	dual	P-channel	−20	±12	66	79	2.0 kV
PMDPB85UPE	dual	P-channel	−20	±8	82	103	2.0 kV
PMDPB55XP	dual	P-channel	−20	±12	55	70	-
PMDPB70XP	dual	P-channel	−30	±12	70	87	-
PMDPB80XP	dual	P-channel	−20	±12	80	102	-
PMDPB38UNE	dual	N-channel	20	±8	38	46	1.6 kV
PMDPB95XNE	dual	N-channel	30	±12	95	120	1.8 kV
PMDPB28UN	dual	N-channel	20	±8	30	37	-
PMDPB30XN	dual	N-channel	20	±12	32	40	-
PMDPB42UN	dual	N-channel	20	±8	40	50	-
PMDPB56XN	dual	N-channel	30	±12	55	73	-

Table 3. Dual MOSFET in DFN2020-6 (SOT1118) *...continued*

Type Name	Configuration	Polarity	Drain-source voltage V_{DS} (V)	Gate-source voltage V_{GS} (V)	Drain-source on-state resistance R_{DSon} (mΩ) V_{GS} = 4.5 V		ESD protection
					Typ	Max	
PMDPB70EN	dual	N-channel	30	±20	67	88	-
PMCPB5530X	complementary	P-channel	−20	±12	55	70	-
		N-channel	20	±12	26	34	-
PMFPB8032XP	MOSFET + Schottky diode	P-channel	−20	±12	80	102	-
PMFPB8040XP	MOSFET + Schottky diode	P-channel	−20	±12	80	102	-
PMC85XP	MOSFET + RET transistor	P-channel	−30	±12	85	110	-

3.3 Thermal performance results for the demo board

The PMPB11EN is assembled as DFN2020MD-6 (SOT1220) type on the NXP demo PCB. The crystal of this MOSFET was assembled into a DFN3333-8 (SOT873-1) and SO-8 (SOT96) package. The MOSFETs in the larger packages are no commercial types and have been produced for a realistic comparison, where identical dies are tested in different packages.

Figure 10, Figure 11 and Figure 12 show photographs of the demo PCB. They display the temperature after the activated load switch FET had reached its final temperature. Test conditions ensure that no airflow can influence the results.

I_{load} = 6 A

Fig 10. Test with SO-8 (SOT96) package

For the 6 A load current the temperature difference between the three packages was roughly 10 °C from the biggest towards the smallest package.

I_{load} = 6 A

Fig 11. Test with DFN3333-8 (SOT873-1) package

I_{load} = 6 A

Fig 12. Test with DFN2020MD-6 (SOT1220) package

The demo PCB uses 1 cm^2 drain pads for each MOSFET. The PCB is a standard FR4 board and the copper-layer thickness is 35 μm only. Figure 13 shows an infrared image of the area around the DFN2020MD-6 (SOT1220) MOSFET. The rather high temperature gradient on the drain pad becomes obvious, because the thin copper cannot conduct the heat away like a thicker copper layer of for example, 70 μm. The 70 μm board technology is often used for MOSFET specification boards.

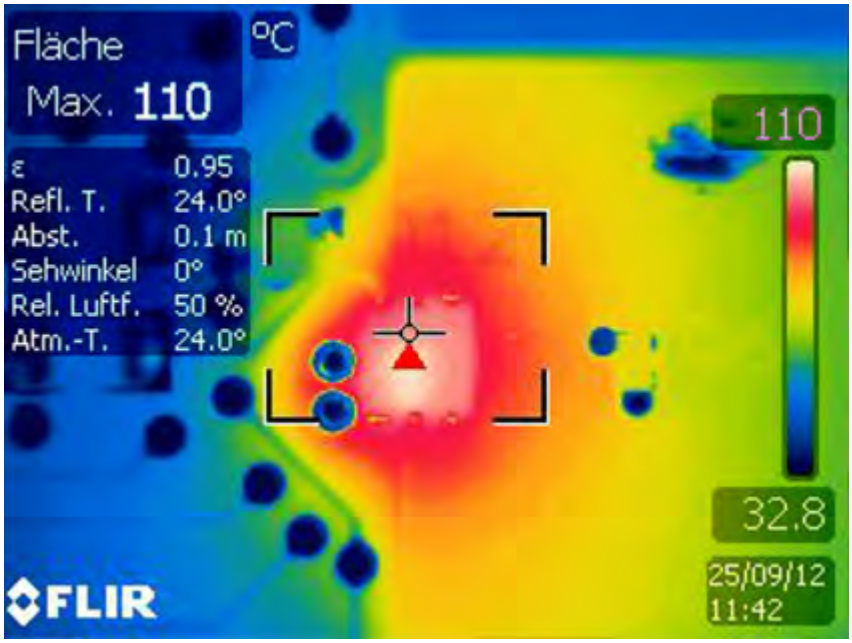


Fig 13. Thermal image of the DFN2020MD-6 (SOT1220)

4. High-power density with MOSFETs in DFN packages

4.1 DFN2020MD-6 (SOT1220) MOSFETs in comparison to DFN3333-8 (SOT873-1) and SO-8 (SOT96)

NXP Semiconductors DFN packages allow handling comparably high power in a small package with a small mounting area. Figure 14 shows this fact in a very compelling way. The mounting area is of about 30 mm^2 for a SO-8 (SOT96), 10 mm^2 for a DFN3333-8 (SOT873-1) and 4 mm^2 for a DFN2020MD-6 (SOT1220). The power density of the DFN2020MD-6 (SOT1220) exceeds the values of the other packages with 425 mW/mm^2 versus 190 mW/mm^2 for the DFN3333-8 (SOT873-1) and 60 mW/mm^2 for the SO-8 (SOT96) package. The power density values are based on the total power dissipation P_{tot} as specified in the data sheets for a 6 cm^2 drain pad at T_{amb} = 25 °C. The power density value of 425 mW/mm^2 results of P_{tot} = 1.7 W divided by 4 mm^2.

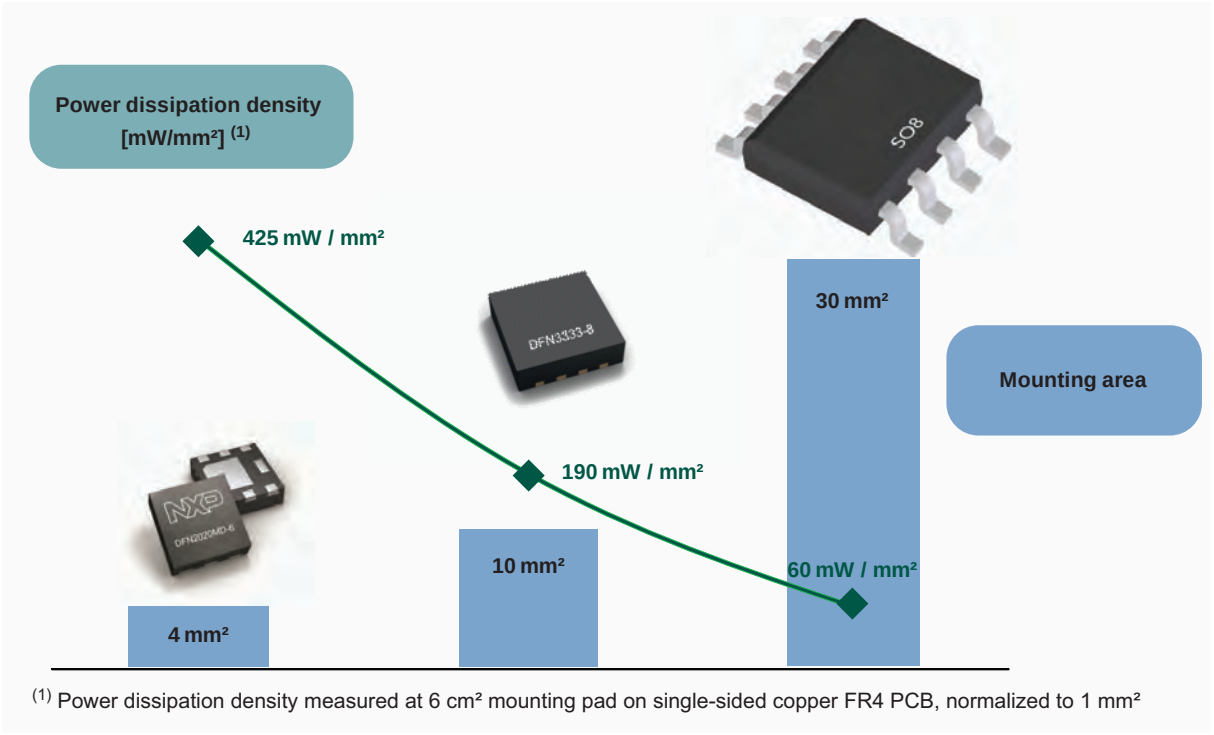


Fig 14. Power dissipation density and mounting area

4.2 DFN1006 packages provide a good thermal performance in smaller sizes

NXP Semiconductors MOSFETs in DFN packages outperform conventional packages in many aspects. Larger dies allow a lower R_{DSon} for a similar mounting area. The good thermal coupling of the comparably large drain pad to the PCB allows dissipating the heat in an optimal way.

Figure 15 shows a comparison of 2 MOSFETs in SOT416 against the corresponding product in a DFN1006 package. The mounting area of a DFN1006 package is significantly smaller with 1.17 mm^2 versus 4.4 mm^2 for the recommended footprints. Although the DFN1006 types require less PCB space, they can support higher maximum drain currents due to the good thermal performance of the DFN packages. These facts are even more obvious when the DFN1006 package is compared to a leaded SOT1208 package which is quite popular for small commodity FETs.

NXP Semiconductors constantly develops a growing portfolio of MOSFETs. Next steps are 1.0 mm × 1.0 mm and 1.6 mm × 1.6 mm products.

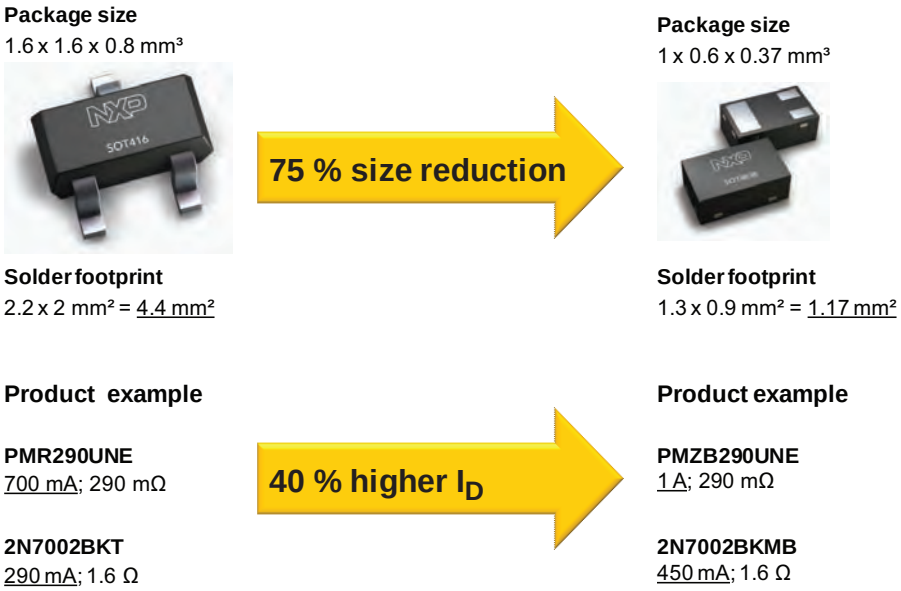


Fig 15. Comparison of SOT416 versus DFN1006 for the examples PMR290UNE/PMZB290UNE and 2N7002BKT/2N7002BKMB

5. Summary

NXP Semiconductors DFN2020MD-6 (SOT1220) single and DFN2020-6 (SOT1118) dual MOSFETs allow more compact designs because of their good electrical and thermal performance. With their increased power density, more power can be handled on a small mounting area. In modern electronic designs like ultralight PCs, tablet PCs and smartphones, space constraints are getting more tough. As these applications are all battery-driven, energy efficiency is also an important selection criterion.

The demo PCB described in this document proves that NXP Semiconductors small DFN package DFN2020MD-6 (SOT1220) can often replace bigger components in DFN3333-8 (SOT873-1) or in SO-8 (SOT96) package.

6. Appendix

The appendix gives further information about the load switch demo PCB. Figure 16 shows the place plan with the component values. Figure 17 depicts the top layer of the board.

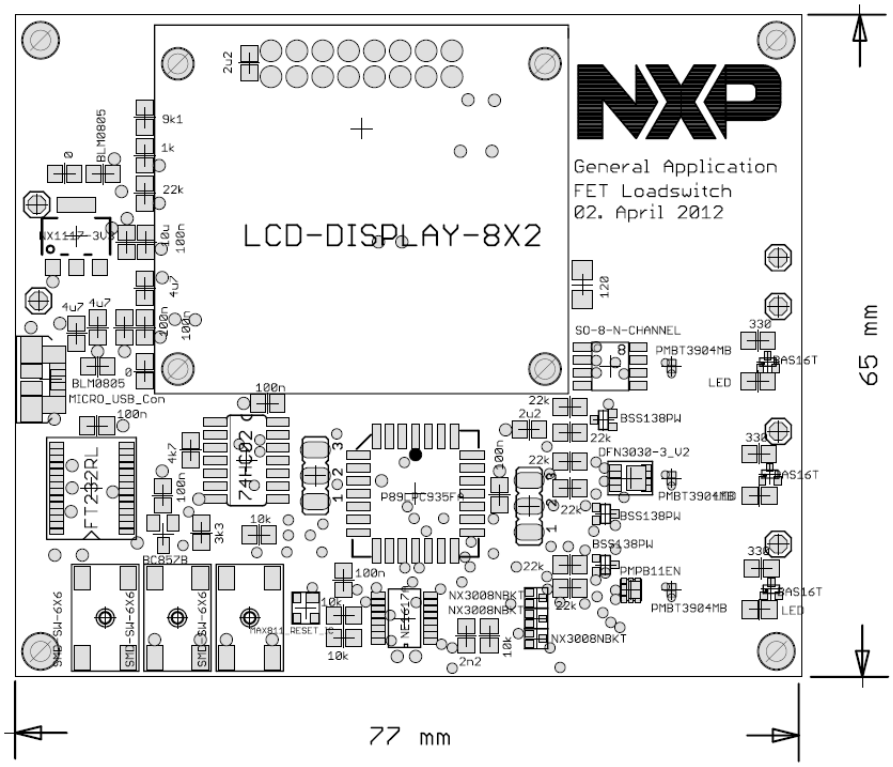


Fig 16. Place plan of the load switch PCB with component values

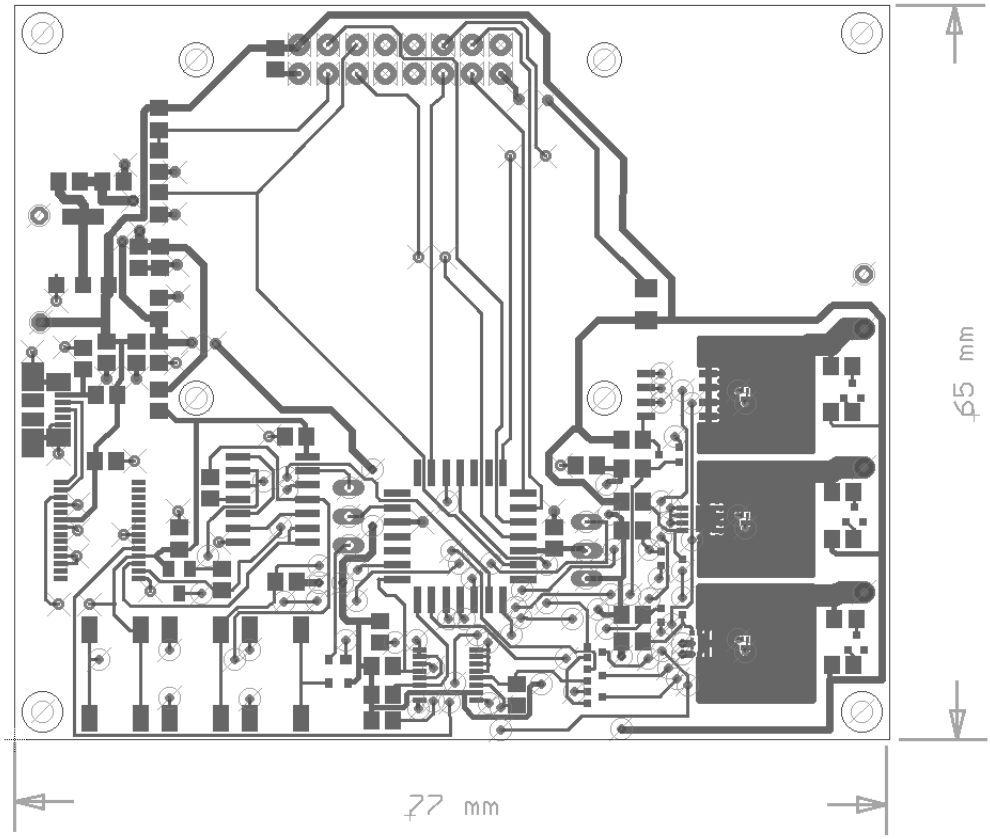


Fig 17. Top layer of the load switch PCB

7. References

[1] **AN11248 —** In-System Programming of LPC18xx/43xx flash

8. Legal information

8.1 Definitions

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9. Contents

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