**Abstract**

Analysis of the thermal performance of discrete semiconductor devices is necessary to efficiently and safely design any system utilizing such devices. This application note presents a quick and inexpensive way to infer the thermal performance using a thermal electrical analogy. This method is applicable to devices such as power MOSFETs, small-signal MOSFETs, diodes and bipolar transistors.

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<td>Analysis of the thermal performance of discrete semiconductor devices is necessary to efficiently and safely design any system utilizing such devices. This application note presents a quick and inexpensive way to infer the thermal performance using a thermal electrical analogy. This method is applicable to devices such as power MOSFETs, small-signal MOSFETs, diodes and bipolar transistors.</td>
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</table>
1. Introduction

The thermal behaviour of discrete semiconductor devices can be predicted using RC thermal models. The model types presented in this application note are known as Foster and Cauer models, consisting in networks of resistors and capacitors. Foster and Cauer models are equivalent representations of the thermal performance of a discrete device and they can be used within a SPICE environment. This document provides some basic theory behind the principle, and how to implement Foster and Cauer RC thermal models. For convenience, Foster and Cauer RC thermal models are referred to as RC models in the rest of this application note. Several methods of using RC thermal models, including worked examples, will be described.

2. Thermal impedance

RC models are derived from the thermal impedance ($Z_{th}$) of a device (see Fig. 1). This figure represents the thermal behavior of a device under transient power pulses. The $Z_{th}$ can be generated by measuring the power losses as a result of applying a step function of varying time periods.

A device subjected to a power pulse of duration $> \sim 1$ second, i.e. steady-state, has reached thermal equilibrium and the $Z_{th}$ plateaus becomes the $R_{th}$. The $Z_{th}$ illustrates the fact that materials have thermal inertia. Thermal inertia means that temperature does not change instantaneously. As a result, the device can handle greater power for shorter duration pulses.

The $Z_{th}$ curves for repetitive pulses with different duty cycles, are also shown in Fig. 1. These curves represent the additional RMS temperature rise due to the dissipation of RMS power.

To assist this discussion, the thermal resistance junction to mounting base ($R_{th(j-mb)}$) from the BUK7S1R0-40H data sheet, has been included in Table 1. The $Z_{th}$ in Fig. 1 also belongs to the BUK7S1R0-40H data sheet. This graph shows the thermal behaviour of a power MOSFET but this method can also be applied for other discrete devices such as diodes or bipolar junction transistor (BJT).

### Table 1. Steady state thermal impedance of BUK7S1R0-40H

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th(j-mb)}$</td>
<td>thermal resistance from junction to mounting base</td>
<td></td>
<td>-</td>
<td>0.35</td>
<td>0.4</td>
<td>K/W</td>
</tr>
</tbody>
</table>

Fig. 1. Transient thermal impedance from junction to mounting base as a function of pulse duration for the BUK7S1R0-40H
3. Calculating junction temperature rise

To calculate the temperature rise within the junction of a semiconductor device with a single active area (i.e. heat source at the junction), the power and duration of the pulse delivered to the device must be known. If the power pulse is a square, then the thermal impedance can be read from the $Z_{th}$ chart. The product of this value with the power gives the temperature rise within the junction.

If constant power is applied to the device, the steady state thermal impedance can be used i.e. $R_{th}$. Again the temperature rise is the product of the power and the $R_{th}$.

For a transient pulse e.g. sinusoidal or pulsed, the temperature rise within the device junction becomes more difficult to calculate.

The mathematically correct way to calculate $T_j$ is to apply the convolution integral. The calculation expresses both the power pulse and the $Z_{th}$ curve as functions of time, and use the convolution integral to produce a temperature profile (see Ref. 2).

$$T_j[\text{rise}] = \int_0^\tau P(t) \cdot \frac{d}{dt} Z_{th}(\tau \cdot t) \, dt$$

(1)

However, this is difficult as the $Z_{th}(\tau \cdot t)$ is not defined mathematically.

An alternative way is to approximate the waveforms into a series of rectangular pulse and apply superposition (see Ref. 1).

While relatively simple, applying superposition has its disadvantages. The more complex the waveform, the more superpositions that must be imposed to model the waveform accurately.

To represent $Z_{th}$ as a function of time, we can draw upon the thermal electrical analogy and represent it as a series of RC charging equations or as an RC ladder. $Z_{th}$ can then be represented in a SPICE environment for ease of calculation of the junction temperature.

4. Association between Thermal and Electrical parameters

The thermal electrical analogy is summarized in Table 2. If the thermal resistance and capacitance of a semiconductor device is known, electrical resistances and capacitances can represent them respectively. Using current as power, and voltage as the temperature difference, any thermal network can be handled as an electrical network.

**Table 2. Fundamental parameters**

<table>
<thead>
<tr>
<th>Type</th>
<th>Resistance</th>
<th>Potential</th>
<th>Energy</th>
<th>Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical</td>
<td>$R = \text{resistance}$ (Ohms)</td>
<td>$V = \text{PD}$ (Volts)</td>
<td>$I = \text{current}$ (Amps)</td>
<td>$C = \text{capacitance}$ (Farads)</td>
</tr>
<tr>
<td>Thermal</td>
<td>$R_{th} = \text{thermal resistance}$ (K/W)</td>
<td>$K = \text{temperature difference}$ (Kelvin)</td>
<td>$W = \text{dissipated power}$ (Watts)</td>
<td>$C_{th} = \text{thermal capacitance}$ (thermal mass)</td>
</tr>
</tbody>
</table>
5. Foster and Cauer RC thermal models

Foster models are derived by semi-empirically fitting a curve to the $Z_{th}$, the result of which is a one-dimensional RC network Fig. 2. The R and C values in a Foster model do not correspond to geometrical locations on the physical device. Therefore, these values cannot be calculated from device material constants as can be in other modeling techniques. Finally, a Foster RC model cannot be divided or interconnected through, i.e. have the RC network of a heat sink connected.

![Fig. 2. Foster RC thermal models](image)

Foster models have the benefit of ease of expression of the thermal impedance $Z_{th}$ as described at the end of Section 2. For example, by measuring the heating or cooling curve and generating a $Z_{th}$ curve, Equation 2 can be applied to generate a fitted curve Fig. 3:

$$Z_{th}(t) = \sum_{i=1}^{n} R_i \cdot \left[ 1 - \exp \left( -\frac{t}{\tau_i} \right) \right]$$

(2)

Where:

$$\tau_i = R_i \cdot C_i$$

(3)

The model parameters $R_i$ and $C_i$ are the thermal resistances and capacitances that build up the thermal model depicted in Fig. 2. The parameters in the analytical expression can be optimized until the time response matches the transient system response by applying a least square fit algorithm.

The individual expression, "i", also draws parallels with the electrical capacitor charging equation. Fig. 3 shows how the individual $R_i$ and $C_i$ combinations, sum to make the $Z_{th}$ curve.

![Fig. 3. Foster RC thermal models](image)

Foster models have no physical meaning since the node-to-node heat capacitances have no physical reality. However, a Foster model can be converted into its Cauer counter-part by means of a mathematical transformation (see Ref. 4).

An n-stage Cauer model can be derived from an n-stage Foster model and they will be equivalent representations of the device thermal performance.
As seen for the Foster model, the Cauer Model also consists of an RC network but the thermal capacitances are all connected to the thermal ground, i.e. ambient temperature as represented in Fig. 4. The nodes in the Cauer Model can have physical meaning and allow access to the temperature of the internal layers of the semiconductor structure.

![Cauer RC thermal models](image)

**Fig. 4. Cauer RC thermal models**

Nexperia provides Foster and Cauer RC models for many of their products on the Product Information Pages, e.g.

- **BUK7S1R0-40H**
- **BC817K-40H**

The models can be found under the tabs “Documentation” and “Support” as shown for BUK7S1R0-40H in Fig. 5.

![Nexperia RC thermal model documentation](image)

**Fig. 5. Nexperia RC thermal model documentation**

Foster and Cauer RC thermal models allow application engineers to perform fast calculations of the transient response of a package to complex power profiles.

In the following sections several examples of using RC thermal models will be presented. Foster models and Cauer models are equivalent representations of the device thermal behaviour but in the described examples Cauer models will be used as more representative of the physical structure of the device.

As shown in Fig. 8, a schematic file is available on Nexperia website for BUK7S1R0-40H Cauer model. Other products may not have this schematic file available and may be provided with a netlist file for the Cauer network as shown in Fig. 6.
Fig. 6.  BUK7S1R0-40H Cauer model netlist

The netlist describes the same Cauer network as in Fig. 8, and can be used to build the same schematic. Pin 1 in the netlist can be identified as the junction temperature pin $T_j$ in the schematic. Similarly pins 6, 7 as the $T_{\text{amb}}$ pins in the schematic.

In order to simulate only the device pins 6 and 7 will both be tied to the ambient voltage source, as shown in Fig. 8.

However, one of the advantages of using Cauer models is to allow to add external networks to the device model, for example to model PCBs, heatsinks etc. In order to do so pin 7 will be tied to ambient and pin 6 to the first pin of the external Cauer network. For correct results, it is fundamental to make sure that the end pin of the external Cauer network is tied to the ambient source.
6. Thermal simulation examples

For highest simulation accuracy, all components losses must be considered, depending on the chosen semiconductor technology:

- Total losses for MOSFETs: \( P = (V_{DS} \times I_D + V_{GS} \times I_G) \)
- Total losses for BJTs: \( P = (V_{CE} \times I_C + V_{BE} \times I_B) \)
- Total losses for diodes: \( P = (V_F \times I_F) \)

6.1. Example 1

RC thermal models are generated from the \( Z_{th} \) curve. This example shows how to work back from an RC model and plot a \( Z_{th} \) curve within a SPICE simulator. It allows for greater ease when trying to read values of the \( Z_{th} \) curve from the data sheet.

This and subsequent examples use the RC thermal model of BUK7S1R0-40H. \( T_{mb} \) represents the mounting base temperature. It is treated as an isothermal and for this example it is set as 0 °C. A single shot pulse of 1 W power is dissipated in the device. Referring to Fig. 7, for a single shot pulse, the time period between pulses is infinite and therefore the duty cycle \( \delta = 0 \). Then the junction temperature \( T_j \) represents the transient thermal impedance \( Z_{th} \).

\[
T_j = T_{mb} + \Delta T = 0 \degree C + \Delta T = \Delta T
\]

\[
\Delta T = P \times Z_{th} = 1W \times Z_{th}
\]

Equation 5 demonstrates that with \( P = 1 \) W, the magnitude of \( Z_{th} \) equates to \( \Delta T \).

The following steps are used to set up and run simulations:

1. set up the RC thermal model of BUK7S1R0-40H in SPICE as shown in Fig. 8
2. set the value of voltage source \( V_{mb} \) to 0, which is the value of \( T_{mb} \)
3. set the value of the current source \( I1 \) to 1
4. create a simulation profile and set the run time to 1 s
5. run the simulation
6. Plot the voltage at node \( T_j \)

Fig. 7. Single-shot pulse
The simulation result in Fig. 9 shows the junction temperature (voltage at $T_j$) which is also the thermal impedance of BUK7S1R0-40H. The values of $Z_{th}$ at different times can be read using the cursors on this plot within SPICE.

The value of the current source in this example is set to 1 A to represent 1 W dissipating through the device. It can be easily changed to represent any value of power. The simulation command can be changed for any duration to represent a range of square power pulses.
6.2. Example 2

Another method of generating the power profile, is to use measurements from the actual circuit. This information is presented to the SPICE simulation in the form of a comma-separated value (CSV) file giving pairs of time/power values. It can be generated either as a summary of observations showing the points of change or from an oscilloscope waveform capture.

Two further methods of generating a power profile are discussed. One method is using a PWL file. The other is to generate the power from a semiconductor device electrical circuit modeled in SPICE. The former is outlined first.

A source within a SPICE simulator can use a PWL file as an input. The contents of a typical PWL file is shown in Table 3. It can list the current, voltage or in this example, power over time. These files can be generated by typing values into a spreadsheet editor and saving as a .csv file, or alternatively exporting waveforms from an oscilloscope. The actual file itself should not contain any column headings.

To implement this procedure within a SPICE environment, follow the same steps as described in Section 6.1 "Example 1", but with the exceptions:

1. Set the property value of the current source to read from a PWL FILE and point it to a .csv file for example: C:\Pulse file\filepulse.csv, which contains the power profile listed in Table 3
2. Set the mounting base $T_{mb} (V_{mb})$ to 125 °C
3. Set the simulation run time to 0.6 s

<table>
<thead>
<tr>
<th>Time (seconds)</th>
<th>Power (Watts)</th>
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<tbody>
<tr>
<td>0.000000</td>
<td>0</td>
</tr>
<tr>
<td>0.000001</td>
<td>120</td>
</tr>
<tr>
<td>0.004000</td>
<td>120</td>
</tr>
<tr>
<td>0.004001</td>
<td>24</td>
</tr>
<tr>
<td>0.004002</td>
<td>24</td>
</tr>
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<td>24</td>
</tr>
<tr>
<td>0.100001</td>
<td>24</td>
</tr>
<tr>
<td>0.100002</td>
<td>80</td>
</tr>
<tr>
<td>0.200000</td>
<td>80</td>
</tr>
<tr>
<td>0.200002</td>
<td>80</td>
</tr>
<tr>
<td>0.200003</td>
<td>0</td>
</tr>
<tr>
<td>0.300000</td>
<td>0</td>
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<tr>
<td>0.300001</td>
<td>80</td>
</tr>
<tr>
<td>0.315000</td>
<td>80</td>
</tr>
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<td>0.315001</td>
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<tr>
<td>0.600000</td>
<td>24</td>
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</table>
Fig. 10. SPICE circuit implementing a PWL file with the thermal model of the BUK7S1R0-40H

The simulation result is shown in Fig. 11. The junction temperature and thermal impedance values labeled in Fig. 11 demonstrate that the $Z_{th}$ value at 4 ms, and $R_{th}$ value, are in line with Fig. 12. It represents the thermal impedance waveform shown in the BUK7S1R0-40H data sheet.
Fig. 11. Simulation results and first power pulse

The red lines highlight the thermal resistance and impedance for the example shown in Fig. 11.

Fig. 12. Transient thermal impedance for BUK7S1R0-40H
6.3. Example 3

The aim of this example is to show how to perform thermal simulation using the power profile generated from a MOSFET circuit.

Following the steps in Section 6.1, set up the thermal model of BUK7S1R0-40H, and set the mounting base temperature to 85 °C.

To set the power value in the current source, construct a MOSFET electrical circuit as provided in Fig. 13. The power supply is 12 V. The gate drive supply is assigned a value of 10 V. It is set to run for 50 cycles with a 1 ms period and a 50 % duty cycle.

The power dissipated in the MOSFET can be calculated from Equation 6 or for greater accuracy; the gate current can be included into the calculation to give Equation 7:

\[ P = V_{ds} \cdot I_d \]  

To improve accuracy:

\[ P = V_{ds} \cdot I_d + V_{gs} \cdot I_g \]  

The current source into the thermal model can now be defined as:

\[ I = V_{(d)} \cdot I(V_d) + V_{(g)} \cdot I(V_g) \]  

Fig. 13 demonstrates the link between the electrical circuit and the thermal model circuit.

The resultant plot of \( T_j \) is shown in Fig. 14. The maximum temperature of the junction can once again be calculated from data sheet values by following the steps outlined in Ref. 1.
7. Discussions

RC thermal models are not perfect. The physical materials used to build Semiconductors have temperature-dependent characteristics. These characteristics mean that thermal resistance is also a temperature-dependent parameter. Whereas in Ohm's law, the Ohmic resistance is usually considered to be constant and independent of the voltage. So the correspondence between electrical and thermal parameters is not perfectly symmetrical but gives a good basis for fundamental thermal simulations.

A further limitation of the models presented is that the mounting base temperature of the device $T_{mb}$, is set as an isothermal. This is rarely the case in real applications where a rise in the mounting base temperature must be considered. This rise is determined by calculating the temperature rise due to the average power dissipation (i.e. the heat flow) from the mounting base through to ambient. It means that the models are of limited use for pulses greater than 1 s, where heat begins to flow into the environment of the device. In this situation, the thermal model for the devices, PCB, heat sink and other materials in proximity must be included.

8. Summary

RC thermal models are available for Nexperia products e.g. power MOSFETs and bipolar discretes on the Nexperia website. The models can be used in SPICE or other simulation tools to simulate the junction temperature rise in transient conditions. They provide a quick, simple and accurate method for application engineers to perform the thermal design.
9. Abbreviations

Table 4. Key to symbols used in equations

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>$P(t)$</td>
<td>power as a function of time</td>
</tr>
<tr>
<td>$Z_{th}(t)$</td>
<td>transient thermal impedance</td>
</tr>
<tr>
<td>$R_{th}$</td>
<td>thermal resistance</td>
</tr>
<tr>
<td>$\tau$</td>
<td>total time of heating pulse</td>
</tr>
<tr>
<td>$\tau_i$</td>
<td>thermal time constant</td>
</tr>
<tr>
<td>$R_i$</td>
<td>constituent thermal resistance element</td>
</tr>
<tr>
<td>$C_i$</td>
<td>constituent thermal capacitance element</td>
</tr>
<tr>
<td>$T_{mb}$</td>
<td>mounting base temperature of the device</td>
</tr>
<tr>
<td>$T_j$</td>
<td>junction temperature of the device</td>
</tr>
<tr>
<td>$T_{j(rise)}$</td>
<td>junction temperature rise in the device</td>
</tr>
<tr>
<td>$\Delta T$</td>
<td>change in temperature</td>
</tr>
<tr>
<td>$V_{ds}$</td>
<td>MOSFET drain to source voltage</td>
</tr>
<tr>
<td>$V_{gs}$</td>
<td>MOSFET gate to source voltage</td>
</tr>
<tr>
<td>$I_D$</td>
<td>MOSFET drain current</td>
</tr>
<tr>
<td>$V_{CE}$</td>
<td>BJT collector-emitter voltage</td>
</tr>
<tr>
<td>$I_C$</td>
<td>BJT collector current</td>
</tr>
<tr>
<td>$V_{BE}$</td>
<td>BJT base-emitter voltage</td>
</tr>
<tr>
<td>$I_B$</td>
<td>BJT base current</td>
</tr>
<tr>
<td>$V_F$</td>
<td>Diode forward voltage</td>
</tr>
<tr>
<td>$I_F$</td>
<td>Diode forward current</td>
</tr>
</tbody>
</table>

10. References

1. Application note AN11156 - “Using Power MOSFET $Z_{th}$ Curves”. Nexperia Semiconductors
2. Application note AN10273 - “Power MOSFET single-shot and repetitive avalanche ruggedness rating”. Nexperia Semiconductors
## 11. Revision history

<table>
<thead>
<tr>
<th>Revision number</th>
<th>Date</th>
<th>Description</th>
</tr>
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| 5.0             | 20210318   | Modifications:  
• Text updated to include reference to BJT as well as MOSFETs.                                                                           |
| 4.0             | 20200511   | Modifications:  
• Section 5 updated to include Cauer model netlist.                                                                                       |
| 3.0             | 20200504   | Modifications:  
• Updated to include Cauer models.                                                                                                         |
|                 |            | • Simulations have been updated using latest released technology T9 and replacing Foster models with Cauer models.                           |
|                 |            | • The format of this application note has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. |
| 2.0             | 20140519   | Second issue.  
Modifications:  
• Fig. 9 is updated.                                                                                                                        |
| 1.0             | 20140129   | first issue                                                                                                                                    |
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