

AN11261

Using RC Thermal Models

Rev. 2 — 19 May 2014

Application note

Document information

Info	Content
Keywords	RC thermal, SPICE, Models, Z_{th} , R_{th} , MOSFET, Power
Abstract	Analysis of the thermal performance of power semiconductors is necessary to efficiently and safely design any system utilizing such devices. This article presents a quick and inexpensive way to infer the thermal performance of power MOSFETs using a thermal electrical analogy.



Revision history

Rev	Date	Description
v.2	20140519	Second issue. Modifications: <ul style="list-style-type: none">• Figure 7 is updated.
v.1	20140129	first issue

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1. Introduction

Networks of resistors and capacitors can be used to create a Foster RC thermal model. The model represents the thermal performance of a MOSFET within a SPICE environment. The article provides some basic theory behind the principle, and how to implement Foster RC thermal models. For convenience, Foster RC thermal models are referred to as RC models in the rest of this paper. This application note describes several methods of using RC thermal models, including worked examples.

2. Thermal impedance

RC models are derived from the thermal impedance (Z_{th}) of a device (see [Figure 1](#)). This figure represents the thermal behavior of a device under transient power pulses. The Z_{th} can be generated by measuring the power losses as a result of applying a step function of varying time periods.

A device subjected to a power pulse of duration $> \sim 1$ s i.e. steady-state, has reached thermal equilibrium and the Z_{th} plateaus becomes the R_{th} . The Z_{th} illustrates the fact that materials have thermal inertia. Thermal inertia means that temperature does not change instantaneously. As a result, the device can handle greater power for shorter duration pulses.

The Z_{th} curves for repetitive pulses with different duty cycles, are also shown in [Figure 1](#). These curves represent the additional RMS temperature rise due to the dissipation of RMS power.

To assist this discussion, the thermal resistance junction to mounting base ($R_{th(j-mb)}$) from the BUK7Y7R6-40E data sheet, has been included in [Table 1](#). The Z_{th} in [Figure 1](#) also belongs to the BUK7Y7R6-40E data sheet.

Table 1. Steady state thermal impedance of BUK7YR6-40E

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 1	-	-	1.58	K/W

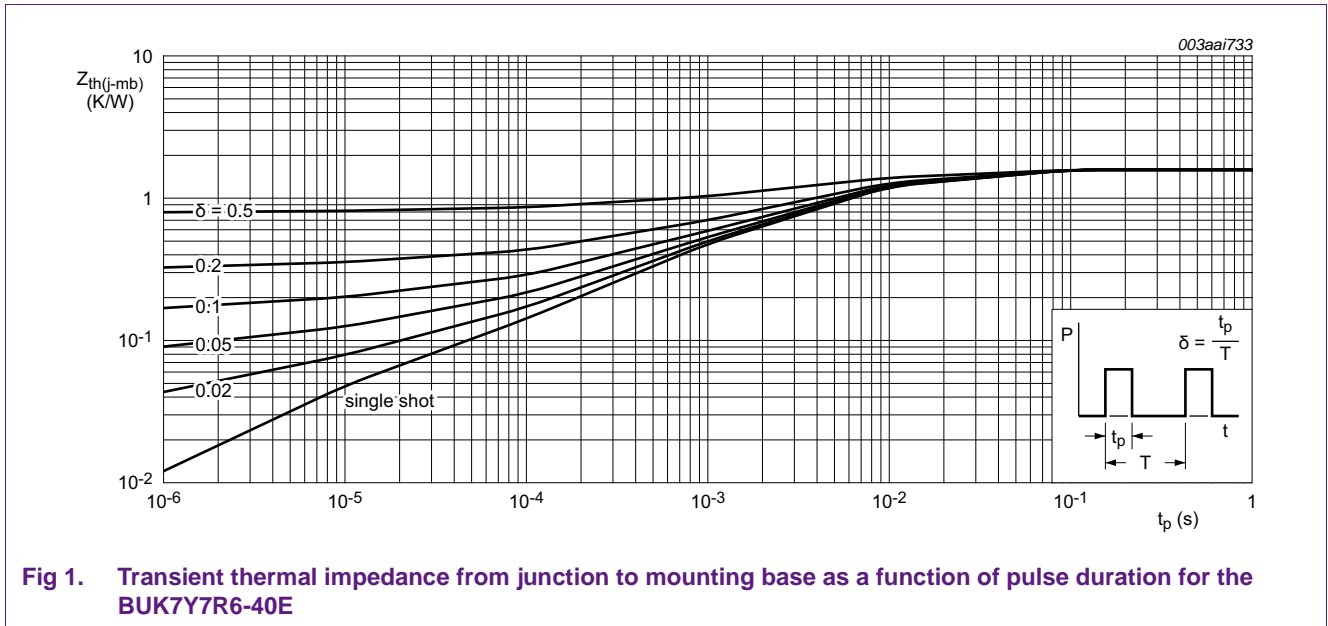


Fig 1. Transient thermal impedance from junction to mounting base as a function of pulse duration for the BUK7Y7R6-40E

3. Calculating junction temperature rise

To calculate the temperature rise within the junction of a power MOSFET, the power and duration of the pulse delivered to the device must be known. If the power pulse is a square, then the thermal impedance can be read from the Z_{th} chart. The product of this value with the power gives the temperature rise within the junction.

If constant power is applied to the device, the steady state thermal impedance can be used i.e. R_{th} . Again the temperature rise is the product of the power and the R_{th} .

For a transient pulse e.g. sinusoidal or pulsed, the temperature rise within the MOSFET junction becomes more difficult to calculate.

The mathematically correct way to calculate T_j is to apply the convolution integral. The calculation expresses both the power pulse and the Z_{th} curve as functions of time, and use the convolution integral to produce a temperature profile (see [Ref. 2](#)).

$$T_{j(rise)} = \int_0^{\tau} P_{(t)} \cdot \frac{d}{dt} Z_{th}(\tau - t) dt \tag{1}$$

However, this is difficult as the $Z_{th(\tau-t)}$ is not defined mathematically.

An alternative way is to approximate the waveforms into a series of rectangular pulse and apply superposition (see [Ref. 1](#)).

While relatively simple, applying superposition has its disadvantages. The more complex the waveform, the more superpositions that must be imposed to model the waveform accurately.

To represent Z_{th} as a function of time, draw upon the thermal electrical analogy and represent it as a series of RC charging equations or as an RC ladder. Z_{th} can then be represented in a SPICE environment for ease of calculation of the junction temperature.

4. Association between Thermal and Electrical parameters

The thermal electrical analogy is summarized in [Table 2](#). If the thermal resistance and capacitance of a semiconductor device is known, electrical resistances and capacitances can represent them respectively. Using current as power, and voltage as the temperature difference, any thermal network can be handled as an electrical network.

Table 2. Fundamental parameters

Type	Resistance	Potential	Energy	Capacitance
Electrical ($R = V/I$)	R = resistance (Ohms)	V = PD (Volts)	I = current (Amps)	C = capacitance (Farads)
Thermal ($R_{th} = K/W$)	R_{th} = thermal resistance (K/W)	K = temperature difference (Kelvin)	W = dissipated power (Watts)	C_{th} = thermal capacitance (thermal mass)

5. Foster RC thermal models

The RC thermal models discussed are Foster Models. These models are derived by semi-empirically fitting a curve to the Z_{th} , the result of which is a one-dimensional RC network ([Figure 2](#)). The R and C values in a Foster model do not correspond to geometrical locations on the physical device. Therefore, these values cannot be calculated from device material constants as can be in other modeling techniques. Finally, a Foster RC model cannot be divided or interconnected through, i.e. have the RC network of a heat sink connected.

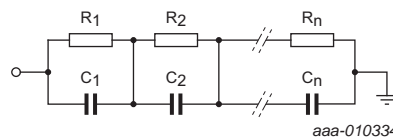


Fig 2. Foster RC thermal models

Foster RC models have the benefit of ease of expression of the thermal impedance Z_{th} as described at the end of [Section 2](#). For example, by measuring the heating or cooling curve and generating a Z_{th} curve, [Equation 2](#) can be applied to generate a fitted curve [Figure 3](#):

$$Z_{th(t)} = \sum_{i=1}^n R_i * \left[1 - \exp\left(-\frac{t}{\tau_i}\right) \right] \tag{2}$$

Where: $\tau_i = R_i * C_i$ (3)

The model parameters R_i and C_i are the thermal resistances and capacitances that build up the thermal model depicted in [Figure 2](#). The parameters in the analytical expression can be optimized until the time response matches the transient system response by applying a least square fit algorithm. It allows application engineers to perform fast calculations of the transient response of a package to complex power profiles.

The individual expression, “i”, also draws parallels with the electrical capacitor charging equation. [Figure 3](#) shows how the individual R_i and C_i combinations, sum to make the Z_{th} curve.

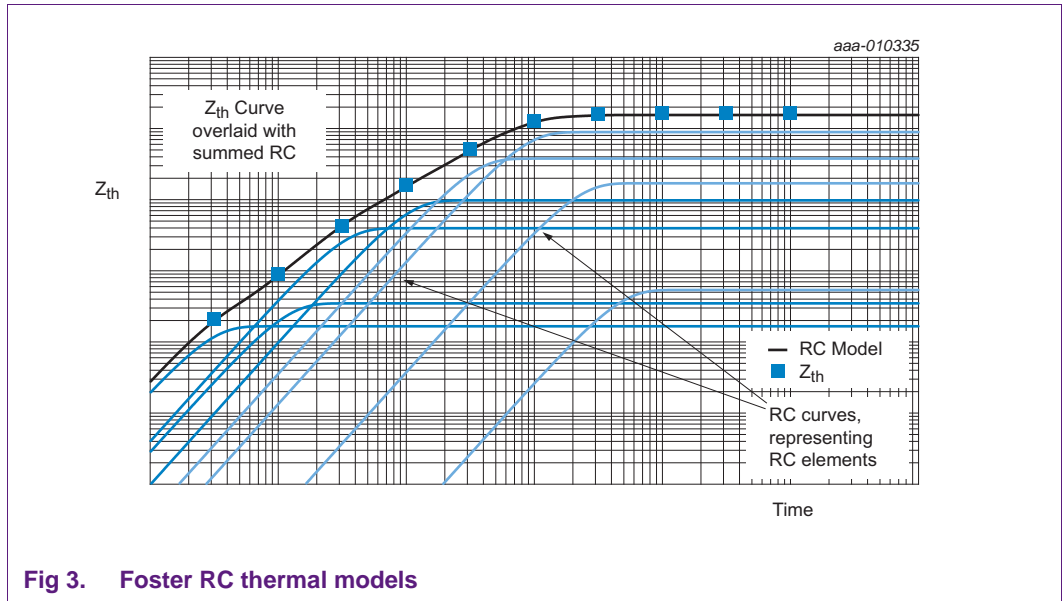


Fig 3. Foster RC thermal models

NXP provides Foster RC models for most of their Automotive Power MOSFET products. The models can be found under the tab “Documentation” > “BUK7Y7R6-40E_RC_Thermal_Model” as demonstrated in [Figure 4](#).

BUK7Y7R6-40E
N-channel 40 V, 7.6 mΩ standard level MOSFET in LFPAK56

Overview Parametrics Package / Packing Quality **Documentation** Ordering Design support Show all

Documentation for this product

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File name	Title	Type
75017357	NXP's Power MOSFET Selection Guide 2013: Smaller, faster, cooler	Selection guide
AN10273	Power MOSFET single-shot and repetitive avalanche ruggedness rating	Application note
AN10874	LFPAK MOSFET thermal design guide	Application note
AN11113	LFPAK MOSFET thermal design guide - Part 2	Application note
AN11113_ZH	LFPAK MOSFET thermal design guide - Part 2	Application note
AN11156	Using Power MOSFET Zth Curves	Application note
AN11158	Understanding power MOSFET data sheet parameters	Application note
AN11158_ZH	Understanding power MOSFET data sheet parameters	Application note
AN11160	Designing RC Snubbers	Application note
AN11243	Failure signature of Electrical Overstress on Power MOSFETs	Application note
BUK7Y7R6-40E	N-channel TrenchMOS standard level FET	Data sheet
BUK7Y7R6-40E	BUK7Y7R6-40E Spice model	SPICE model
BUK7Y7R6-40E	BUK7Y7R6-40E Thermal model	Thermal model
BUK7Y7R6-40E_RC_Thermal_Model	BUK7Y7R6-40E Thermal design model	Thermal design

aaa-010336

Fig 4. NXP RC thermal model documentation

6. Thermal simulation examples

6.1 Example 1

RC thermal models are generated from the Z_{th} curve. This example shows how to work back from an RC model and plot a Z_{th} curve within a SPICE simulator. It allows for greater ease when trying to read values of the Z_{th} curve from the data sheet.

This and subsequent examples use the RC thermal model of BUK7Y7R6-40E. T_{mb} represents the mounting base temperature. It is treated as an isothermal and for this example it is set as 0 °C. A single shot pulse of 1 W power is dissipated in the MOSFET. Referring to [Figure 5](#); for a single shot pulse, the time period between pulses is infinite and therefore the duty cycle $\delta = 0$. Then the junction temperature T_j represents the transient thermal impedance Z_{th} .

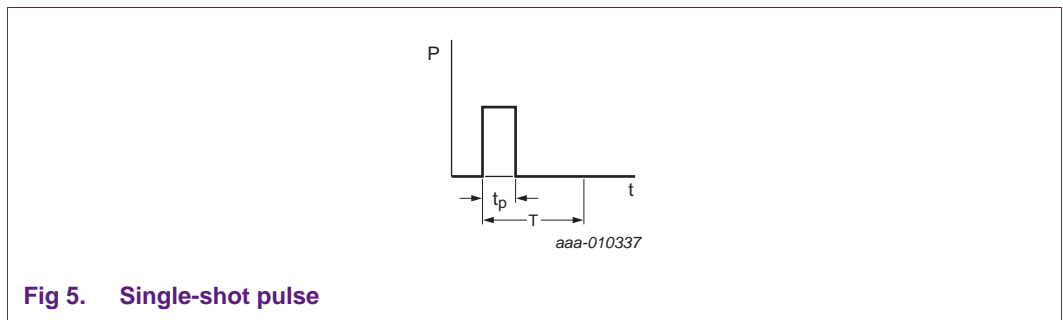


Fig 5. Single-shot pulse

[Equation 4](#) and [Equation 5](#) demonstrate why T_j is used to represent the transient thermal impedance Z_{th} in this simulation.

$$T_{mb} = 0 \text{ } ^\circ\text{C}$$

$$P = 1 \text{ W}$$

$$T_j = T_{mb} + \Delta T = 0 \text{ } ^\circ\text{C} + \Delta T = \Delta T \tag{4}$$

$$\Delta T = P * Z_{th} = 1 \text{ W} * Z_{th} \tag{5}$$

[Equation 5](#) demonstrates that with $P = 1 \text{ W}$, the magnitude of Z_{th} equates to ΔT .

The following steps are used to set up and run simulations:

1. set up the RC thermal model of BUK7Y7R6-40E in SPICE as shown in [Figure 6](#)
2. set the value of voltage source V_{mb} to 0, which is the value of T_{mb}
3. set the value of the current source I1 to 1
4. create a simulation profile and set the run time to 1 s
5. run the simulation
6. Plot the voltage at node T_j

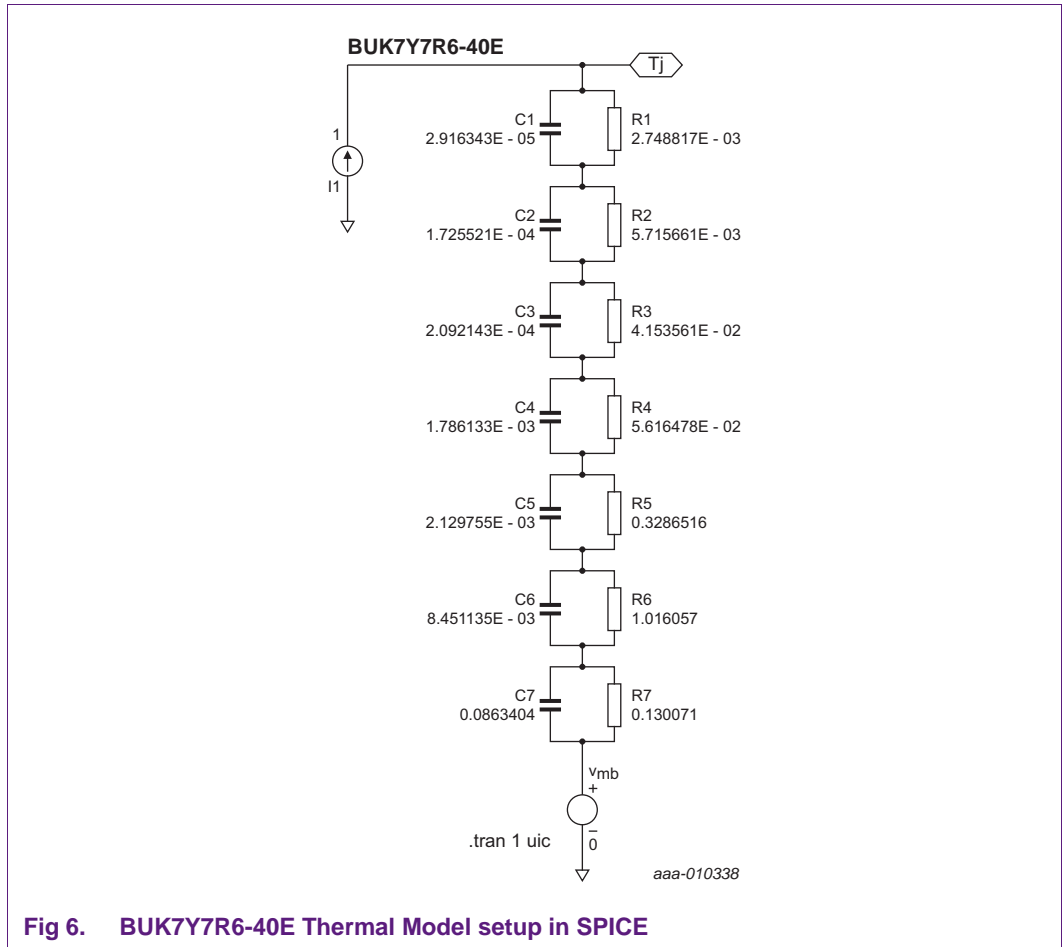


Fig 6. BUK7Y7R6-40E Thermal Model setup in SPICE

The simulation result in [Figure 7](#) shows the junction temperature (voltage at T_j) which is also the thermal impedance of BUK7Y7R6-40E. The values of Z_{th} at different times can be read using the cursors on this plot within SPICE.

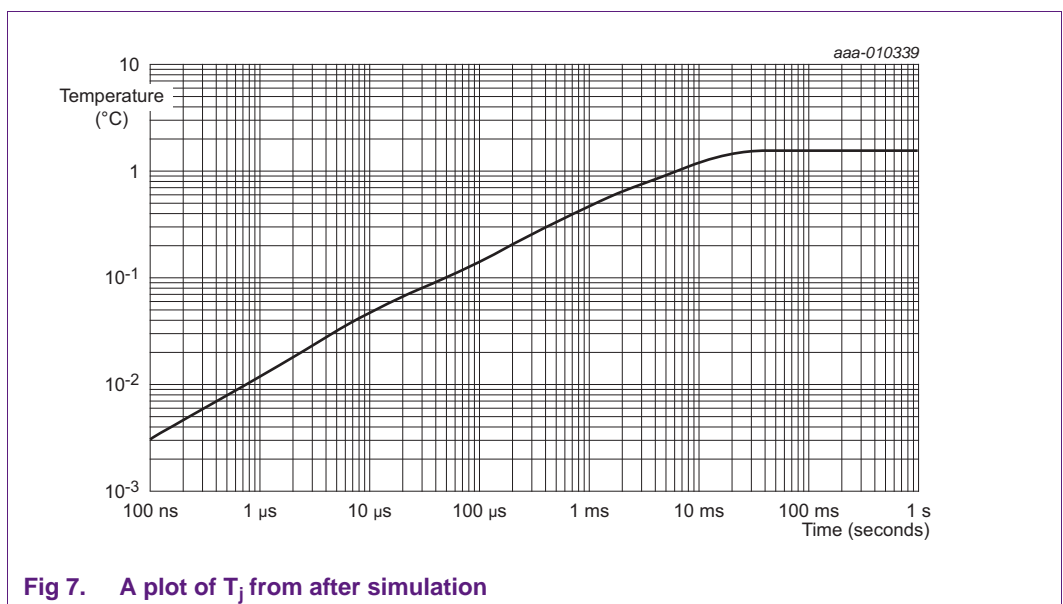


Fig 7. A plot of T_j from after simulation

The value of the current source in this example is set to 1 A to represent 1 W dissipating through the device. It can be easily changed to represent any value of power. The simulation command can be changed for any duration to represent a range of square power pulses.

6.2 Example 2

Another method of generating the power profile, is to use measurements from the actual circuit. This information is presented to the SPICE simulation in the form of a comma-separated value (CSV) file giving pairs of time/power values. It can be generated either as a summary of observations showing the points of change or from an oscilloscope waveform capture.

Two further methods of generating a power profile are discussed. One method is using a PWL file. The other is to generate the power from an MOSFET electrical circuit modeled in SPICE. The former is outlined first.

A source within a SPICE simulator can use a PWL file as an input. The contents of a typical PWL file is shown in [Table 3](#) It can list the current, voltage or in this example, power over time. These files can be generated by typing values into a spreadsheet editor and saving as a .csv file, or alternatively exporting waveforms from an oscilloscope. The actual file itself should not contain any column headings.

To implement this procedure within a SPICE environment, follow the same steps as described in [Section 6.1 “Example 1”](#), but with the exceptions:

- 1) Set the property value of the current source to read from a PWL FILE and point it to a .csv file for example: C:\Pulse file\filepulse.csv, which contains the power profile listed in [Table 3](#).
- 2) Set the mounting base T_{mb} (V_{mb}) to 125.
- 3) Set the simulation run time to 3.5 s

Table 3. Data example for use in a PWL file

Time (seconds)	Power (Watts)
0	0
0.000001	30
0.015	30
0.015000001	6
1.1	6
1.100001	6
1.100002	20
1.5	20
1.500002	20
1.500003	0
1.6	0
1.600001	20
1.615	20
1.615001	6

Table 3. Data example for use in a PWL file ...continued

Time (seconds)	Power (Watts)
2.9	6
2.900001	0
3	0
3.000001	30
3.015	30
3.015001	6

The simulation result is shown in Figure 9. The junction temperature and thermal impedance values labeled in Figure 9, demonstrate that the Z_{th} value at 3 ms, and R_{th} value, are in line with Figure 10. It represents the thermal impedance waveform shown in the BUK7Y7R6-40E data sheet.

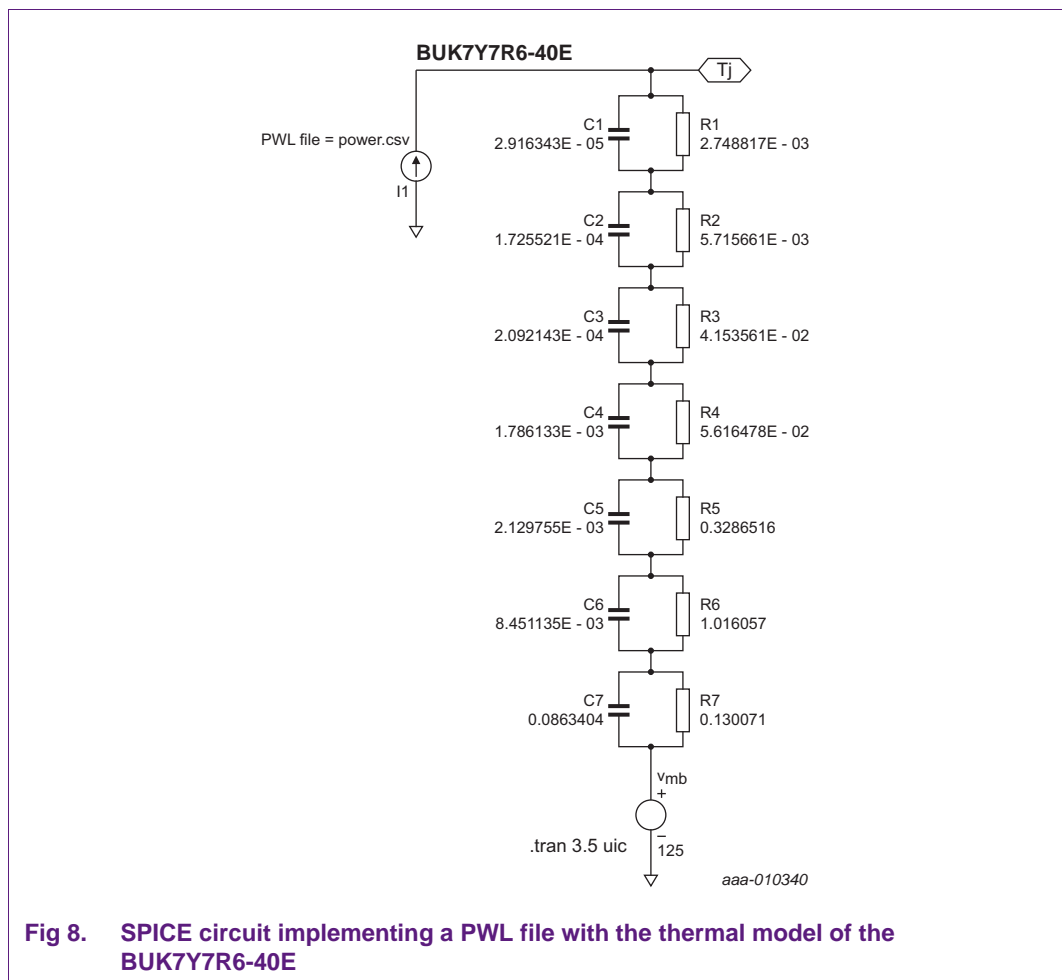
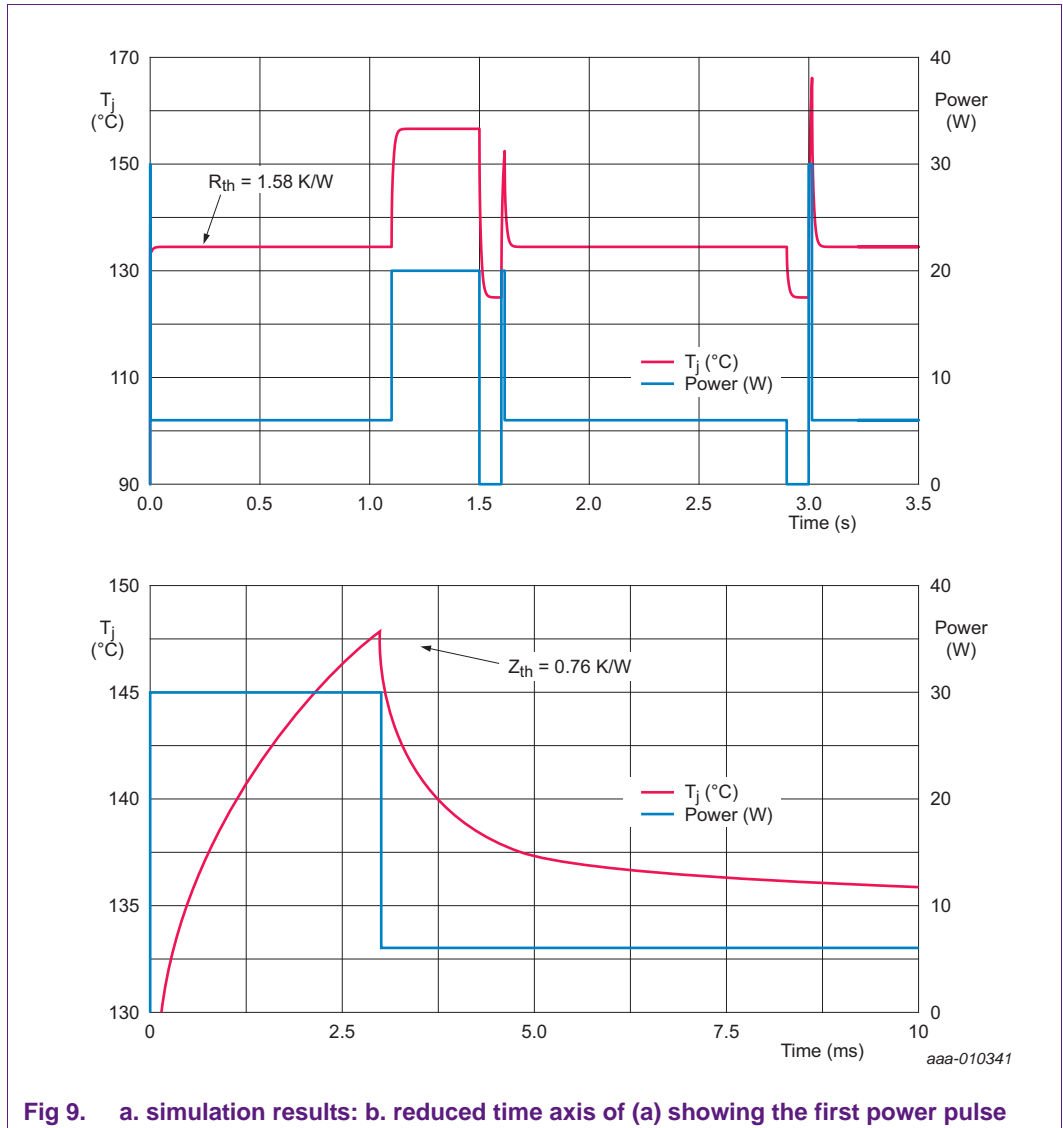
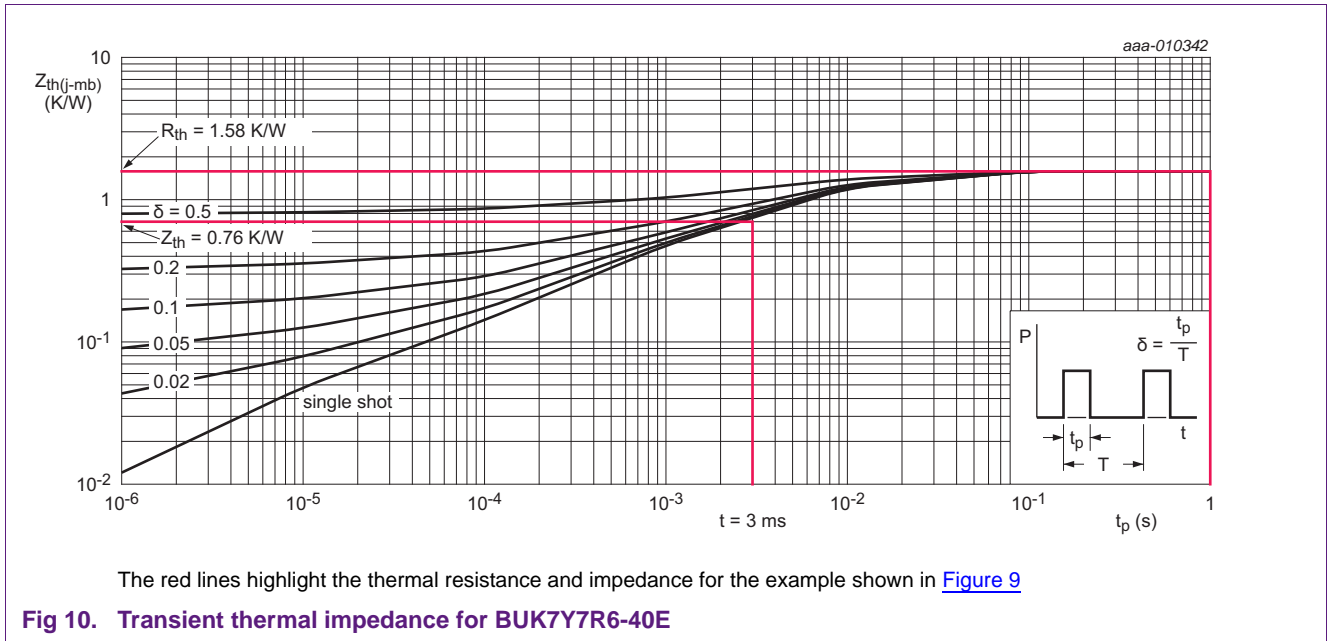


Fig 8. SPICE circuit implementing a PWL file with the thermal model of the BUK7Y7R6-40E





6.3 Example 3

The aim of this example is to show how to perform thermal simulation using the power profile generated from a MOSFET circuit.

Following the steps in [Section 6.1](#), set up the thermal model of BUK7Y7R6-40E, and set the mounting base temperature to 85° C.

To set the power value in the current source, construct a MOSFET electrical circuit as provided in [Figure 11](#). The power supply is 14 V and the load is a 0.1 Ω resistance. The gate drive supply is assigned a value of 10 V. It is set to run for 50 cycles with a 1 ms period and a 50 % duty cycle.

The power dissipated in the MOSFET can be calculated from [Equation 6](#) or for greater accuracy; the gate current can be included into the calculation to give [Equation 7](#):

$$P = V_{ds} * I_d \tag{6}$$

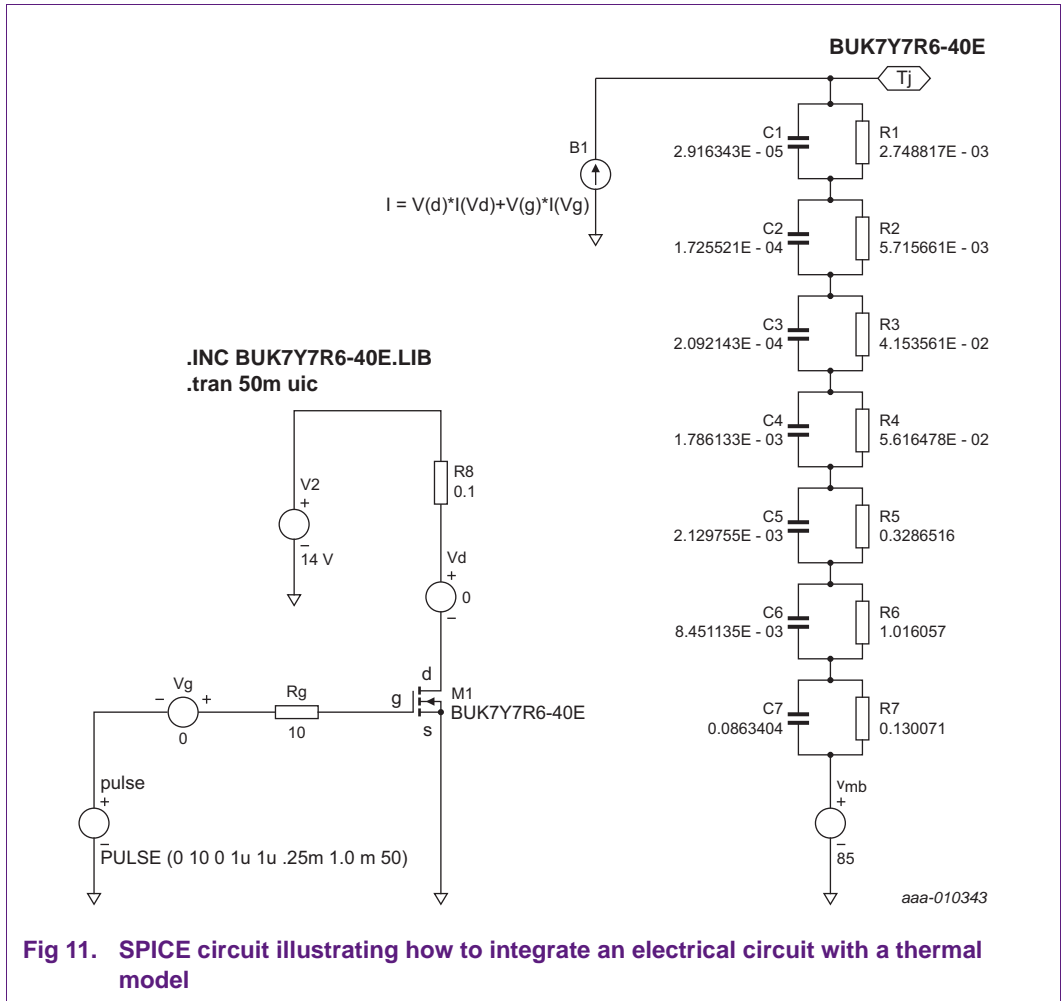
To improve accuracy:

$$P = V_{ds} * I_d + V_{gs} * I_g \tag{7}$$

The current source into the thermal model can now be defined as:

$$I = V_{(d)} * I(V_d) + V_{(g)} * I(V_g) \tag{8}$$

[Figure 11](#) demonstrates the link between the electrical circuit and the thermal model circuit.



The resultant plot of T_j is shown in [Figure 12](#). The maximum temperature of the junction can once again be calculated from data sheet values by following the steps outlined in [Ref. 1](#).

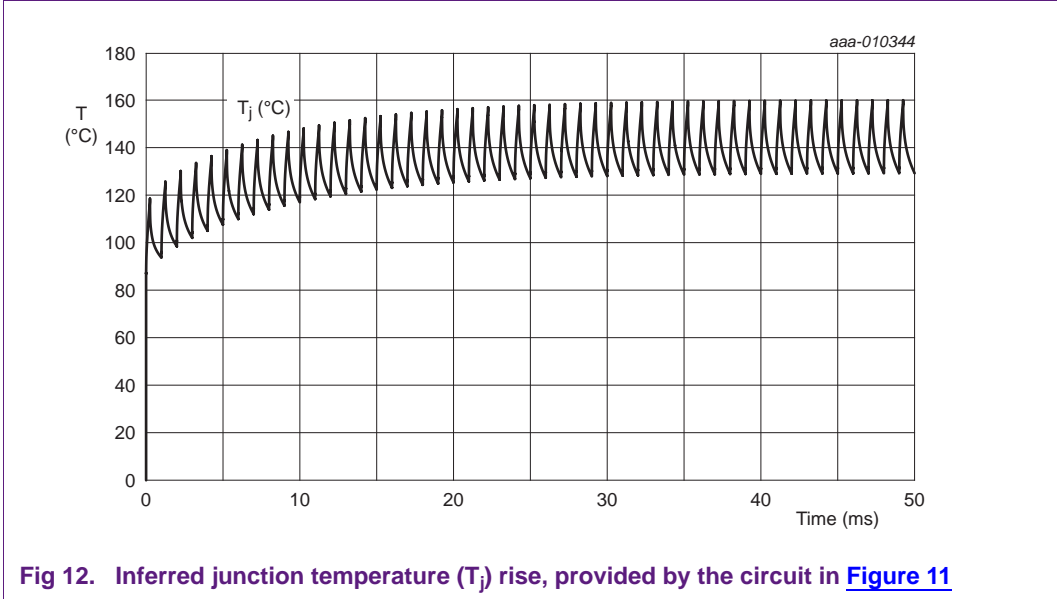


Fig 12. Inferred junction temperature (T_j) rise, provided by the circuit in [Figure 11](#)

7. Discussions

RC thermal models are not perfect. The physical materials used to build Semiconductors have temperature-dependent characteristics. These characteristics mean that thermal resistance is also a temperature-dependent parameter. Whereas in ohm's law, the ohmic resistance is constant and independent of the voltage. So the correspondence between electrical and thermal parameters is not perfectly symmetrical but gives a good basis for fundamental thermal simulations.

In power electronic systems, the thermal resistance of silicon amounts to 2 % to 5 % of the total resistance. The error resulting from the temperature dependence is relatively small and can be ignored for most cases. To obtain a more accurate analysis, replace the passive resistors in the RC model with voltage-dependent resistors. In these resistors, the change in temperature can correspond to change in voltage.

A further limitation of the models presented is that the mounting base temperature of the MOSFET T_{mb} , is set as an isothermal. This is rarely the case in real applications where a rise in the mounting base temperature must be considered. This rise is determined by calculating the temperature rise due to the average power dissipation (i.e. the heat flow) from the mounting base through to ambient. It means that the models are of limited use for pulses greater than 1 s, where heat begins to flow into the environment of the MOSFET. In this situation, the thermal model for the MOSFETs, PCB, heat sink and other materials in proximity must be included. However these components cannot be connected to the Foster RC models.

8. Summary

RC thermal models are available for NXP power MOSFETs on the NXP website. The models can be used in SPICE or other simulation tools to simulate the junction temperature rise in transient conditions. They provide a quick, simple and accurate method for application engineers to perform the thermal design.

9. Abbreviations

Table 4. Key to symbols used in equations

Symbol	Description
$P_{(t)}$	power as a function of time
$Z_{th(t)}$	transient thermal impedance
R_{th}	thermal resistance
τ	total time of heating pulse
τ_i	thermal time constant
R_i	constituent thermal resistance element
C_i	constituent thermal capacitance element
T_{mb}	mounting base temperature of the MOSFET
T_j	junction temperature of the MOSFET
$T_{j(rise)}$	junction temperature rise in the MOSFET
ΔT	change in temperature
V_{ds}	drain to source voltage of the MOSFET
V_{gs}	gate to source voltage of the MOSFET
I_d	drain current

10. References

- [1] Application note AN11156 - "Using Power MOSFET Z_{th} Curves". NXP Semiconductors
- [2] Application note AN10273 - "Power MOSFET single-shot and repetitive avalanche ruggedness rating". NXP Semiconductors
- [3] Combination of Thermal Subsystems Modeled by Rapid Circuit Transformation. Y.C. Gerstenmaier, W. Kiffe, and G. Wachutka

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Date of release: 19 May 2014

Document identifier: AN11261