

## Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use <http://www.nexperia.com>

Instead of [sales.addresses@www.nxp.com](mailto:sales.addresses@www.nxp.com) or [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com), use [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com) (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

# AN11076

## Thermal behavior of small-signal discretes on multilayer PCBs

Rev. 1 — 11 July 2011

Application note

### Document information

Info	Content
<b>Keywords</b>	Low VCEsat, BISS, thermal resistance ( $R_{th}$ ), thermal impedance ( $Z_{th}$ ), total power dissipation ( $P_{tot}$ )
<b>Abstract</b>	This application note illustrates how to improve the power dissipation of discrete components by using multilayer PCBs. It focuses on the impact of using larger copper areas to improve the thermal behavior of applications.



## Revision history

Rev	Date	Description
1	20110711	Initial version

## Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 1. Introduction

In today’s data sheets thermal characteristics are measured on a standard FR4 single copper layer Printed-Circuit Board (PCB). Customers should be able to compare devices easily just by evaluating standard data sheet parameters. In reality, design engineers cannot only rely on data sheet parameters and must consider the individual design requirements.

## 2. Thermal resistance

### 2.1 Key parameters

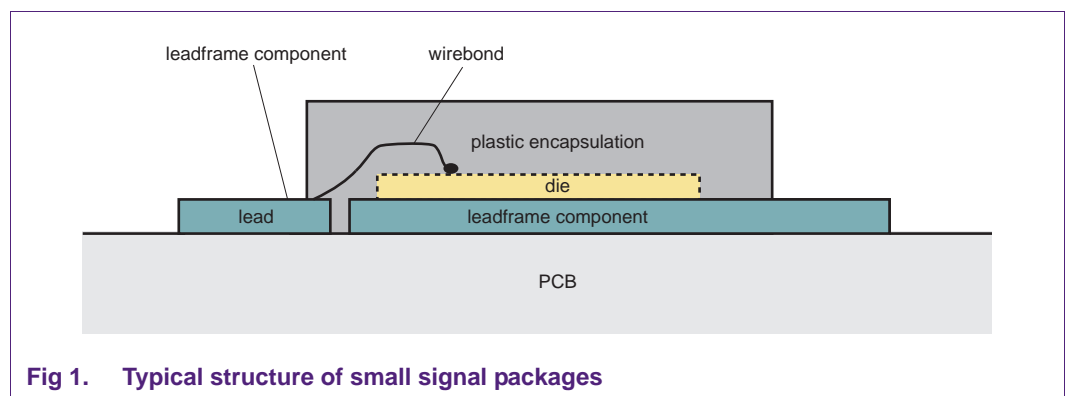
The main thermal parameters for semiconductor device are junction temperature ( $T_j$ ) and thermal resistance ( $R_{th}$ ). Thermal resistance depends on the environment surrounding a semiconductor device. In data sheets, design engineers can find different thermal resistances (see [Section 2.1.1](#) and [2.1.2](#)).

Thermal resistance of semiconductor devices is defined in general as:

$$R_{thx} = \frac{T_j - T_x}{P_{tot}} \tag{1}$$

Where  $R_{thx}$  = thermal resistance from the device junction to specific environment [K/W];  
 $T_j$  = device junction temperature in steady state [°C];  
 $T_x$  = reference temperature of the specific environment [°C] and  
 $P_{tot}$  = maximum power dissipation of the semiconductor device [W].

Thermal data is not comparable, unless a semiconductor supplier provides all test conditions. NXP Semiconductors provides them. They are often marked with a note at the end of an abstract or table, in the data sheet.



**Fig 1. Typical structure of small signal packages**

[Figure 1](#) shows the typical structure of small signal devices. The heat is generated at the junction and must be transferred by the leadframe to the outside of the package. Thermal conduction between the die and the leadframe and between the leadframe and the PCB allow this transfer. The heat transfer between PCB and air can be done by convection and/or radiation.

### 2.1.1 Thermal resistance from junction to solder point $R_{th(j-sp)}$

This parameter depends on the component. The size of the die, the material of the leadframe and the mold compound influence the  $R_{th(j-sp)}$ . The solder point is defined as the mounting point where the device would be normally soldered to the PCB. It is a conduction path only.

### 2.1.2 Thermal resistance from junction to ambient $R_{th(j-a)}$

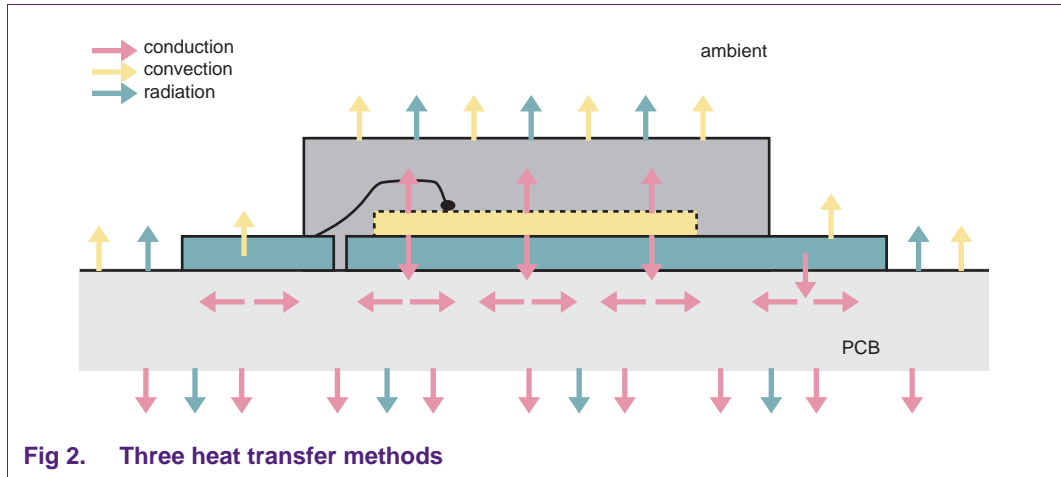
This parameter describes the thermal resistance from the junction (die) to the ambient. It is a single thermal resistance value including all effects of possible series and parallel paths from the junction to the ambient. Typically, it includes all the heat transfer methods of conduction and convection, from the surface of the package and via the PCB.

$R_{th(j-a)}$  is only valid for a specific PCB and not for:

- PCBs of different size, shape or layer stack to the test specification
- Several devices mounted on one PCB
- Operation within a housing, which influences the convection
- Forced cooling, for example, by cooling fan

### 3. Heat transfer mechanism

Up to three different transfer methods can be used to transfer heat from the die to the ambient.



#### 3.1 Thermal conduction

Conduction is a heat transfer in a medium due to a temperature change. For small-signal discrete components the heat transfer between the die and the leadframe and then the leadframe and the PCB is done by conduction.

#### 3.2 Thermal convection

Convection is a heat transfer from a body due to the movement of a medium, which is in contact with the surface of the body. In our case, it is the transfer of heat from the PCB surface and the ambient air. Due to the poor thermal conductivity of the plastic package, the main path for convection is the PCB/air interface.

#### 3.3 Thermal radiation

Radiation is a heat transfer by emitting heat from a hot body, which will be absorbed by a cooler one. For example PCB surface and surrounding objects such as the side panel of the housing.

### 4. Thermal measurement results

In PCB design, the numbers of variables are significant. The thermal resistance depends on board size, thickness, cooling pad area and ambient temperature.

Therefore, NXP Semiconductors has developed specific  $R_{th}$ -PCBs which are according to the JEDEC standards. It helps designers to compare easily relevant thermal parameters from different small-signal discrete vendors. Unfortunately, most applications are not developed on single layer FR4 PCBs. To get a better view of customer requirements, NXP Semiconductors set up a four-layer PCB. All PCBs differ by the top layer layout. Layers 2 to 4 consist of pure copper layers with a dimension of approximately 32 x 42 mm (see Figure 4). The top layer design was made on standard footprint and with a 1 cm<sup>2</sup> cooling pad area for each package.

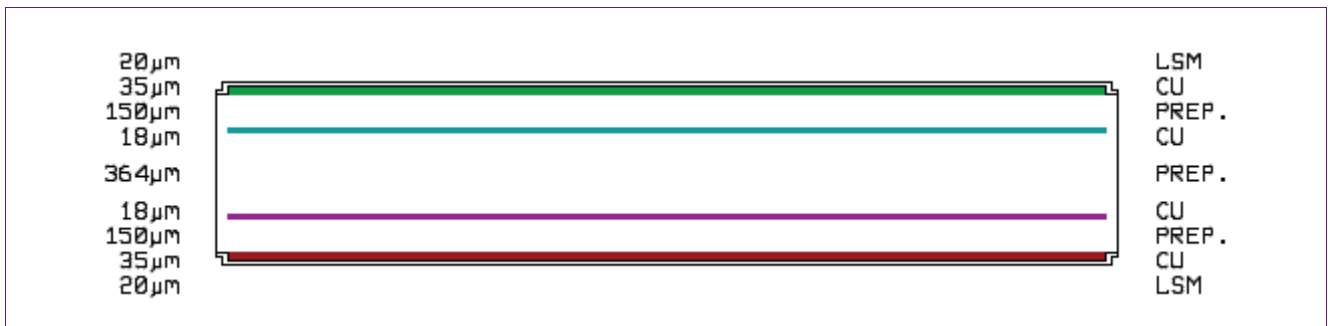


Fig 3. Layer stack of modified  $R_{th}$ -PCBs

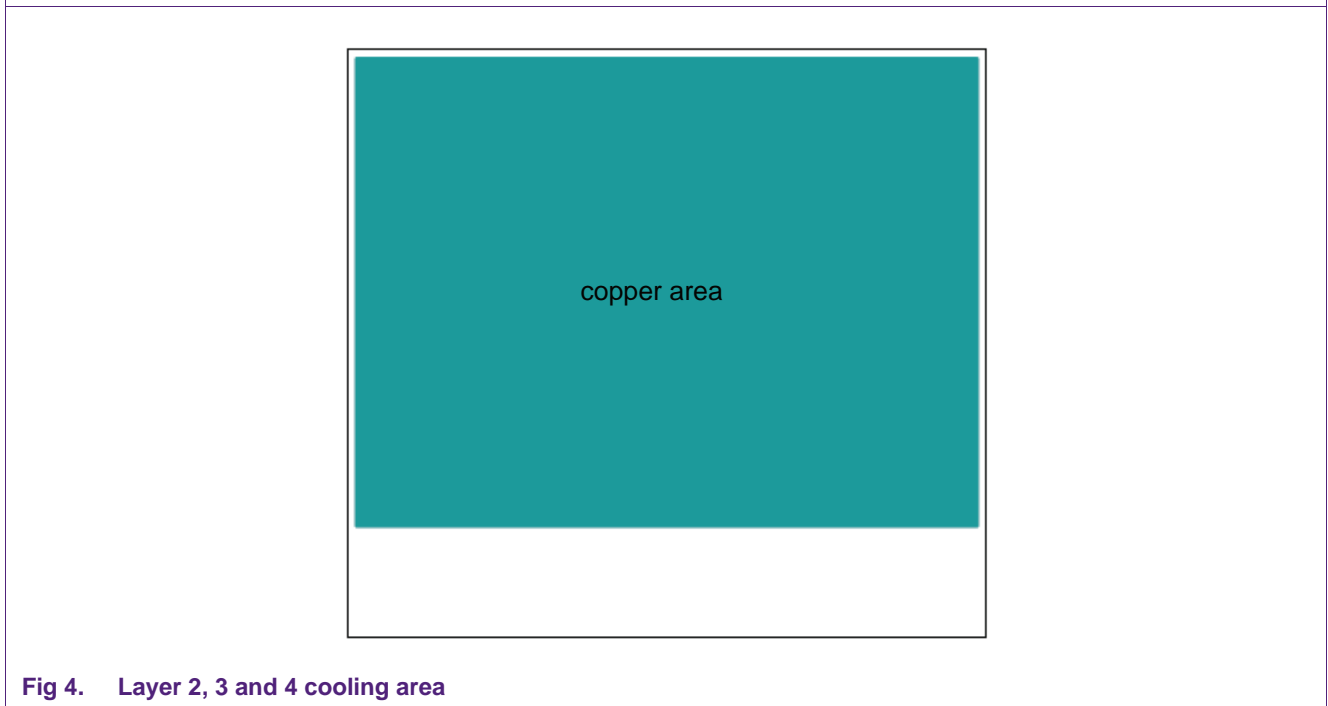


Fig 4. Layer 2, 3 and 4 cooling area

4.1 SOT457

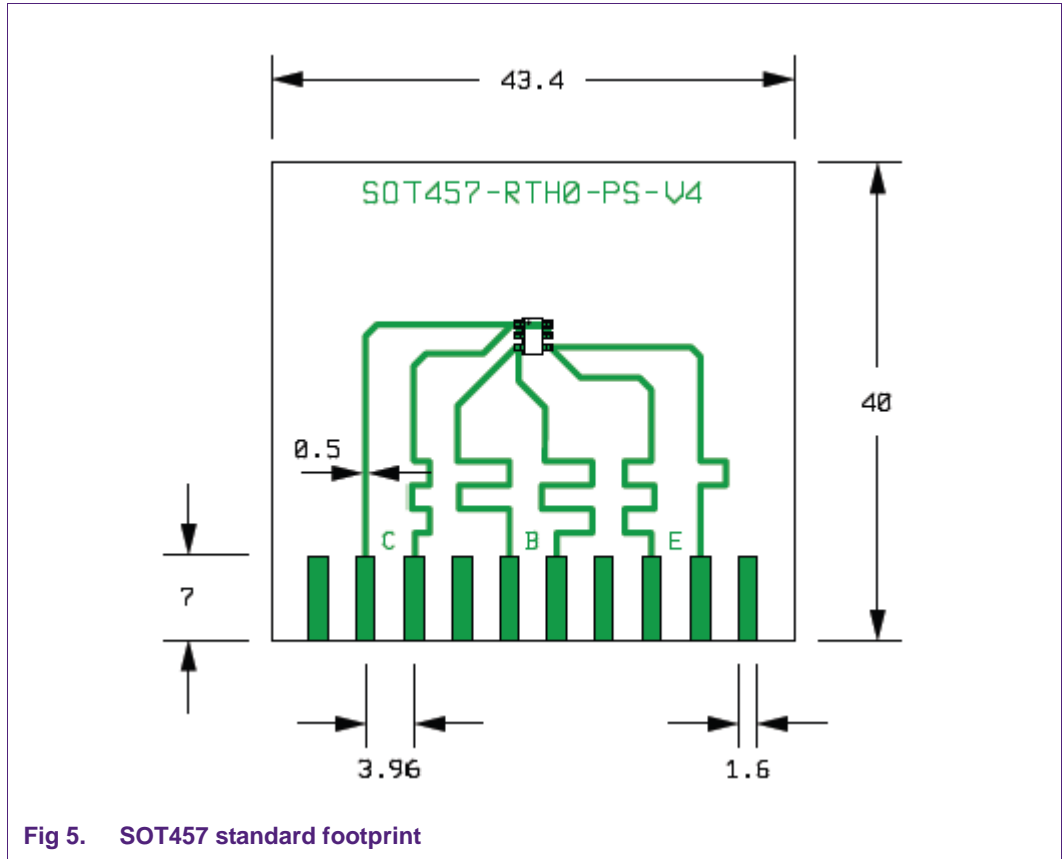


Fig 5. SOT457 standard footprint



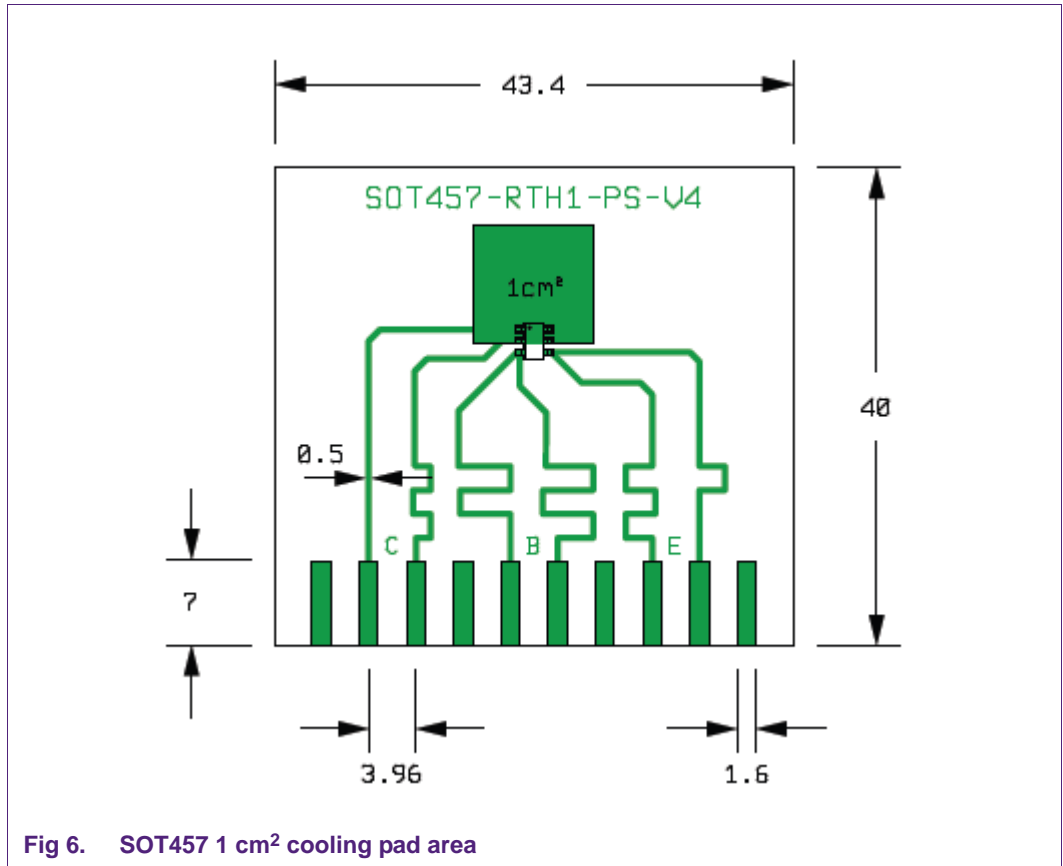


Table 1. PBSS5350D in SOT457; typical values

Sample	Standard footprint		1 cm <sup>2</sup> cooling pad	
	R <sub>th</sub> (K/W)	P <sub>tot</sub> (mW)	R <sub>th</sub> (K/W)	P <sub>tot</sub> (mW)
1	181	689	141	889
2	181	689	141	889
3	181	689	141	889
Average	181	689	141	889
+15 % safety margin	208	600	162	770
Single layer FR4	275	450	208	600

4.2 SOT89

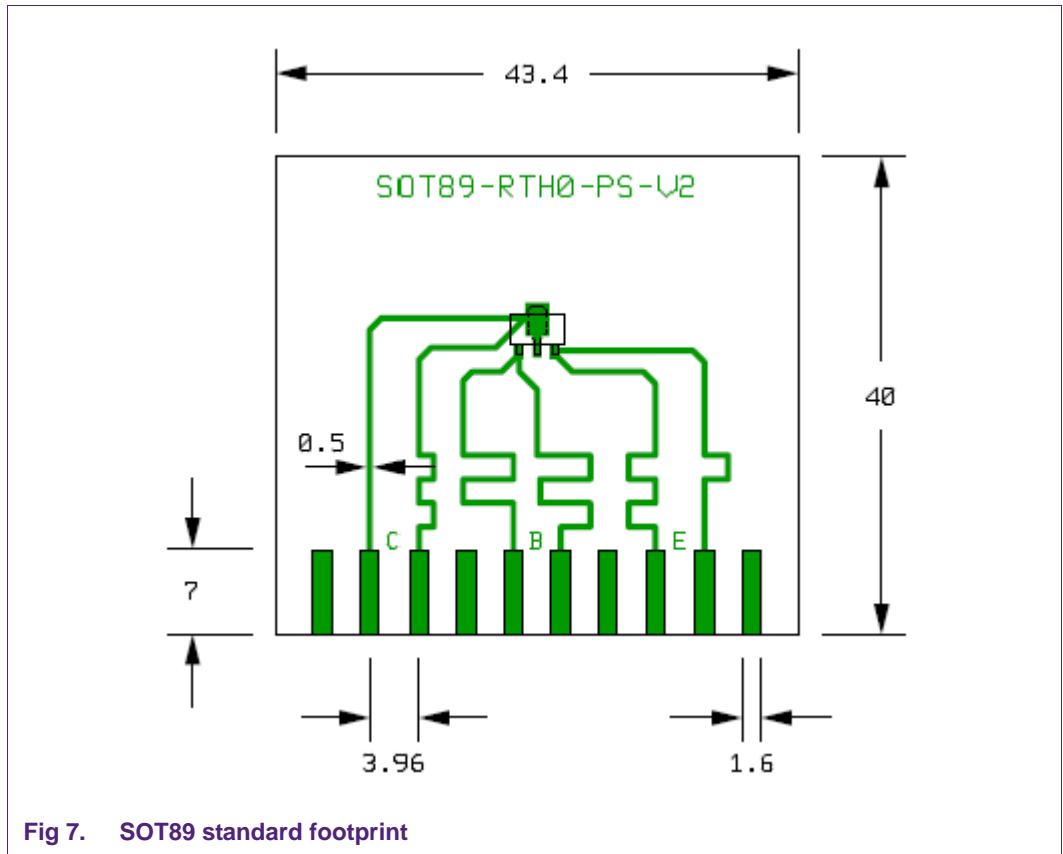


Fig 7. SOT89 standard footprint

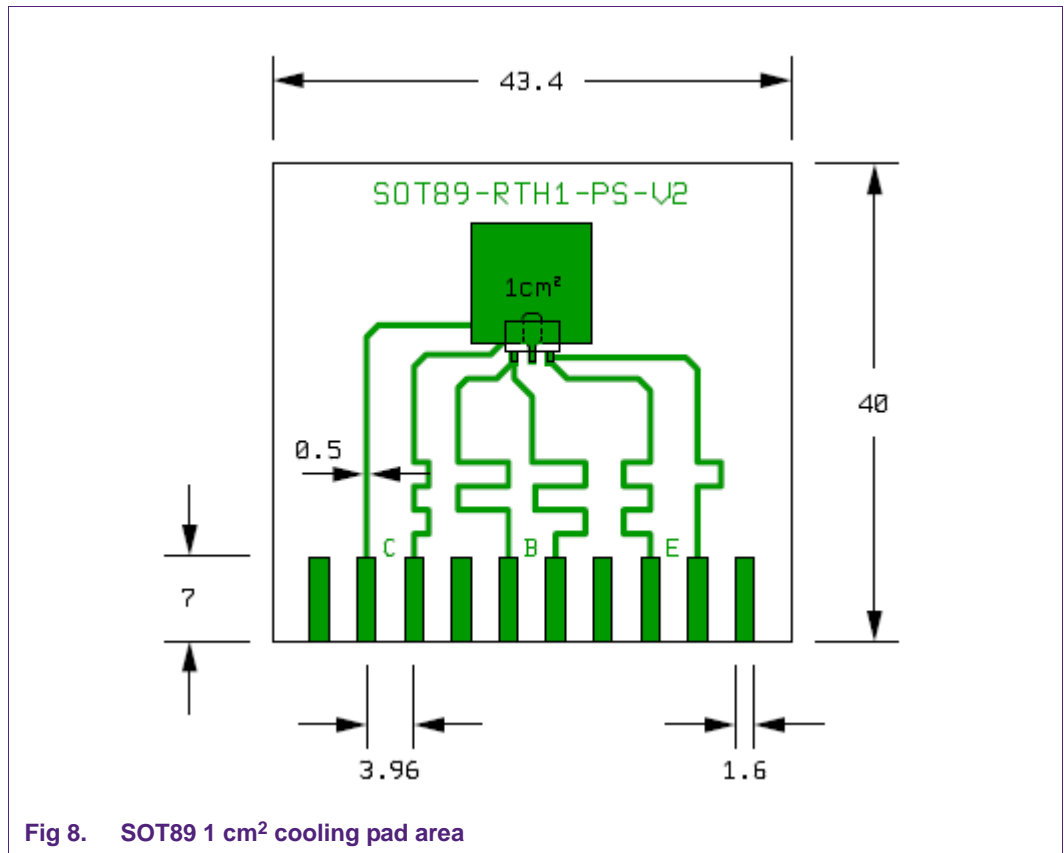
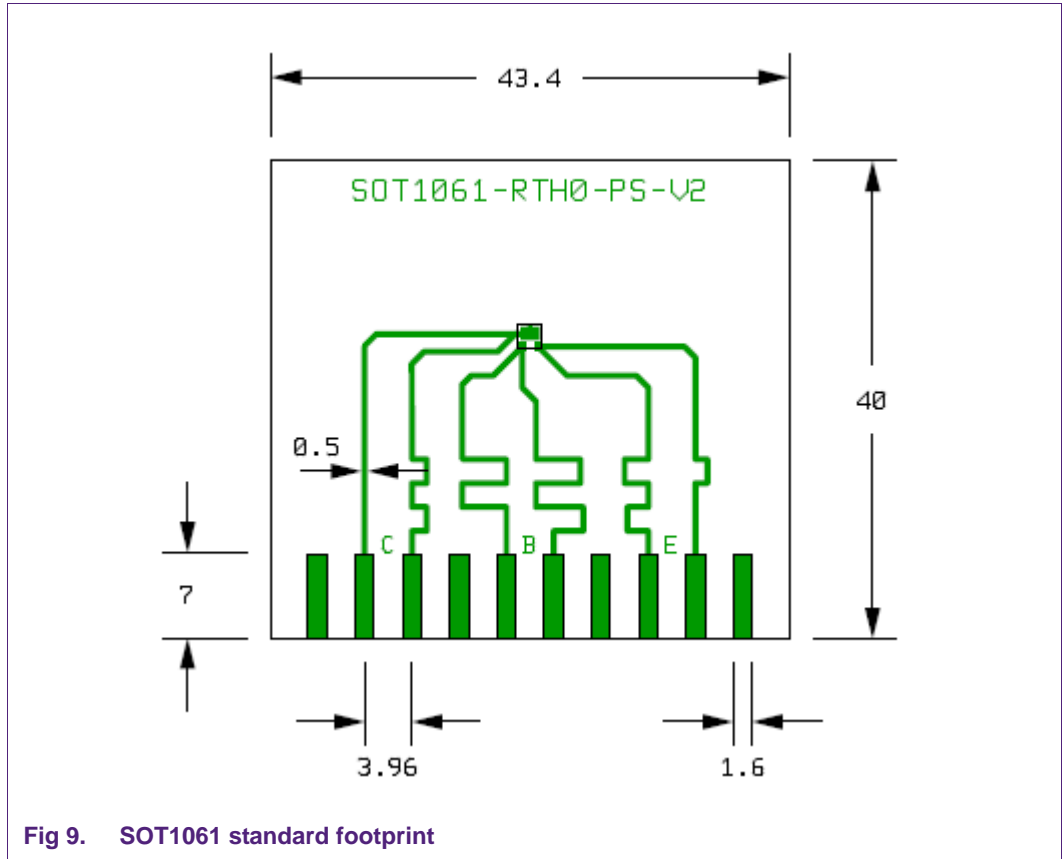


Table 2. PBSS5330X in SOT89; typical values

Sample	Standard footprint		1 cm <sup>2</sup> cooling pad	
	R <sub>th</sub> (K/W)	P <sub>tot</sub> (mW)	R <sub>th</sub> (K/W)	P <sub>tot</sub> (mW)
1	79	1582	47	2660
2	77	1623	42	2976
3	72	1736	43	2907
Average	76	1647	44	2848
+15 % safety margin	88	1420	51	2450
Single layer FR4	225	550	125	1000

4.3 SOT1061



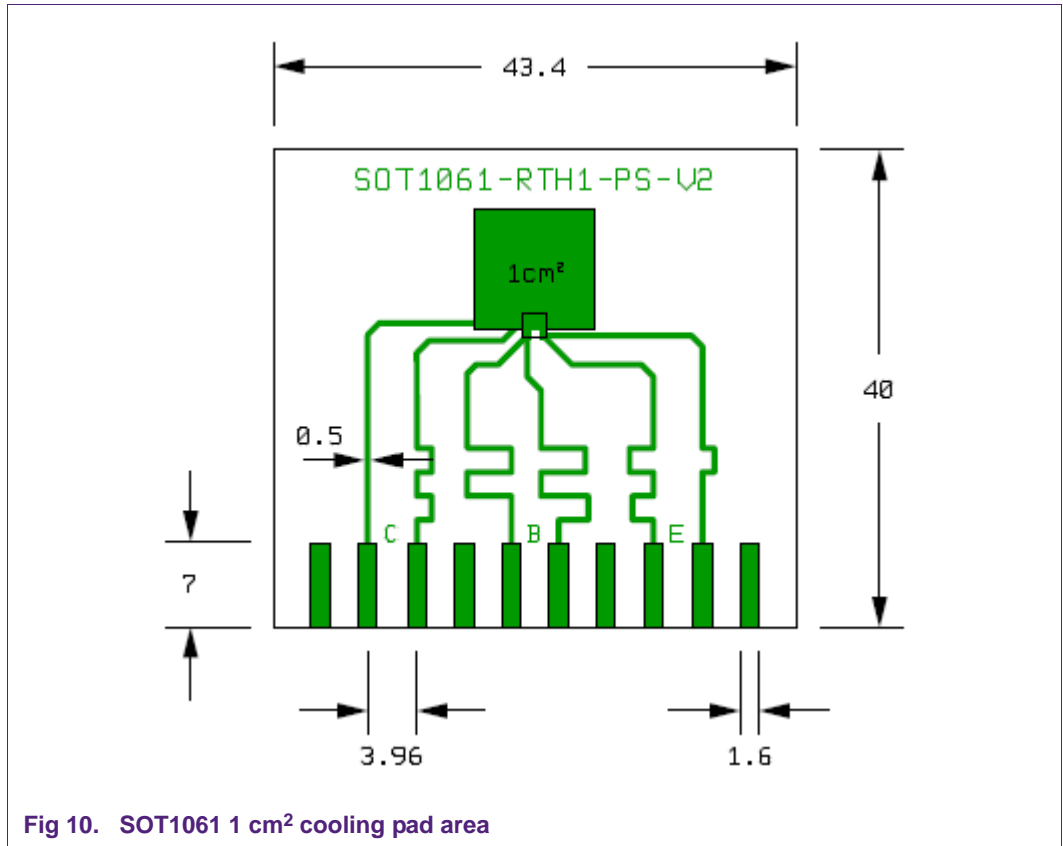


Fig 10. SOT1061 1 cm<sup>2</sup> cooling pad area

Table 3. PBSS5330PA in SOT1061; typical values

Sample	Standard footprint		1 cm <sup>2</sup> cooling pad	
	R <sub>th</sub> (K/W)	P <sub>tot</sub> (mW)	R <sub>th</sub> (K/W)	P <sub>tot</sub> (mW)
1	114	1096	50	2500
2	113	1106	51	2541
3	111	1126	52	2404
Average	112	1116	51	2541
+15 % safety margin	129	970	59	2110
Single layer FR4	250	500	125	1000

4.4 SOT1118

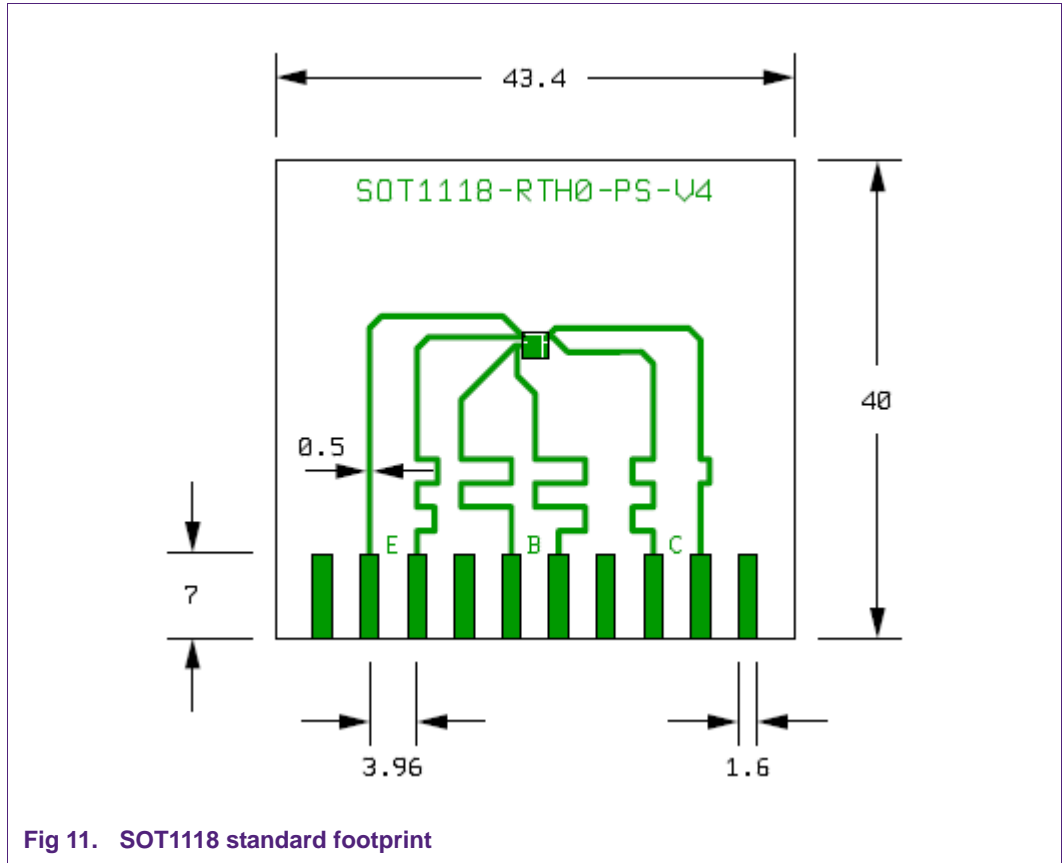


Fig 11. SOT1118 standard footprint

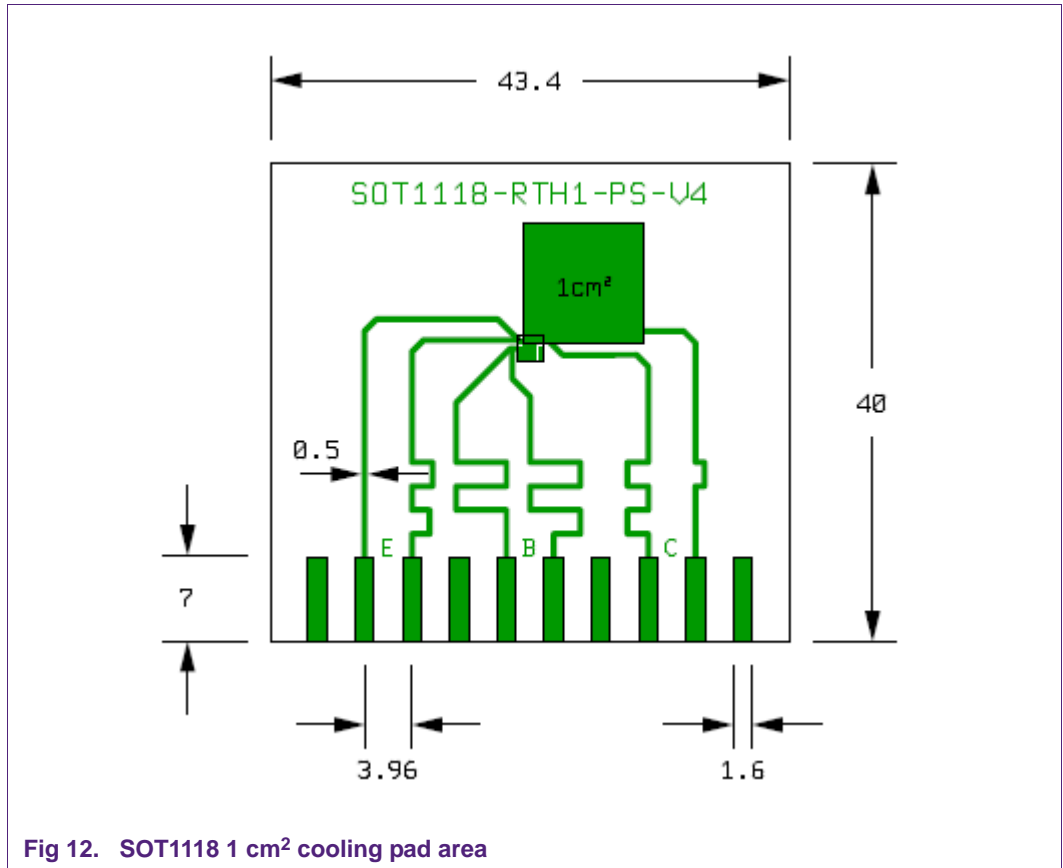


Table 4. PBSM5240PF in SOT1118; typical values

Sample	Standard footprint		1 cm <sup>2</sup> cooling pad	
	R <sub>th</sub> (K/W)	P <sub>tot</sub> (mW)	R <sub>th</sub> (K/W)	P <sub>tot</sub> (mW)
1	149	839	82	1524
2	154	812	86	1453
3	153	817	81	1543
Average	152	822	83	1506
+15 % safety margin	175	715	96	1300
single layer FR4	300	410	180	700

### 4.5 Conclusion

By using the additional copper area of multilayer PCB applications, power dissipation of a transistor can be increased significantly. Most improvement can be seen with newer flat or leadless packages, like SOT89 and SOT1061. The heat generated at the junction can be transported directly by conduction via the collector tab into the PCB. Most of the heat is transferred through the collector pad/exposed heatsink of SOT1061/SOT1118 packages to the PCB. Always consider PCB as an additional tool to manage the thermal behavior of a transistor in any design.

## 5. Legal information

### 5.1 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

### 5.2 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product

design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Evaluation products** — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

### 5.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.



## 6. Contents

---

<b>1</b>	<b>Introduction</b> .....	<b>3</b>
<b>2</b>	<b>Thermal resistance</b> .....	<b>3</b>
2.1	Key parameters .....	3
2.1.1	Thermal resistance from junction to solder point $R_{th(j-sp)}$ .....	4
2.1.2	Thermal resistance from junction to ambient $R_{th(j-a)}$ .....	4
<b>3</b>	<b>Heat transfer mechanism</b> .....	<b>5</b>
3.1	Thermal conduction .....	5
3.2	Thermal convection .....	5
3.3	Thermal radiation .....	5
<b>4</b>	<b>Thermal measurement results</b> .....	<b>6</b>
4.1	SOT457 .....	7
4.2	SOT89 .....	9
4.3	SOT1061 .....	11
4.4	SOT1118 .....	13
4.5	Conclusion .....	14
<b>5</b>	<b>Legal information</b> .....	<b>15</b>
5.1	Definitions .....	15
5.2	Disclaimers .....	15
5.3	Trademarks .....	15
<b>6</b>	<b>Contents</b> .....	<b>16</b>

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

---

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 11 July 2011

Document identifier: AN11076