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Kind regards,

Team Nexperia
This application note illustrates how to improve the power dissipation of discrete components by using multilayer PCBs. It focuses on the impact of using larger copper areas to improve the thermal behavior of applications.
Contact information

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1. Introduction

In today’s data sheets thermal characteristics are measured on a standard FR4 single copper layer Printed-Circuit Board (PCB). Customers should be able to compare devices easily just by evaluating standard data sheet parameters. In reality, design engineers cannot only rely on data sheet parameters and must consider the individual design requirements.

2. Thermal resistance

2.1 Key parameters

The main thermal parameters for semiconductor device are junction temperature (Tj) and thermal resistance (Rth). Thermal resistance depends on the environment surrounding a semiconductor device. In data sheets, design engineers can find different thermal resistances (see Section 2.1.1 and 2.1.2).

Thermal resistance of semiconductor devices is defined in general as:

\[ R_{thx} = \frac{T_j - T_x}{P_{tot}} \]  

(1)

Where \( R_{thx} \) = thermal resistance from the device junction to specific environment [K/W]; \( T_j \) = device junction temperature in steady state [°C]; \( T_x \) = reference temperature of the specific environment [°C] and \( P_{tot} \) = maximum power dissipation of the semiconductor device [W].

Thermal data is not comparable, unless a semiconductor supplier provides all test conditions. NXP Semiconductors provides them. They are often marked with a note at the end of an abstract or table, in the data sheet.

Figure 1 shows the typical structure of small signal devices. The heat is generated at the junction and must be transferred by the leadframe to the outside of the package. Thermal conduction between the die and the leadframe and between the leadframe and the PCB allow this transfer. The heat transfer between PCB and air can be done by convection and/or radiation.
2.1.1 Thermal resistance from junction to solder point $R_{th(j-sp)}$

This parameter depends on the component. The size of the die, the material of the leadframe and the mold compound influence the $R_{th(j-sp)}$. The solder point is defined as the mounting point where the device would be normally soldered to the PCB. It is a conduction path only.

2.1.2 Thermal resistance from junction to ambient $R_{th(j-a)}$

This parameter describes the thermal resistance from the junction (die) to the ambient. It is a single thermal resistance value including all effects of possible series and parallel paths from the junction to the ambient. Typically, it includes all the heat transfer methods of conduction and convection, from the surface of the package and via the PCB.

$R_{th(j-a)}$ is only valid for a specific PCB and not for:

- PCBs of different size, shape or layer stack to the test specification
- Several devices mounted on one PCB
- Operation within a housing, which influences the convection
- Forced cooling, for example, by cooling fan
3. Heat transfer mechanism

Up to three different transfer methods can be used to transfer heat from the die to the ambient.

3.1 Thermal conduction
Conduction is a heat transfer in a medium due to a temperature change. For small-signal discrete components the heat transfer between the die and the leadframe and then the leadframe and the PCB is done by conduction.

3.2 Thermal convection
Convection is a heat transfer from a body due to the movement of a medium, which is in contact with the surface of the body. In our case, it is the transfer of heat from the PCB surface and the ambient air. Due to the poor thermal conductivity of the plastic package, the main path for convection is the PCB/air interface.

3.3 Thermal radiation
Radiation is a heat transfer by emitting heat from a hot body, which will be absorbed by a cooler one. For example PCB surface and surrounding objects such as the side panel of the housing.
4. Thermal measurement results

In PCB design, the numbers of variables are significant. The thermal resistance depends on board size, thickness, cooling pad area and ambient temperature.

Therefore, NXP Semiconductors has developed specific $R_{th}$-PCBs which are according to the JEDEC standards. It helps designers to compare easily relevant thermal parameters from different small-signal discrete vendors. Unfortunately, most applications are not developed on single layer FR4 PCBs. To get a better view of customer requirements, NXP Semiconductors set up a four-layer PCB. All PCBs differ by the top layer layout. Layers 2 to 4 consist of pure copper layers with a dimension of approximately $32 \times 42$ mm (see Figure 4). The top layer design was made on standard footprint and with a $1$ cm$^2$ cooling pad area for each package.
4.1 SOT457

![SOT457 standard footprint](image)

Fig 5. SOT457 standard footprint
Table 1. PBSS5350D in SOT457; typical values

<table>
<thead>
<tr>
<th>Sample</th>
<th>Standard footprint</th>
<th>1 cm² cooling pad</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R(_{th}) (K/W)</td>
<td>P(_{tot}) (mW)</td>
</tr>
<tr>
<td>1</td>
<td>181</td>
<td>689</td>
</tr>
<tr>
<td>2</td>
<td>181</td>
<td>689</td>
</tr>
<tr>
<td>3</td>
<td>181</td>
<td>689</td>
</tr>
<tr>
<td>Average</td>
<td>181</td>
<td>689</td>
</tr>
<tr>
<td>+15 % safety margin</td>
<td>208</td>
<td>600</td>
</tr>
<tr>
<td>Single layer FR4</td>
<td>275</td>
<td>450</td>
</tr>
</tbody>
</table>

Fig 6. SOT457 1 cm² cooling pad area
4.2 SOT89

Fig 7. SOT89 standard footprint
Table 2. PBSS5330X in SOT89; typical values

<table>
<thead>
<tr>
<th>Sample</th>
<th>Standard footprint</th>
<th>1 cm² cooling pad</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$R_{th}$ (K/W)</td>
<td>$P_{tot}$ (mW)</td>
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<tr>
<td>1</td>
<td>79</td>
<td>1582</td>
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<tr>
<td>2</td>
<td>77</td>
<td>1623</td>
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<td>3</td>
<td>72</td>
<td>1736</td>
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<td>Average</td>
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<td>+15 % safety margin</td>
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<td>1420</td>
</tr>
<tr>
<td>Single layer FR4</td>
<td>225</td>
<td>550</td>
</tr>
</tbody>
</table>
4.3 SOT1061

Fig 9. SOT1061 standard footprint
Fig 10. SOT1061 1 cm² cooling pad area

Table 3. PBSS5330PA in SOT1061; typical values

<table>
<thead>
<tr>
<th>Sample</th>
<th>Standard footprint</th>
<th>1 cm² cooling pad</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Rth (K/W)</td>
<td>Ptot (mW)</td>
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<tr>
<td>1</td>
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<td>1096</td>
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<tr>
<td>2</td>
<td>113</td>
<td>1106</td>
</tr>
<tr>
<td>3</td>
<td>111</td>
<td>1126</td>
</tr>
<tr>
<td>Average</td>
<td>112</td>
<td>1116</td>
</tr>
<tr>
<td>+15 % safety margin</td>
<td>129</td>
<td>970</td>
</tr>
<tr>
<td>Single layer FR4</td>
<td>250</td>
<td>500</td>
</tr>
</tbody>
</table>
4.4 SOT1118

![SOT1118 standard footprint](image)

Fig 11. SOT1118 standard footprint
4.5 Conclusion

By using the additional copper area of multilayer PCB applications, power dissipation of a transistor can be increased significantly. Most improvement can be seen with newer flat or leadless packages, like SOT89 and SOT1061. The heat generated at the junction can be transported directly by conduction via the collector tab into the PCB. Most of the heat is transferred through the collector pad/exposed heatsink of SOT1061/SOT1118 packages to the PCB. Always consider PCB as an additional tool to manage the thermal behavior of a transistor in any design.
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