

AN11045

Next generation of NXP low VCEsat transistors: improved technology for discrete semiconductors

Rev. 3 — 28 February 2013

Application note

Document information

Info	Content
Keywords	Breakthrough In Small Signal (BISS) transistor, low VCEsat, load switch, DC-to-DC converter
Abstract	This application note contains detailed information about the latest generation of low VCEsat transistors providing a further improvement in performance. This opens a new field of applications for bipolar transistors with higher power requirements and improved energy efficiency.



Revision history

Rev	Date	Description
3	20130228	Added Table 5 and Table 6
2	20110623	Table 3 : corrected mounting area.
1	20110525	Initial version

Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

The performance of bipolar transistors has significantly improved in recent years. The collector-emitter saturation resistance has been reduced towards values which were known from MOSFETs only. NXP Semiconductors latest generation of medium-power low collector-emitter saturation voltage V_{CEsat} transistors in Surface-Mounted Design (SMD) packages opens a new field of applications. Switching applications with higher power and current requirements can also be realized, while the overall efficiency is further improved.

In the last years switching applications for higher power ratings are realized with MOSFETs as switching elements in most cases because the low drain-source on-state resistance R_{DSon} values together with fast switching times guarantee low losses. Furthermore MOSFETs do not require a static control current.

Nowadays there is a revival of bipolar transistors in load switch and charging applications for mobile equipment in the area of communication and consumer applications. The residual on-state resistance of the latest generation bipolar transistors has become comparable to MOSFETs in the same package. Due to a high and constant current amplification, rather small base currents are sufficient to control the Bipolar junction transistor (BJT) switches. Although the bipolar technology has the disadvantage of the current-based control, there are important advantages such as ElectroStatic Discharge (ESD) robustness and an inherent backward current blocking. The temperature stability of some important key parameters is higher for bipolar transistors than for MOSFETs. The base-emitter voltage V_{BE} has a temperature coefficient of about 2 mV/K, whereas the gate-source threshold voltage $V_{GS(th)}$ changes with a factor of about 4 mV/K to 6 mV/K. The same holds for the on-state resistance. The collector-emitter saturation resistance R_{CEsat} decreases with about 0.4 %/K over temperature, the drain-source on-state resistance R_{DSon} of a MOSFET increases with a factor of about 0.6 %/K.

NXP Semiconductors developed a new architecture for its fourth generation of low V_{CEsat} Breakthrough In Small Signal (BISS) transistors. The medium-power transistors in SMD packages mark a new milestone in performance, expanding the spectrum of applications.

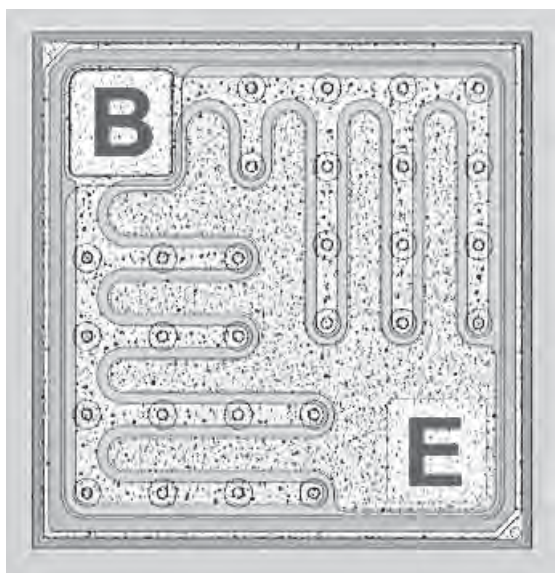
2. Higher performance for low V_{CEsat} BISS transistors

2.1 Technological background of low V_{CEsat} transistors

The major contribution to the power dissipation of a bipolar transistor in a switching application is the collector current related loss, which can be calculated as $P_C = V_{CEsat} \times I_C$. The current depends on the application, this means on the resistance of the load and the supply voltage. Therefore the minimum residual voltage measured between collector and emitter when the transistor is driven in a saturated condition is the only choice for a designer to improve the power efficiency. Transistors developed with the target to achieve a very low saturation voltage are called low V_{CEsat} transistors. In the design of the die, the emitter region is spread across a large area. The layout of the base contact has a geometry which enables an even and efficient drive for the whole active area. Low V_{CEsat} transistors show a so-called mesh-design, in which the transistor is separated into many corresponding cell structures. Transistors with this topology have an outstanding performance regarding V_{CEsat} and also show a high and constant current amplification.

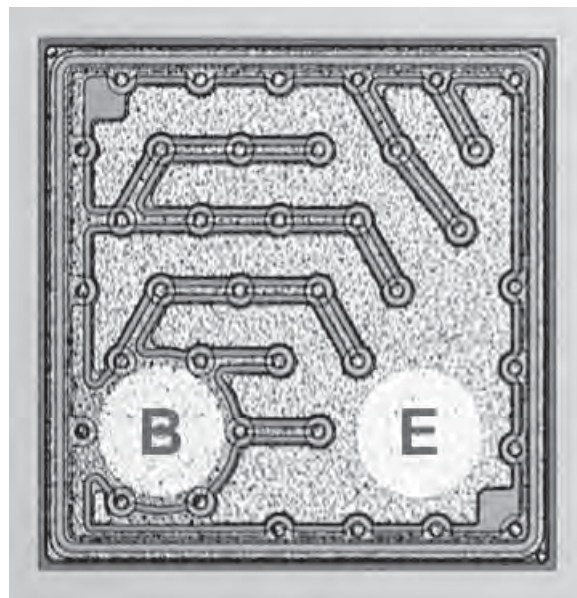
[Figure 1](#) to [Figure 4](#) show the die layout of the four generations of NXP BISS transistors.

The generations BISS-3 and specifically BISS-4 show an even more efficient use of the emitter area and a higher number of corresponding cell structures.



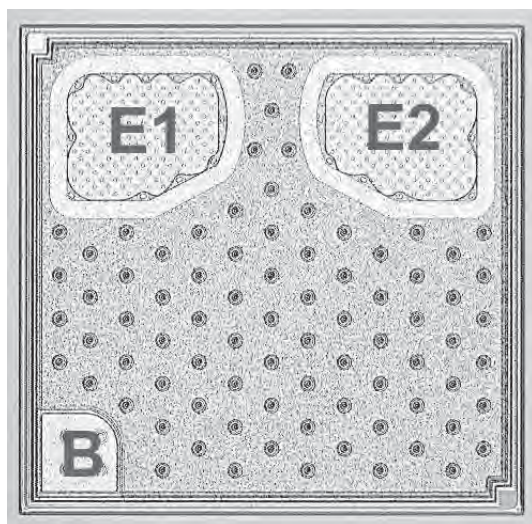
006aac619

Fig 1. Die layout of a BISS first generation



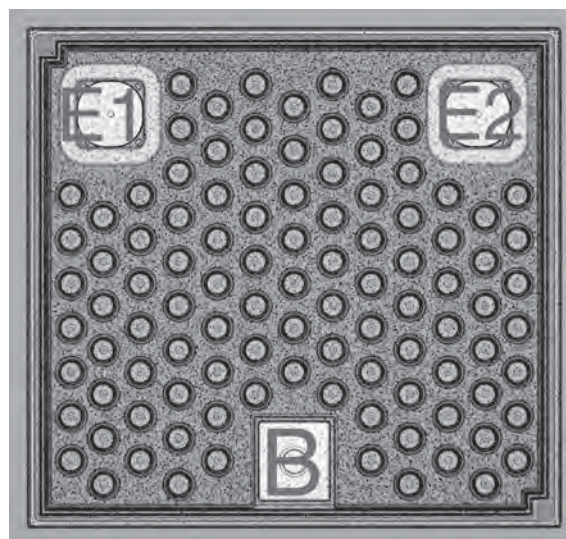
006aac620

Fig 2. Die layout of a BISS second generation



006aac621

Fig 3. Die layout of a BISS third generation



006aac622

Fig 4. Die layout of a BISS fourth generation

2.2 BISS-4: a milestone in the development of medium-power bipolar transistors

The development of a new family of medium-power bipolar transistors requires a review of the whole architecture of the transistor: the chip design itself, the choice of material, the metallization of the chip, the connection between chip and package, the bonding and the consideration of the aspects of the different packages. All of these items contribute to the overall collector-emitter resistance which can be achieved for the final component.

The BISS-4 product portfolio has two branches. The first focuses on an ultra low V_{CEsat} performance in order to minimize the saturation resistance as much as possible. The target for the development was to reach an R_{CEsat} as low as 14 m Ω in SMD packages. This is an on-state resistance seen previously only in advanced MOSFETs. The second branch was designed for high-speed switching applications. In addition to the reduction of R_{CEsat} , short switching and storage times were an important target for development.

A requirement of the architecture of the products from both branches was the possibility to integrate it into a wide range of SMD packages. The target packages were SOT23, SOT457 (SC-74), SOT223, SOT89 and SOT96 (SO-8). This large portfolio enables the implementation of transistors into various applications. A cost-effective mass production with high volume and a good delivery performance can be ensured by this approach. The NXP low V_{CEsat} transistors are qualified according to AEC-Q101 and are suitable for applications in the automotive area, as well as communication, consumer, computing and industrial areas. The whole product family is produced in Dark Green packages, which are free of halogens and antimony oxides and complies with the classification UL94V-0 and Restriction of Hazardous Substances (RoHS) standards regarding non-flammability.

2.2.1 Reduction of the on-state resistance to ultra low values

The saturation voltage can be separated into ohmic losses and losses produced by recombination and injection processes. Ohmic losses are the biggest contributor to the saturation voltage of a bipolar transistor. This includes the resistance of the semiconductor substrate, the design of the chip, the resistances introduced by bonding, and the package technology.

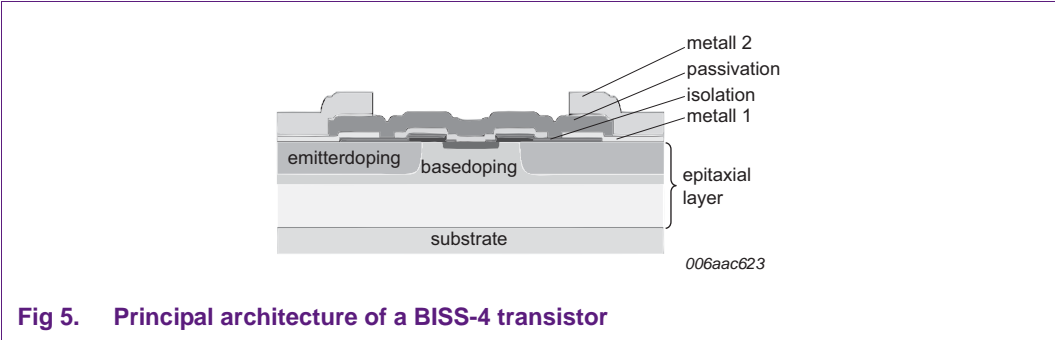


Fig 5. Principal architecture of a BISS-4 transistor

In order to reduce the losses of the semiconductor material, low-ohmic substrates doped with phosphorus are often used. A very homogenous current distribution in the chip and a low resistance in the chip front-side metallization are key factors necessary to achieve a low V_{CEsat} value.

The homogenous current distribution is achieved by the mesh-design (see Figure 1 to 4) which divides the transistor into a cell structure. A patented double-layer front-side metallization minimizes the resistance of the emitter paths. Figure 5 shows the principal architecture of a fourth generation BISS transistor.

Figure 6 shows the reduction of R_{CEsat} compared to a conventional low V_{CEsat} transistor in an SOT23 package. It also shows the contribution of changes in assembly, front metallization, active area, and substrate material.

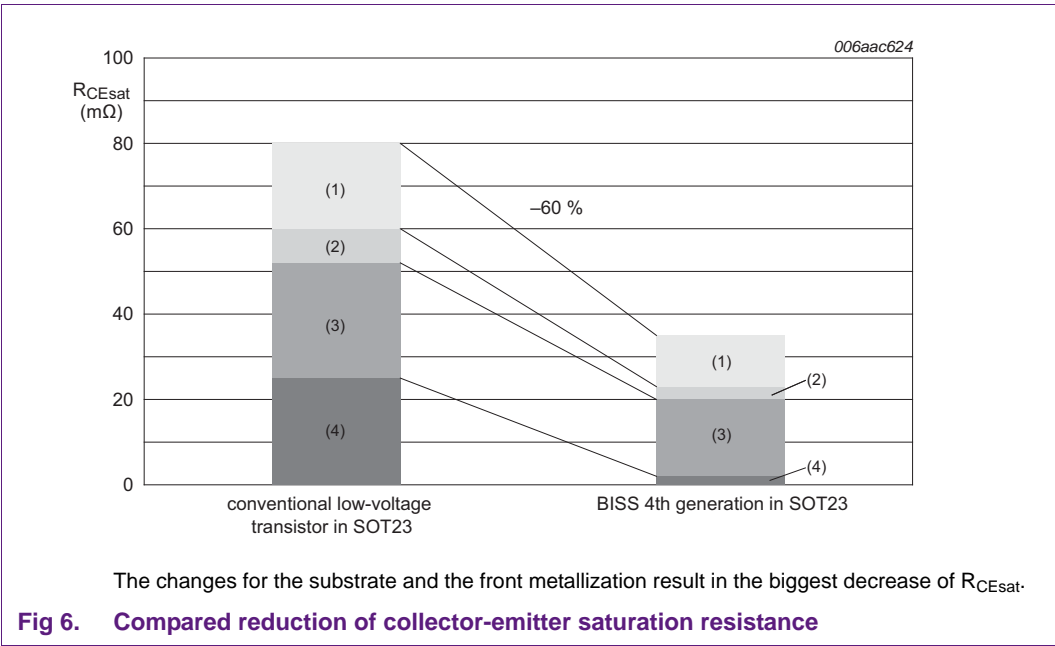
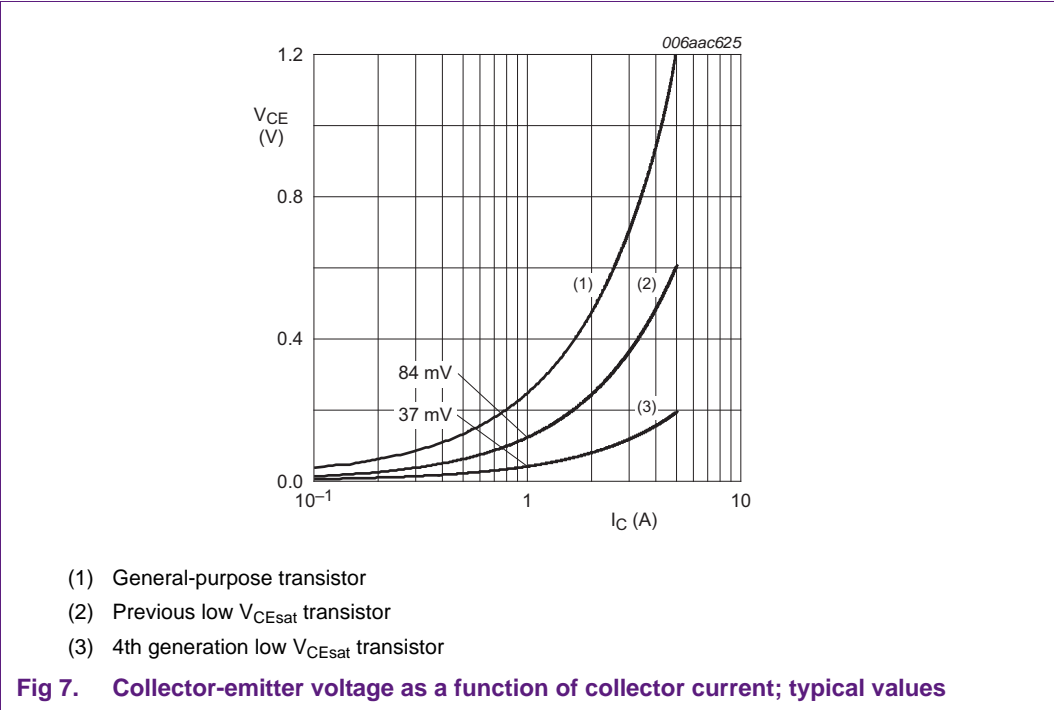


Fig 6. Compared reduction of collector-emitter saturation resistance

Figure 7 shows the saturation voltage as a function of collector current for a general-purpose transistor such as a BC847 compared to a BISS transistor of the previous generation and to a BISS-4 transistor (PBSS4021NT). The package type is SOT23.

The saturation voltage for a collector current of 1 A is highlighted. For the new type a saturation voltage of only 37 mV is measured, which is more than a factor two compared to the older generation.



2.2.2 Reduction of switching and storage times

The target of the design of the second branch of the BISS-4 family was to achieve short switching and storage times in addition to a small saturation voltage. The diffusion capacities play the major role for the switching speed. For a transistor in saturation mode, the base voltage is higher than the collector potential. Parasitic clamping diodes as depicted in Figure 9 help to reduce the storage time (t_s) significantly.

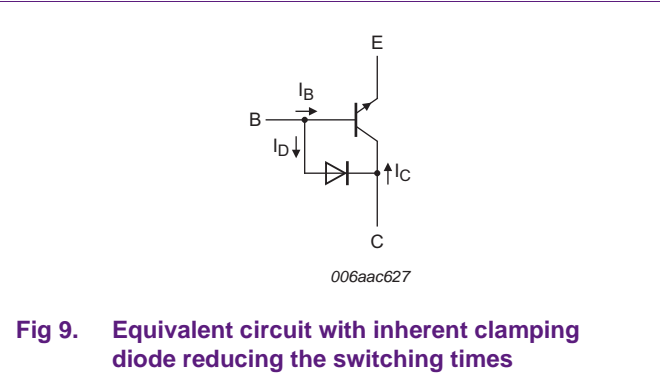
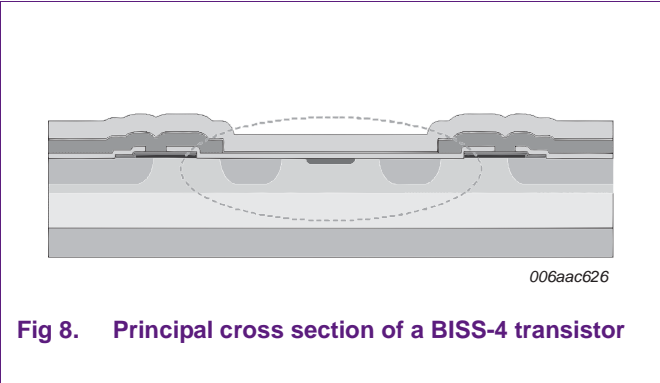


Table 1 shows a comparison between the two branches of the 4th generation of BISS transistors regarding the storage time and the rise time.

The PBSS4021NT is optimized for an ultra low V_{CEsat} , the PBSS4032NT is designed for an optimized switching performance. The rise time of the PBSS4032NT is reduced by a factor three and the storage time is significantly shorter as well.

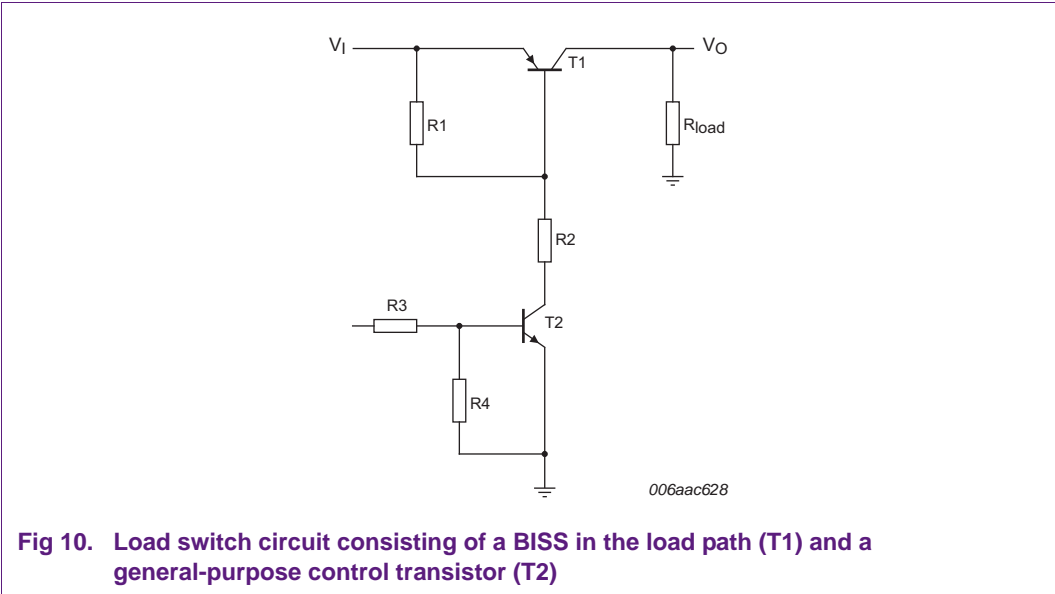
Table 1. Comparison of the storage times between the two branches of transistors from the 4th generation BISS

Transistor version	Type number	storage time (t_s)	rise time (t_r)
BISS-4, switching-optimized	PBSS4032NT	135 ns	20 ns
BISS-4, optimized for lowest V_{CEsat}	PBSS4021NT	340 ns	60 ns

3. Application examples with BISS transistors

3.1 Load switch application

A typical application for low V_{CEsat} transistors is a so-called load switch (see Figure 10). The most commonly used architecture for this circuit is the combination of a high-side switch (T1) and a control transistor (T2). In this approach the loads are constantly connected to ground and the positive supply can be turned on and off.



The realization of a load switch with bipolar transistors has some major advantages.

Reverse currents from the output side back to the input are blocked as an inherent feature of a BJT. This function is required if the load switch is used as a path element in a charger application. A battery connected to the output must not feed back current into a connected input power supply which is switched off. If the load transistor is realized with a P-channel MOSFET, the body diode would conduct a reverse current. To avoid this, an extra diode in the load current path needs to be implemented. Because the forward voltage of the diode needs to be added to the R_{DSon} losses of the FET, the efficiency of such a load switch application becomes rather low.

A further advantage of the solution with bipolar transistors is the robustness with respect to ESD.

Moreover a bipolar transistor requires a small control voltage only, because the forward voltage of the base-emitter diode is about 0.7 V without a large spread. The gate-source threshold of a MOSFET has a rather large spread. Therefore a bigger control voltage is required in practice. If small voltages shall be switched with a P-channel MOSFET in the load path, a simple circuit approach like depicted in [Figure 10](#) cannot be used anymore and a BISS transistor is a good option.

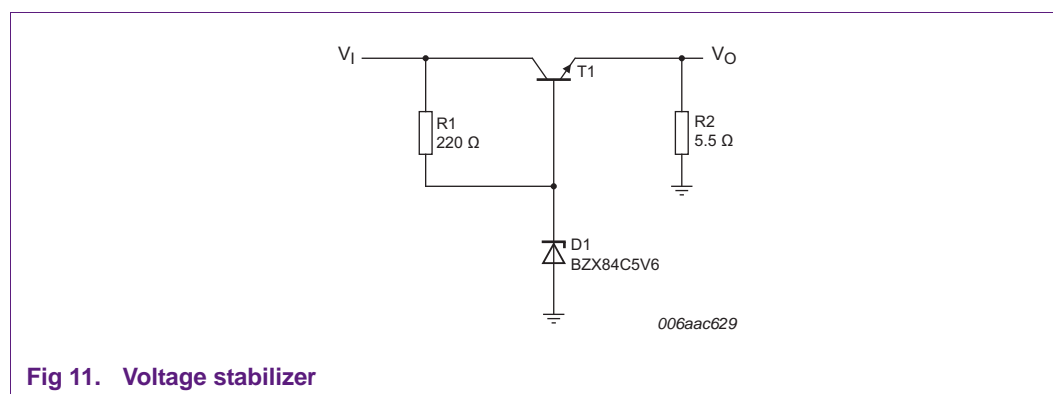
The NXP BISS transistors provide a high and constant current amplification. A current gain (h_{FE}) of about 400 is typical for the BISS transistor family. Thus the control losses are small compared to a conventional BJT. The control losses for the load path are equal to $I_{C(T2)} \times V_I$. In many applications where MOSFETs have been used, the BISS-transistor-based solution can be considered.

3.2 Voltage stabilizer

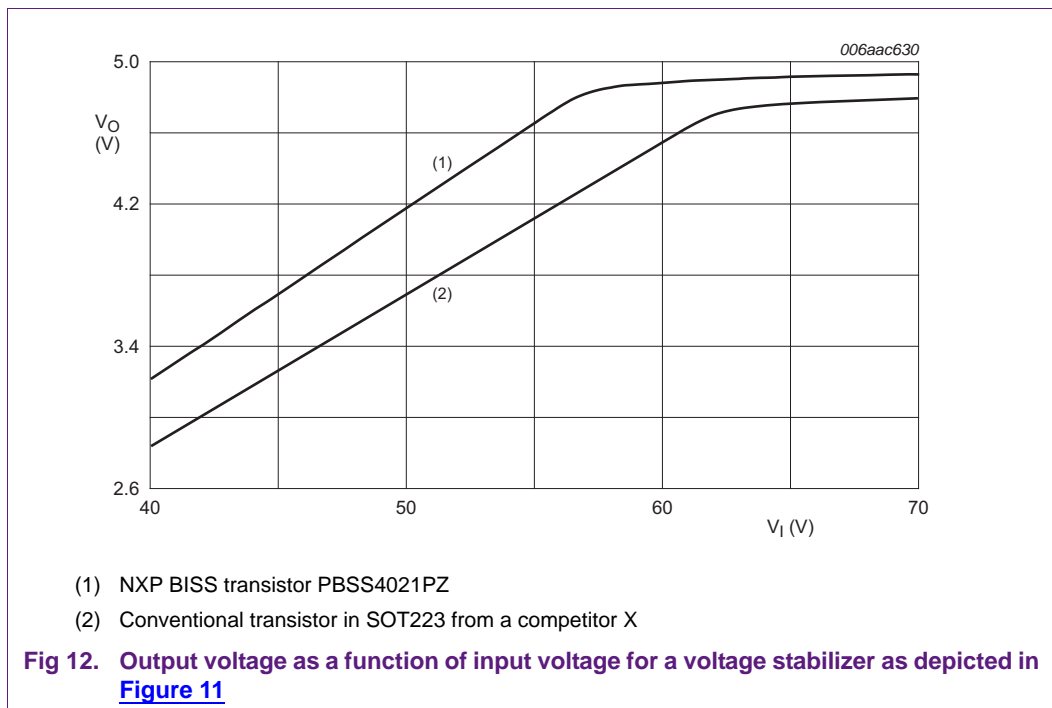
Due to the high and constant current amplification, BISS transistors are a better choice than general-purpose bipolar transistors for many applications where the device is not driven in saturation mode.

As an example, [Figure 11](#) shows a simple voltage stabilizer. The active part of the circuit is an NPN transistor. Its base is connected to the input voltage via R1 and a Zener diode connected to ground. The output voltage V_O follows the equation: $V_O = V_Z - V_{BE}$ (V_Z is the Zener voltage).

An important key parameter for a voltage stabilizer is the voltage headroom required to come to the nominal output voltage for a defined output current, this is the so-called dropout voltage.



[Figure 12](#) shows the output voltage of the circuit versus the input voltage with a load resistor of 10 Ω . This means that about 0.5 A are driven through the load.

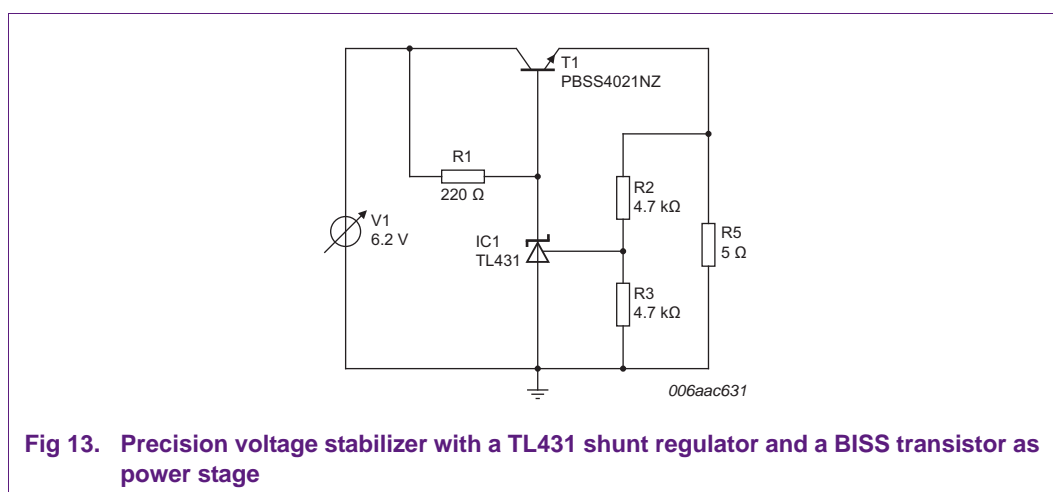


Due to the high current amplification factor of the BISS transistor, the circuit starts to work in order to stabilize the output voltage from about 5.8 V onwards. As a result of the low saturation voltage, a low dropout voltage can be achieved. The general-purpose transistor requires 0.6 V more. This means that the minimum dropout voltage of the BISS-transistor-based solution is significantly lower. The base-emitter voltage V_{BE} of the general-purpose transistor is constantly higher, even if a high input voltage is applied. The power efficiency of the solution with the NXP BISS transistor is significantly higher. A lower input voltage can be applied and a lower base current is needed for a desired output current. The energy efficiency of the solution based on a BISS transistor is much higher.

Figure 13 shows a more precise voltage stabilizer circuit. The simple Zener diode is replaced by a TL431 shunt regulator. If the reference voltage at R2 tends to fall below 2.495 V, the device increases its cathode to anode resistance. As a consequence T1 gets a higher base current via R1, increasing the output voltage and thus the exact reference voltage is maintained. The output voltage can be calculated according to the formula:

$$V_O = (1 + R3/R2) \times 2,495 \text{ V}$$

The circuit example is designed for an output voltage of 5 V. A load current of 1 A is simulated. An input voltage of 6.2 V is high enough as headroom for the stabilizer.



3.3 DC-to-DC converter

Another suitable application for low V_{CEsat} transistors and specifically the product branch optimized for high-speed switching is the area of DC-to-DC conversion.

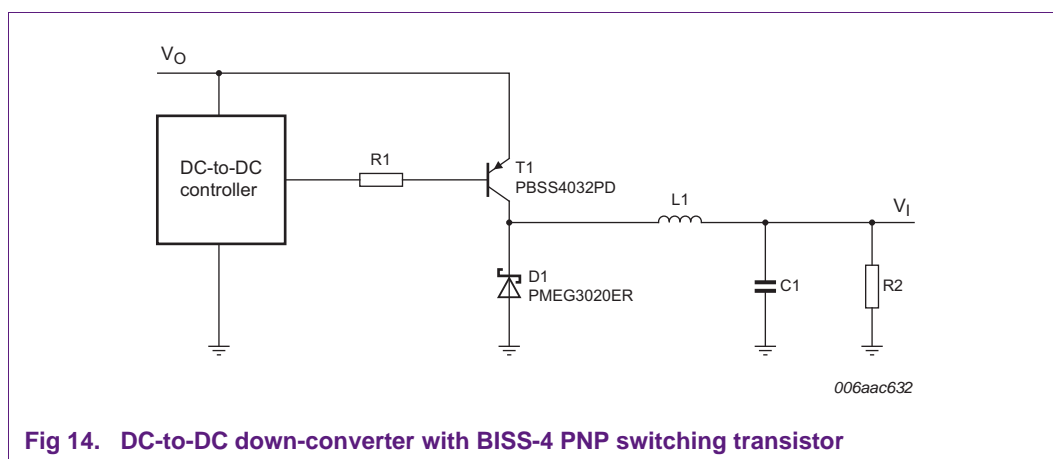


Figure 14 shows an example for a DC-to-DC down-converter. While the BISS transistor T1 is switched on, the current through the inductor L1 increases. The capacitor C1 is charged and a current flows through the load resistor R2. When the transistor is switched off, the current through L1 continues to flow, but through the Schottky diode D1. The current decreases over time. As a result, the current through L1 shows a triangle shape if we assume a load condition where the converter runs in the so-called continuous mode. This means that the current through the inductor never goes

down to zero. The ripple of the output voltage is reduced by the capacitor C1 to a desired level. If the switching frequency is increased, smaller inductors and capacitors can be used. On the other hand more switching losses occur in T1.

The efficiency of the circuit is mainly determined by the R_{CEsat} of T1 and the switching losses at the transition times of T1. The diode D1 produces forward losses ($V_F \times I_{load}$) for the time that T1 is switched off and reverse losses ($V_I \times I_R$) when T1 is switched on. If the diode is run at a high temperature, the reverse losses increase while the forward voltage is decreasing.

Furthermore the control energy for T1 has to be taken into account ($I_B \times V_{BE}$) as well as ohmic losses in L1 and C1.

The output voltage for the continuous mode can be calculated rather easily as $V_O = \delta \times V_I$. δ is the duty cycle of the switching of T1.

The high and constant current gain, the low saturation voltage and the good switching performance of NXP BISS-4 transistors like the PBSS4032PD allow the use of a bipolar transistor for the described circuit of medium-power DC-to-DC converter instead of a P-channel MOSFET. The BISS transistor proposed in the example is optimized for minimized switching times. It is a product out of the high-speed switching branch from the fourth-generation BISS transistor family (see [Section 2.2.2](#)). The storage and switching times are much reduced compared to types optimized for an ultra low V_{CEsat}.

3.4 Overvoltage protection

This section is about an application that can protect a load circuit against an overvoltage which might occur due to a defective or an unsuitable power supply.

[Figure 15](#) shows the circuit diagram. The input voltage V_I is connected via the resistor divider R2 and R3 to the reference input of a TL431 shunt regulator IC1. If the voltage at the reference input is below 2.495 V, there is a very low current through R1 and T2 does not conduct. Therefore T1 is switched on via the bias resistor R5 and the input voltage is fed to the load circuit without large voltage losses ($V_O = V_I - V_{CEsat}$).

If the input voltage rises to a value where the voltage at the reference pin of IC1 exceeds 2.495 V, a current starts to flow through R1, T2 is switched on and T1 is switched off. The load circuit at the output is protected against an overvoltage. If $V_I > (1 + R3/R2) \times 2.495$, the protection is getting active. This means that the load is disconnected from the supply voltage.

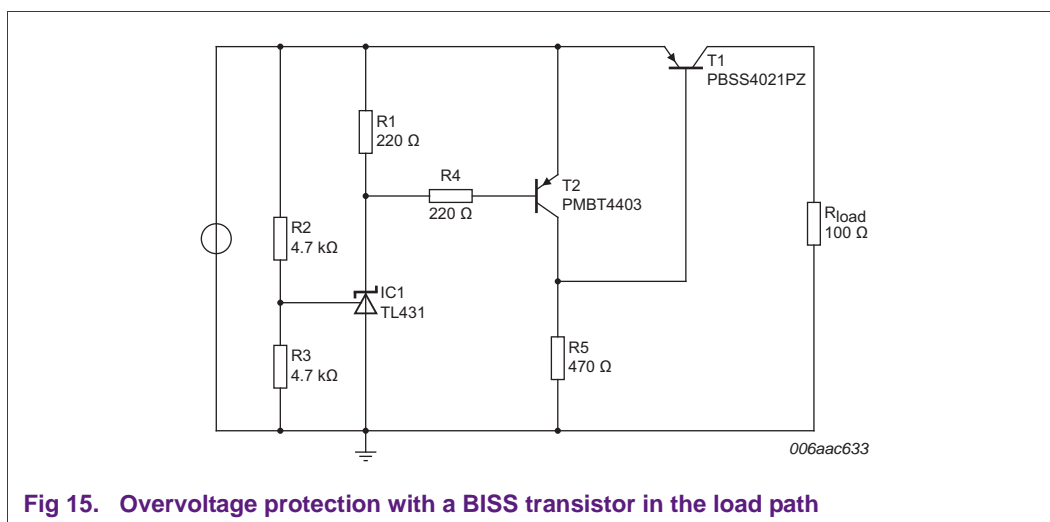
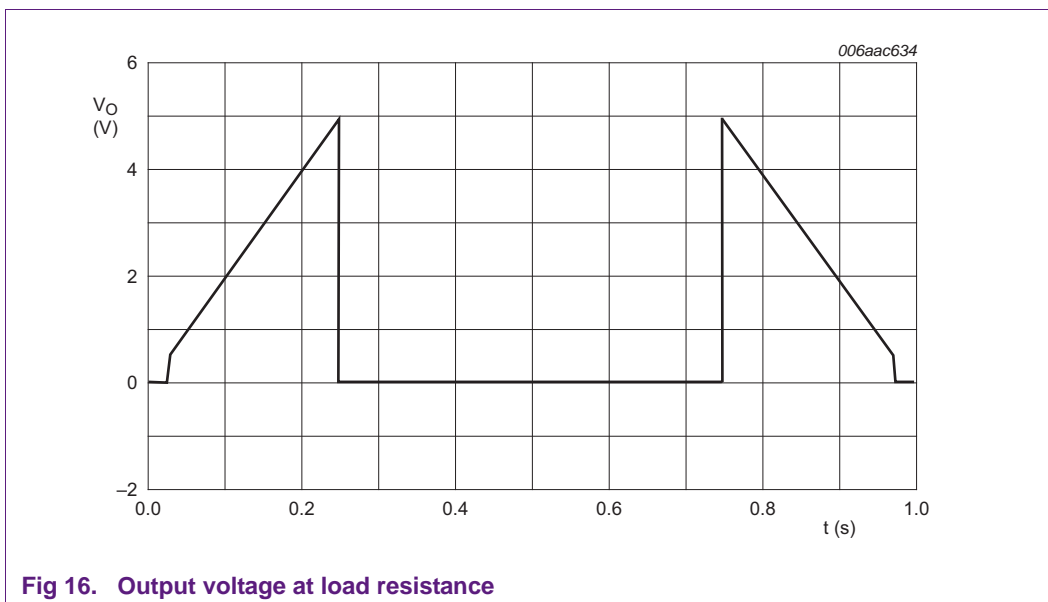


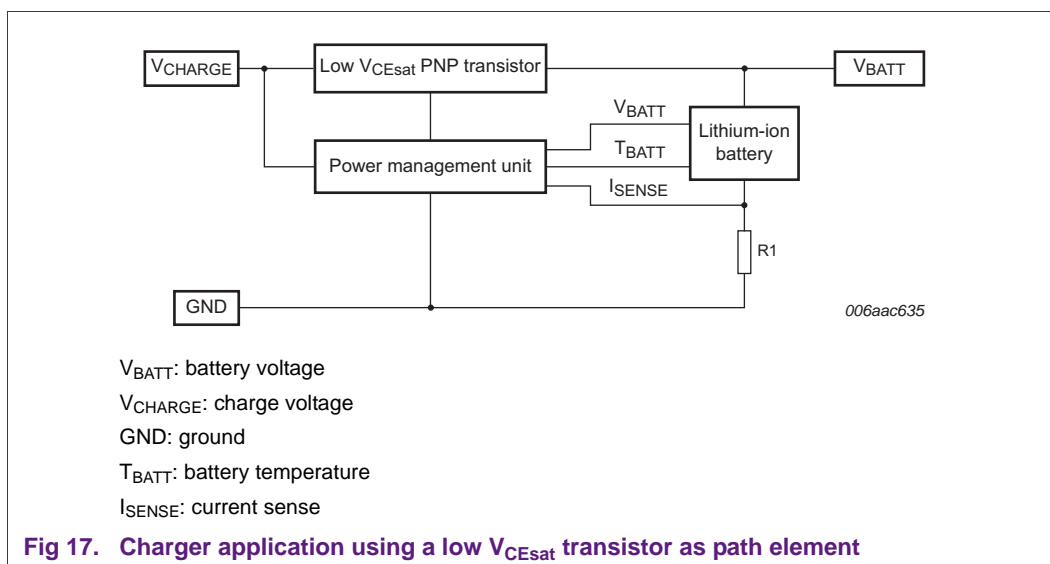
Fig 15. Overvoltage protection with a BISS transistor in the load path

The scope trace in [Figure 16](#) shows the output voltage of the circuit at the load resistor R_{load} . A triangle-shaped waveform is applied at the input of the circuit. The output voltage follows the input until $V_I > (I + R3/R2) \times 2,495$ becomes true. In this case the output voltage is switched off and the connected circuit cannot be destroyed by an overvoltage supplied from the input.



3.5 Charger application

Low V_{CEsat} transistors can be found in many charger applications, such as chargers for mobile phone, navigation systems and other battery-driven medium-power applications. A block diagram of such a charging application is shown in [Figure 17](#).



The advantage of this solution is the inherent reverse blocking of a bipolar transistor. In FET solutions, an extra diode needs to be added or two FETs in a back-to-back configuration need to be used. Depending on the concept of the power management unit, the charging is controlled in a linear or switched mode.

4. Higher performance in smaller packages

4.1 General-purpose transistors versus low V_{CEsat} transistors

A comparison of a general-purpose transistor like a BC817-40 versus a state-of-the-art low V_{CEsat} transistor in mesh-emitter technology like the PBSS4240T in depicted in [Table 2](#). It shows the large achievements in performance for the new design.

With the reduced saturation voltage of the BISS transistor the collector-emitter losses $I_C \times V_{CEsat}$ are significantly smaller (factor 7 for the maximum values at collector current $I_C = 0.5$ A in the example from [Table 2](#)). For a defined maximum junction temperature, the BISS can be used for higher currents. Smaller energy losses and a lower junction temperature can be achieved if a general-purpose transistor is replaced by a BISS transistor in an application. As a result, BISS transistors can replace general-purpose transistors in much bigger packages.

A further advantage is the high gain amplification of the low V_{CEsat} transistors. In addition the current gain h_{FE} remains stable for high collector currents.

Table 2. Comparison of a general-purpose transistor with a BISS transistor, both in SOT23

Type number	Collector current $I_{C(max)}$	Collector-emitter voltage $V_{CEO(max)}$	Total power dissipation P_{tot}	Collector-emitter saturation voltage $V_{CEsat(max)}$		Current gain $h_{FE(min)}$ $I_C = 0.5$ A
				$I_C = 0.5$ A; $I_B = 0.05$ A	$I_C = 2$ A; $I_B = 0.2$ A	
BC817-40	0.5 A	45 V	250 mW	700 mV	-	40
PBSS4240T	2.0 A	40 V	300 mW	320 mV	320 mV	300

Many applications do not require high collector-emitter voltages and types like the PBSS4021NT with a maximum V_{CEO} of 20 V can be used. [Table 3](#) compares a BCP54 medium-power general-purpose transistor in SOT223 with a PBSS4021NT BISS transistor in SOT23. The maximum saturation voltage of the PBSS4021NT is 17 % of the value for the BCP54 although the base current is five times smaller for the BISS transistor. The power capability of the SOT223 package is about a factor of 3.5 higher than for the SOT23. This factor is smaller than the improvement factor for the saturation voltage. This shows that the much smaller BISS transistor can easily replace a general-purpose transistor in a much bigger package if it is applied in a switching application.

Furthermore the drive current requirements for the driving circuit are very much reduced for a BISS transistor approach. There is a factor 15 for the minimum gain amplification between the two types compared in [Table 3](#).

Table 3. Comparison of a general-purpose transistor (BCP54 in SOT223) with a BISS transistor (PBSS4021NT in SOT23)

Type number	mounting area	Collector current $I_{C(max)}$	Collector-emitter voltage $V_{CEO(max)}$	Total power dissipation P_{tot}	Collector-emitter saturation voltage $V_{CEsat(max)}$	Current gain $h_{FE(min)}$ $I_C = 0.5$ A
					$I_C = 0.5$ A	
BCP54	46 mm ²	1 A	45 V	640 mW	500 mV (at $I_B = 50$ mA)	40
PBSS4021NT	8.2 mm ²	4.3 A	20 V	390 mW	20 mV (at $I_B = 25$ mA)	300

4.2 Supported packages for NXP BISS transistors

NXP BISS transistors are offered in a significant variety of SMD packages: SOT223, SOT89, SOT457, SOT23, SOT323, SOT363, SOT416, SOT666, and SOT883. In addition to these well-known gull wing packages, a DFN2020-3 (SOT1061) 2 mm × 2 mm Quad Flat No-leads (QFN) package is available. This package has a thermal performance which is close to a SOT89, however the mounting area is much smaller. [Table 4](#) compares two 30 V BISS transistors, the PBSS4630PA in DFN2020-3 (SOT1061) and the PBSS4032NX in SOT89. The factor between the mounting areas is about a quarter, which means that the DFN2020-3 (SOT1061) package enables a large Printed-Circuit Board (PCB) area saving for designs with space constraints.

Table 4. Comparison of two low V_{CEsat} transistors: PMSS4630PA in DFN2020-3 and PBSS4032NX in SOT89

Type number	mounting area	Collector current $I_{C(max)}$	Collector-emitter voltage $V_{CEO(max)}$	Total power dissipation P_{tot} [1]	Collector-emitter saturation voltage $V_{CEsat(max)}$	Current gain $h_{FE(min)}$
					$I_C = 2\text{ A}; I_B = 0.4\text{ A}$	$I_C = 2\text{ A}$
PBSS4630PA	4.8 mm ²	6 A	30 V	500 mW	185 mV	260
PBSS4032NX	19.9 mm ²	4.7 A	30 V	600 mW	250 mV	250

[1] Device mounted on an FR4 PCB, single-layer, standard footprint.

NXP develops an increasing portfolio of low V_{CEsat} transistors in DFN packages. [Table 5](#) and [6](#) give an overview of available BISS transistors in leadless packages.

Table 5. NPN low V_{CEsat} BISS transistors in leadless packages

Type number	Package	Collector-emitter voltage $V_{CEO(max)}$	Collector-emitter saturation voltage V_{CEsat}	Collector current $I_{C(max)}$
			$I_C = 0.5\text{ A}; I_B = 0.5\text{ A}$	
PBSS4612PA	DFN2020-3	12 V	20 mV	6.0 A
PBSS4620PA	DFN2020-3	20 V	20 mV	6.0 A
PBSS4330PA	DFN2020-3	30 V	40 mV	3.0 A
PBSS4630PA	DFN2020-3	30 V	21 mV	6.0 A
PBSS4560PA	DFN2020-3	60 V	22 mV	6.0 A
PBSS4580PA	DFN2020-3	80 V	25 mV	5.6 A
PBSS8510PA	DFN2020-3	100 V	30 mV	5.2 A
PBSS2515M	DFN1006-3	15 V	250 mV (max)	0.5 A
PBSS2515MB	DFN1006B-3	15 V	250 mV (max)	0.5 A
PBSS2540M	DFN1006-3	40 V	200 mV	0.5 A
PBSS2540MB	DFN1006B-3	40 V	200 mV	0.5 A

Table 6. PNP low V_{CEsat} BISS transistors in leadless packages

Type number	Package	Collector-emitter voltage $V_{CEO(max)}$	Collector-emitter saturation voltage V_{CEsat}	Collector current $I_{C(max)}$
			$I_C = -0.5\text{ A}; I_B = -0.5\text{ A}$	
PBSS5612PA	DFN2020-3	-12 V	-20 mV	-6.0 A
PBSS5620PA	DFN2020-3	-20 V	-25 mV	-6.0 A
PBSS5330PA	DFN2020-3	-30 V	-45 mV	-3.0 A
PBSS5630PA	DFN2020-3	-30 V	-25 mV	-6.0 A
PBSS5560PA	DFN2020-3	-60 V	-35 mV	-5.0 A
PBSS5580PA	DFN2020-3	-80 V	-40 mV	-4.0 A
PBSS9410PA	DFN2020-3	-100 V	-45 mV	-2.7 A
PBSS3515M	DFN1006-3	-15 V	-150 mV	-0.5 A
PBSS3515MB	DFN1006B-3	-15 V	-150 mV	-0.5 A
PBSS3540M	DFN1006-3	-40 V	-220 mV	-0.5 A
PBSS3540MB	DFN1006B-3	-40 V	-220 mV	-0.5 A

5. Summary

Thanks to their outstanding low saturation voltage combined with a high current amplification rather constant for high collector currents, NXP low V_{CEsat} transistors can improve the energy efficiency in many application areas. With the fourth generation of BISS transistors NXP offers the best-in-class products. Due to their superior performance, low V_{CEsat} transistors can replace standard transistors in bigger packages allowing more compact designs on smaller PCBs.

Two branches of low V_{CEsat} transistors are provided. The first is optimized for ultra low saturation voltages, and the second branch is optimized for high-speed switching. The products are available in a significant range of SMD packages from SOT223 down to the small SOT883. The devices are offered as single and double transistors, as Resistor-Equipped Transistors (RETs) and as integrated load switches.

A wide field of application can be supported in consumer, automotive, computing and industrial areas. BISS transistors are often a better choice than comparable MOSFETs because they provide reverse blocking and high ESD robustness. The losses in the collector-emitter path are comparable to the R_{DSon} losses of MOSFETs. Due to the high current amplification, the energy required for the control could be significantly decreased.

6. Legal information

6.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

7. Contents

1	Introduction	3
2	Higher performance for low V_{CEsat} BISS transistors	3
2.1	Technological background of low V_{CEsat} transistors	3
2.2	BISS-4: a milestone in the development of medium-power bipolar transistors	5
2.2.1	Reduction of the on-state resistance to ultra low values	6
2.2.2	Reduction of switching and storage times	7
3	Application examples with BISS transistors	8
3.1	Load switch application	8
3.2	Voltage stabilizer	9
3.3	DC-to-DC converter	11
3.4	Overvoltage protection	13
3.5	Charger application	15
4	Higher performance in smaller packages	16
4.1	General-purpose transistors versus low V_{CEsat} transistors	16
4.2	Supported packages for NXP BISS transistors	17
5	Summary	18
6	Legal information	19
6.1	Definitions	19
6.2	Disclaimers	19
6.3	Trademarks	19
7	Contents	20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 28 February 2013

Document identifier: AN11045