AN10911

SD(HC)-memory card and MMC interface conditioning

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Document information

Info	Content
Keywords	SD-memory card, Multi Media Card (MMC), ElectroStatic Discharge (ESD) protection, ElectroMagnetic Interference (EMI) filtering
Abstract	This document gives an overview about different ESD protection and EMI filter devices optimized for SD-memory card and MMC interfaces. These devices cover the range from 1-bit to current standard 4-bit (SD-memory card, SD 2.0) or 8-bit (MMC) high-speed memory card interfaces.

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Revision history

Rev	Date	Description
2	20130404	Discontinued products removed
1	20100429	Initial version

1. Introduction

The SD-memory card and MMC are the most popular memory cards in modern communication, computer and consumer appliances. They support state-of-the-art security and capacity requirements of modern audio and video applications in consumer and communication products.

SD-memory cards support content protection, prevention of illegal use of content and security systems based on, for example ISO-7816. An embedded version of MMC is eMMC, according to the JESD84-A43. It offers up to 8-bit wide interface and can be applied in SD-memory card compatible hardware interfaces.

While the SD-memory card adds an advanced data storage function to an application, there is a more general Secure Digital Input Output (SDIO) card.

The SDIO card specification provides separately a specified interface to different I/O units. It provides various functions to an SD host, including memory storage that is compatible with the SD-memory card specification. Even if an SD host is not SDIO compatible (just supporting SD-memory cards), no physical damage or disruption of operation will occur.

An SD-memory card communication is based on an advanced 8/9-pin interface (clock, command, 1- or 4-bit data and 2/3 × power/GND) designed to operate at a maximum operating frequency of 50 MHz according to SD 2.0 specification.

The MMC works with an up to 52 MHz clock but supports in its latest versions up to 8 data bits in a 13-pin interface (clock, command, 1-, 4- or 8-bit data, 3 × power/GND).

While the SD-memory card can contain some ESD protection (see chapter 8.1.3. of Ref. 1 “SD specifications, part 1, Physical Layer Specification version 2.00, May 9, 2006”), SD host interfaces require an additional high-level ESD protection according to the IEC61000-4-2 standard in addition to the host-interface integrated ESD protection which is typically very weak.

Strict EMI regulations and system requirements, as specified in GSM mobile phones, request filters that reduce the radiated and/or conducted EMI but still comply with the electrical requirements of the interface specification.

The continuing trend in miniaturization of portable appliances implies that interface devices offering ESD protection and EMI filtering should also, where possible, integrate biasing circuits or resistors into a single small-sized package.

NXP Semiconductors SD-memory card interface conditioning devices explained in this document fully support this continuing trend and offer interface conditioning functions such as:

- High-level ESD protection according the IEC61000-4-2 standard, often exceeding the highest specified level 4
- EMI filtering, suppressing unwanted Radio Frequencies (RF), in combination with SD interface compliant physical signaling
- Integrated biasing resistor networks to reduce the component count and to free up additional space on the Printed-Circuit Board (PCB) surface

2. SD-memory card electrical interface

Today many appliances use 2.7 V to 3.6 V operating mode. It enables the use of a fixed voltage interface and power supply to reduce cost and complexity of the control circuitry.

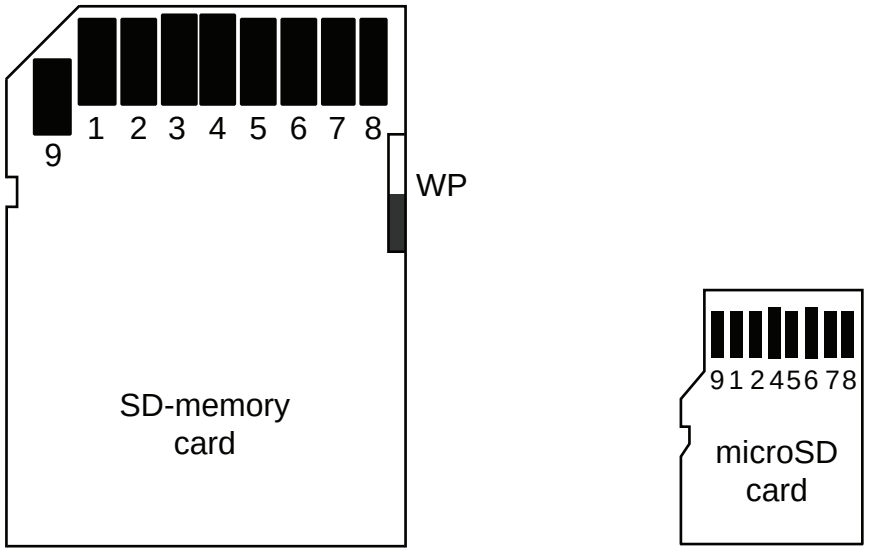
All further descriptions are related to this high-voltage range: 2.7 V to 3.6 V supply voltage operated interfaces.

A list of SD-memory card threshold levels for this range is listed in Table 2.

2.1 SD-memory card and microSD card interfaces

The SD-memory card exhibits nine pins (eight pins in case of microSD card) that are used to support electrical communication in two alternative communication protocols: SD and SPI (Serial Peripheral Interface). The host system can choose either one of these modes. The card detects which mode is requested by the host when the reset command is received and expects all further communication to be in the same communication mode (see Ref. 1).

Figure 1 shows an SD-memory card and microSD card with the interface pins.



microSD card pin numbering complies with Table 1

Fig 1. Shapes and interfaces of SD-memory card and microSD card (bottom view)

The SD bus includes the following signals:

- CLK: host to card clock signal
- CMD: bidirectional command/response signal
- DAT0 - DAT3: four bidirectional data signals
- V_{DD}, V_{SS1}, V_{SS2}: power and ground signals

The SPI bus includes the following signals:

- CS: host to card chip select signal
- CLK: host to card clock signal
- DataIn: host to card data signal
- DataOut: card to host data signal

The SPI interface uses 7 out of the SD 9 signals (DAT1 and DAT 2 are not used, DAT3 is the CS signal) of the SD bus.

Table 1 summarizes the pins of the SD card interface as used in SD and SPI modes:

Table 1. Interface pins of an SD-memory card and microSD card

Pin number	SD mode			SPI mode		
	Name	Type	Description	Name	Type	Description
1	CD/DAT3	I/O/PP	card-detect / data line (bit3)	CS	I	chip select (active low)
2	CMD	PP	command/response	DI	I	data in
3	GND1/VSS1	S	supply voltage ground	VSS	S	supply voltage ground
4	VDD	S	supply voltage		S	supply voltage
5	CLK	I	clock	SCLK	I	clock
6	GND2/VSS2	S	supply voltage ground		S	supply voltage ground
7	DAT0	I/O/PP	data line (bit 0)	DO	O/PP	data out
8	DAT1	I/O/PP	data line (bit 1)	RSV	-	reserved
9	DAT2	I/O/PP	data line (bit 2)	RSV	-	reserved

[1] I: input, O: output, PP: input / output using push-pull drivers, S: power supply.

The signals listed in Table 1 are directly provided from the SD-memory card itself. Additionally card holder can provide mechanical switches for card detection (CD) and write protection (WP) mechanisms.

2.2 Bus operation conditions

The minimum output level of the driving device and the input level of the receiving device are specified in Table 2 (see Ref. 1).

To decouple the SD-memory card interface specification from the signal-conditioning device (EMI filter, ESD protection, etc.), an intermediate signal threshold is specified in Table 3. This “EMI filter, card interface side” leveling is taken as a minimum requirement for an SD-memory card compliant interface conditioning device.

As ESD protection and EMI filter devices should be placed as close as possible to the contacts of the protected interface and integrate a major portion of the total bus capacitance C_{BUS}, they are responsible, as any other filter device, for most of the voltage drop.

Then the high-level and the low-level output voltages of the filter or conditioning device can be reduced (refer to V_{OH} and V_{OL} in Table 3) comparing to the output threshold levels (see Table 2) and still exceed the input voltage level requirements.

A detailed graphical overview of the different threshold levels at different positions of the signal path is depicted in Figure 2, starting with the driver output on the left side and ending with the receiving side on the right side of the drawing.

Three different threshold levels are shown in relation to each other in Figure 3, comparing the SD-memory card output, the NXP Semiconductors signal-conditioning device output and the SD-memory card input threshold levels.

Table 2. SD-memory card threshold levels for high-voltage range
Values taken from Ref. 1

Symbol	Parameter	Condition	Min	Max	Unit
V_{SD}	SD-memory card supply voltage		2.7	3.6	V
V_{OH}	high-level output voltage	I_{OH} = −100 μA; V_{SD} = 2.7 V	0.75 × V_{SD}	-	V
V_{OL}	low-level output voltage	I_{OL} = 100 μA; V_{SD} = 2.7 V	-	0.125 × V_{SD}	V
V_{IH}	high-level input voltage		0.625 × V_{SD}	-	V
V_{IL}	low-level input voltage		-	0.25 × V_{SD}	V
t_{Pup}	power up time	0 V ≤ V_{SD} ≤ 2.7 V	-	250	ms

Table 3. SD-memory card operating conditions

Symbol	Parameter		Min	Max	Unit
V_{SD}	SD-memory card supply voltage		2.7	3.6	V
I_{DD}	supply current in high-speed mode		-	200	mA
V_{OH}	high-level output voltage	[1][3]	0.7 × V_{SD}	-	V
V_{OL}	low-level output voltage	[2][3]	-	0.2 × V_{SD}	V
C_L	load capacitance		-	40	pF
C_{CARD}	SD-memory card signal line capacitance		-	10	pF
$C_{HOST + BUS}$	capacitance of host interface and signal bus		-	30	pF
R_{CMD}	external pull-up resistor value to prevent bus floating		10	100	kΩ
R_{DAT}	external pull-up resistor value to prevent bus floating; DAT0, DAT1 and DAT2		10	100	kΩ
R_{DAT3}	SD-memory card internal pull-up resistor value DAT3/CD pin only		10	90	kΩ
L_{ch}	single line inductance		-	16	nH

[1] SD-memory card specification is: V_{OH} minimum is 0.75 × V_{SD} and V_{IH} minimum is 0.625 × V_{SD} in Ref. 1; NXP Semiconductors V_{OH} minimum is 0.7 × V_{SD}.

[2] SD-memory card specification is: V_{OL} maximum is 0.125 × V_{SD} and V_{IL} maximum is 0.25 × V_{SD} in Ref. 1; NXP Semiconductors V_{OL} minimum is 0.2 × V_{SD}.

[3] 20 % to 70 % limits are chosen also to cover MMC specification.

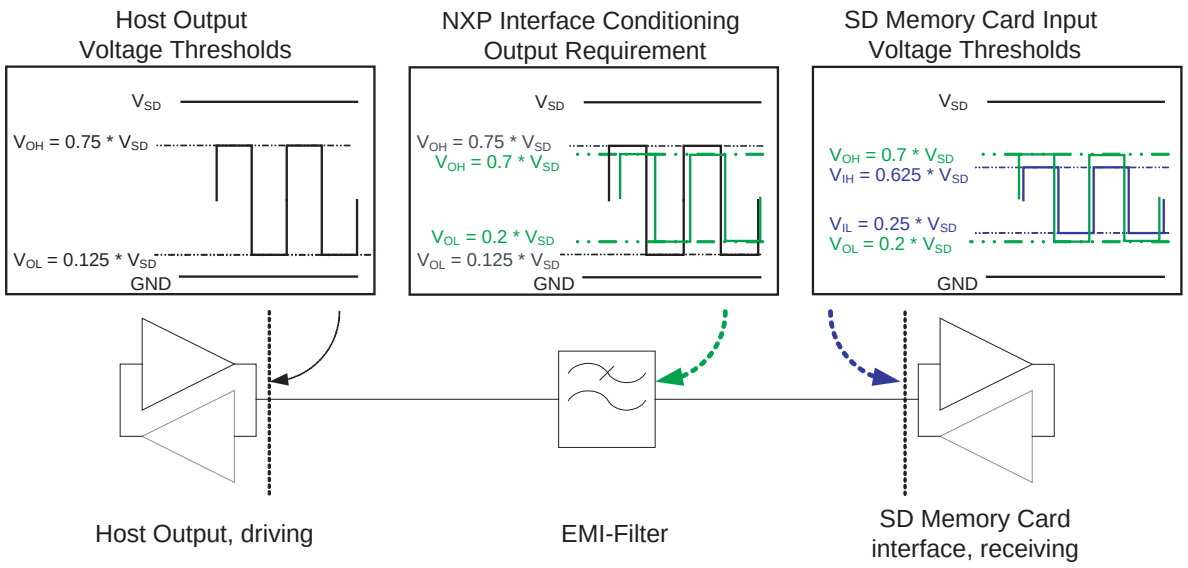


Fig 2. Threshold voltage levels along the signal path

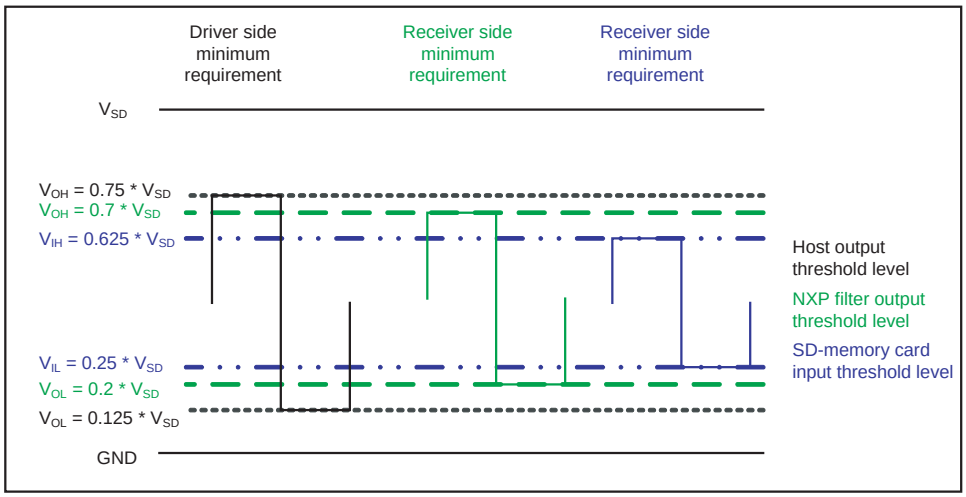


Fig 3. Threshold voltage levels, output levels versus input levels

All further considerations are based on a chosen 20 % and 70 % threshold respectively, related to the SD-memory card supply voltage V_{SD}, as specified in Table 3, unless otherwise indicated. These relative voltage levels also simplify an alignment with the MMC specification.

2.3 SD-memory card bus timing conditions

The SD-memory card interface has different timing requirements for the default mode and for the high-speed mode up to 50 MHz clock frequency.

Special attention should be paid to the clock signal rise time and fall time requirements (3 ns maximum).

All NXP Semiconductors devices support both the high-speed mode and the default mode requirements. Since high-speed mode requirements contain default mode requirements, only the former considered in this document.

Table 4. SD-memory card timing conditions (high-speed mode)[1]

Symbol	Parameter	Condition		Min	Max	Unit
f_{PP}	operating clock frequency			0	50	MHz
t_r	rise time	20 % to 70 % of V_{DD}	[2]	-	3	ns
t_f	fall time	70 % to 20 % of V_{DD}	[2]	-	3	ns

[1] Other timing parameters such as hold time, set-up time, high-level and low-level are dependent on the host and SD-memory card interface and not significantly influenced by the NXP Semiconductors interface conditioning devices.

[2] Values refer to V_{OH} and V_{OL} specified for the EMI filter output.

2.4 Capacitive load at the interface conditioning device output

NXP Semiconductors devices, such as IP4352CX24, have rise time and fall time requirements specified similarly to the data shown in Table 5.

Table 5. Time domain response

T_{amb} = 25 °C, V_{CC} = 1.8 V, V_{BAT} = 3.5 V, V_{SD} = 2.9 V; 20 % to 70 % LOW-to-HIGH limits.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_r, t_f	rise time, fall time	Z_{load} = 20 pF || 100 kΩ	-	1.5	2.5	ns
t_r, t_f	rise time, fall time	Z_{load} = 40 pF || 100 kΩ	-	2.7	3.6	ns

The following abbreviations are used:

- Z_{load}: capacitive load representing C_{PCB2} + C_{HOLD} + C_{CARD} in NXP Semiconductors data sheets
- C_{PCBx}: PCB trace capacitance
- C_{HOLD}: card holder capacitance
- C_{BUS}: total single bus channel capacitance excluding the SD-memory card
- C_L: total single bus channel capacitance including the SD-memory card

For further details refer to Figure 4.

In this specification, Z_{load} represents C_{CARD} and a part of C_{BUS}.

Figure 4 depicts the various basic capacitances of the signal path summing up to:

$$C_{BUS} = C_{PCB1} + C_{CH/2} + C_{CH/2} + C_{PCB2} + C_{HOLD} \leq 30 \text{ pF}$$

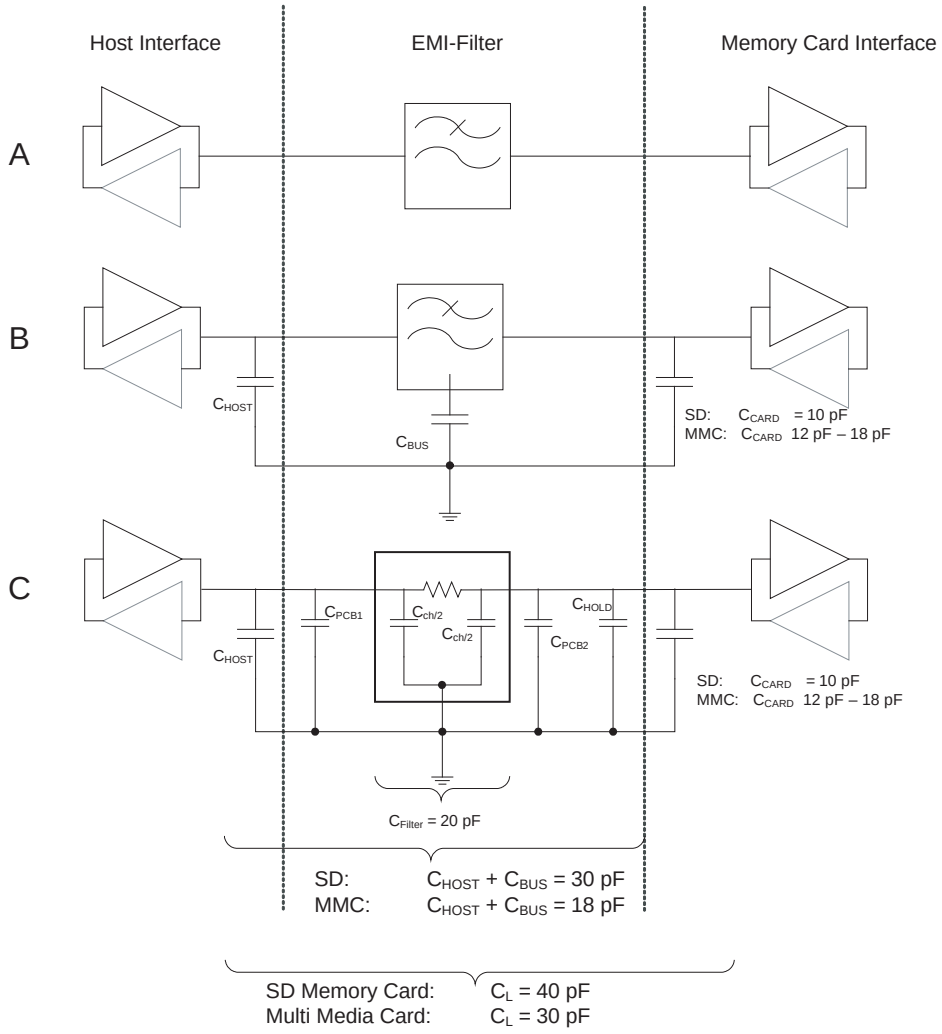
Note that a significant portion (NXP Semiconductors assumption 20 % to 30 %) of the SD-memory cards available on the market today have a card capacitance (C_{CARD}) of more than 10 pF.

According to the SD-memory card specification (refer to chapter 6.5.5 of Ref. 1), the total channel capacitance C_L is defined as:

$$C_L = C_{BUS} + C_{CARD} \leq 40 \text{ pF}$$

Assuming that state-of-the-art host interfaces show a capacitance of $C_{HOST} \leq 4$ pF and the NXP Semiconductors interface-conditioning devices add a capacitance in the range of $C_{CH} = 2 \times C_{CH/2} \leq 20$ pF , a capacitance of $C_{PCB1} + C_{PCB2} + C_{HOLD} \leq 6$ pF is left for the routing on the PCB and the card holder, which can already amount to 3 pF to 5 pF.

Due to Z_{load} representing a lumped capacitance of 20 pF in addition to the filter channel capacitance, it is obvious that the rise time and fall time requirement of 3 ns can be easily fulfilled.



Note: C_{BUS} is a lumped representative of the total channel capacitances of PCB, interface conditioning and card holder.

A. Basic simplified memory card signal channel

B. More detailed level

C. Detailed memory card signal channel showing the relevant capacitive contributors

Fig 4. Basic signal channel depicted in three different detail levels

2.5 SD-memory card-detect mechanism

To detect an SD-memory card two different mechanisms can be used.

The conventional detection mechanism uses a mechanical switch in the card holder. The other mechanism is based on the pull-up resistor integrated into the SD-memory card. This resistor is connected to the DAT3/CD pin (where CD is card-detect). A detailed schematic showing both detection mechanisms is depicted in Figure 6.

If MMC and SD-memory card are used in the same holder, only the mechanical switch-based card detection can be used.

In contrast to the SD-memory card specification, the MMC specification does not specify any internal pull-up resistors for an electrical card detection mechanism.

Additionally, the SD-memory card specification gives clear priority to the mechanical switch detection method.

3. MMC electrical interface

Advanced appliances optimized for low-power consumption can operate MMCs at two different supply voltages with small disadvantage of the increased control effort and a selectable supply voltage. A number of MMC threshold levels for the high-voltage range are listed in Table 6.

3.1 Bus operating conditions

The minimum output level of the driving device, together with the receiving device input level is specified in Table 6 (see Ref. 2 “Multi Media Card System Specification version 4.3, JESD84-A43, November 2007”).

Similar considerations as shown in Section 2.3 “SD-memory card bus timing conditions”, are also applicable to the MMC.

For high-voltage operation mode the threshold conditions are identical to the SD-memory card conditions. Therefore both can be operated if connected to the same physical interface as long as the electrical card detection mechanism is not used.

Table 6. MMC threshold levels
(values taken from Ref. 2)

Symbol	Parameter	Condition	Min	Max	Unit
V_{MMC}	MMC supply voltage				
	high-voltage range		2.7	3.6	V
	low-voltage range	[1]	1.7	1.95	V
Push-pull mode bus signal level for high-voltage MMC					
V_{OH}	high-level output voltage	I_{OH} = −100 μA; V_{MMCmin}	0.75 × V_{MMC}	-	V
V_{OL}	low-level output voltage	I_{OL} = 100 μA; V_{MMCmin}	-	0.125*V_{MMC}	V
V_{IH}	high-level input voltage		0.625 × V_{MMC}	V_{MMC} + 0.3	V
V_{IL}	low-level input voltage		V_{SS} − 0.3	0.25 × V_{MMC}	V
Push-pull mode bus signal level for the dual voltage MMC in 1.70 V to 1.95 V mode for high-voltage specified above for high-voltage MMC					
V_{OH}	high-level output voltage	I_{OH} = −100 μA; V_{MMCmin}	V_{MMC} − 0.2	-	V
V_{OL}	low-level output voltage	I_{OL} = 100 μA; V_{MMCmin}	-	0.2	V
V_{IH}	high-level input voltage		0.7 × V_{MMC}	V_{MMC} + 0.3	V
V_{IL}	low-level input voltage		V_{SS} − 0.3	0.3 × V_{MMC}	V

[1] Low-voltage levels are part of the dual voltage range card specification including high-voltage range. The voltage range from 1.95 V to 2.7 V is not specified.

Compared to the SD-memory card, the MMC bus is limited to a maximum of 30 pF (SD-memory card is 40 pF maximum).

Two basic differences between MMC and SD-memory card are:

- minimum resistor value of R_{CMD} which is less than a half of the specified minimum of the SD-memory card specification
- DAT0 to DAT7 pull-up resistor values, starting at 50 kΩ instead of 10 kΩ in the SD-memory card specification (see Table 3).

The Embedded Multi Media Card (eMMC) contains internal pull-up resistors at the pins DAT1 to DAT7 to prevent floating of unconnected data lines (see Ref. 2). All other MMCs do not contain any pull-up resistors to prevent bus floating.

Table 7. MMC operating conditions

Symbol	Parameter		Min	Max	Unit
C_L	total bus capacitance for each signal line		-	30	pF
C_{CARD}	single card signal line capacitance				
	C_{MICRO}		-	12	pF
	C_{MOBILE}		-	18	pF
	C_{BGA}		-	12	pF
R_{CMD}	CMD pull-up resistor value		4.7	100	kΩ
$R_{DAT7\text{-}DAT0}$	external DAT7 to DAT0 pull-up resistor value	[1]	50	100	kΩ
R_{intDAT}	eMMC internal DAT7 to DAT0 pull-up resistor value		50	150	kΩ
L_{ch}	maximum signal line capacitance		-	16	nH

[1] except eMMC

3.2 Bus timing conditions

The MMC interface has different timing requirements for the default mode and for the high-speed mode running up to 52 MHz. Special attention should be paid to the clock signal rise and fall time requirement (3 ns maximum) which is similar to the high-voltage range cards and the SD-memory card timing conditions (see Table 4).

Also, a reduced clock speed of up to 26 MHz can be used with these cards to save power in appliances that do not require high data rates.

All NXP Semiconductors devices support both the high-speed mode and the default mode requirements. Since high-speed mode requirements contain default mode requirements, only the former considered in this document.

Table 8. MMC timing conditions (high-speed mode)[1]

Symbol	Parameter		Min	Max	Unit
f_{PP}	operating clock frequency		0	52	MHz
t_{rise}	high-speed mode clock rise time	[2]	-	3	ns
t_{fall}	high-speed mode clock fall time		-	3	ns

[1] Other timing parameters such as hold time, set-up time, high-time and low-time depend on the host and MMC interface. They are not significantly influenced by NXP Semiconductors interface conditioning devices.

[2] Refer to Ref. 2, chapter 12.7.1 for further details.

3.3 Capacitive load at the interface conditioning device output

Refer to Section 2.4 for a detailed overview and calculation.

The drawing depicted in Figure 4 shows that it is difficult to build an MMC specification-compliant bus system that includes high-level ESD protection and EMI filtering. Nevertheless, most implementations used are related to the SD-memory card application and use only slightly higher total channel capacitances, reaching the SD specification for the value of $C_{HOST} + C_{BUS}$.

4. SD-memory card and MMC interface comparison

A short summary of the main electrical interface parameters of the SD-memory card versus the MMC are listed in the following table:

Table 9. SD-memory card and MMC electrical parameters comparison

Symbol	Parameter		SD-memory card	MMC	Unit
$V_{sd/MMC}$	memory card supply voltage				
	high-voltage range		2.7 - 3.6	2.7 - 3.6	V
	low-voltage range		-	1.7 - 1.95	V
f_{PP}	maximum operating clock frequency		50	52	MHz
t_{rise}	maximum high-speed mode clock rise time		3	3	ns
t_{fall}	maximum high-speed mode clock fall time		3	3	ns
C_L	maximum total bus capacitance for each signal line		40	30	pF
C_{CARD}	maximum capacitance single card signal line		10	-	pF
	C_{MICRO}		-	12	pF
	C_{MOBILE}		-	18	pF
	C_{BGA}		-	12	pF
R_{CMD}	CMD pull-up resistor value		10 - 100	4.7 - 100	kΩ
$R_{DAT7(3)-0}$	external DAT7(3) - DAT0 pull-up resistor value to prevent bus floating	[1]	10 - 100	50 - 100	kΩ
$R_{intDAT3}$	eMMC internal DAT7- DAT0 pull-up resistor value		-	50 - 150	kΩ
	DAT3/CD (SD)		10 - 90	-	kΩ
L_{ch}	maximum signal line inductance		16	16	nH

[1] except eMMC

5. Passive ESD protection and EMI filter devices

NXP Semiconductors offers a wide range of devices for the interface conditioning of the SD-memory card and/or MMC interface. The product range covers EMI filters and ESD protection devices, such as IP4252CZ12-6 or IP4252CZ16-8.

These devices can be also used for Serial Peripheral Interface (SPI)-based interface operation modes. In this case 4-channel devices can be used although this is not the preferred method of data exchange with SD-memory cards due to the lower speed and single bit access.

An overview is given in Table 10 and a detailed description is given in the next chapters. These filter devices are available in leadless plastic packages (DFN) and Wafer Level Chip Size Packages (WLCSP).

Even though the MMC and SD-memory card specifications state exact minimum and maximum values for the various internal and external pull-up and pull-down resistors, a majority of implemented interfaces in available appliances do not follow these recommendations. This is especially true for the minimum CMD signal pull-up resistor value, which is often undercut to guarantee a sufficiently short rise time in an open-drain communication mode. The minimum values of the external pull-up resistor values of the MMC specification are also sometimes replaced by values from the SD-memory card specification range.

Therefore most NXP Semiconductors devices can be used in both interface applications, MMCs and SD-memory cards, even though data sheets are referring to just one interface type.

Modern memory cards typically support interfaces which are slightly out of the related general interface specification.

Table 10. SD-memory card and MMC interface devices overview

Product name	Device type	Additional features	Number of filter channels	Package type and size
Memory card interface ESD protection and EMI filter devices with integrated biasing (pull-up-/pull-down) resistors, ESD protection level > 15 kV contact, far exceeding the IEC61000-4-2, level 4 (8 kV contact, 15 kV air)				
IP4340CX15	ESD protection and EMI filter		6	CSP, 0.4 mm pitch $1.56 \times 1.56 \times 0.47$ mm^3
IP4350CX24	ESD protection and EMI filter	including WP and CD	6 (+5) [1]	CSP, 0.4 mm pitch $2.01 \times 2.02 \times 0.61$ mm^3
IP4352CX24	ESD protection and EMI filter	including WP and CD	6 (+5) [1]	CSP, 0.4 mm pitch 2.01×2.02 mm^2
IP4357CX17	ESD protection and EMI filter			CSP, 0.4 mm pitch (staggered) 1.1×2.4 mm^2
Memory card interface ESD protection and EMI filter devices, ESD protection level according IEC61000-4-2, level 4 (8 kV contact, 15 kV air discharge)				
IP4252CZ8-4	ESD protection and EMI filter		4	DFN, 0.4 mm pitch $1.35 \times 1.7 \times 0.5$ mm^3
IP4252CZ12-6	ESD protection and EMI filter		6	DFN, 0.4 mm pitch $1.35 \times 2.5 \times 0.5$ mm^3
IP4252CZ16-8	ESD protection and EMI filter		8	DFN, 0.4 mm pitch $1.35 \times 3.3 \times 0.5$ mm^3

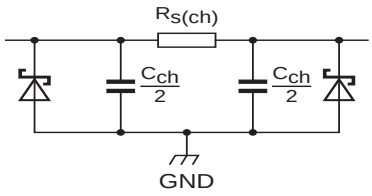
[1] Numbers in brackets represent additional channels such as pull-up and pull-down channels, WP and CD that are not required for the basic data communication.

5.1 ESD protection EMI filter devices in plastic package IP4252CZ8-4, IP4252CZ12-6, IP4252CZ16-8

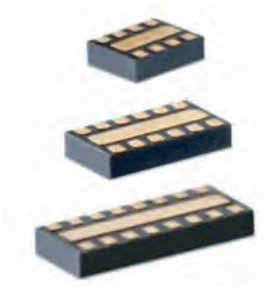
If pull-up resistors are integrated in the host interface, then ESD protection and EMI filtering devices such as IP4252 family are recommended. These devices are available in 4-, 6- and 8-channel versions: IP4252CZ8-4, IP4252CZ12-6 andIP4252CZ16-8.

They all contain an RC-based pi-filter (also called Capacitor-Resistor-Capacitor (CRC) filter) consisting of two ESD protection diodes, acting as filter capacitors, and a serial channel resistor connected between the cathodes of these diodes.

Single filter channel schematic is shown in Figure 5 (left side) together with DFN plastic packages (right side). These packages have 0.4 mm contact pitch and 0.5 mm maximum package height.



a. Schematic view for a single channel



b. IP4252CZ8-4, IP4252CZ12-6 and IP4252CZ16-8 package (top to bottom)

Fig 5. IP4252: schematic view and package photograph

Table 11. IP4252 parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		–0.5	-	+5.6	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; all pins to ground				
		contact discharge	–8	-	+8	kV
		air discharge	–15	-	+15	kV
$R_{s(ch)}$	channel series resistance		32	40	48	Ω
C_{ch}	channel capacitance $= 2*\frac{C_{ch}}{2}$	$V_{bias(DC)}$ = 0 V, f = 100 kHz	-	18	-	pF
		$V_{bias(DC)}$ = 2.5 V, f = 100 kHz	-	12	-	pF

[1] Total channel capacitance is distributed between both ports of the channels, see Figure 5.

Due to the integrated symmetrical pi-filter structure (often referred to as CRC structure) all NXP Semiconductors IP4252 devices offer a direction-independent and symmetrical ESD protection as well as a direction-independent and symmetrical EMI filter performance.

Integrated pi-filter structures provide very low ESD clamping voltage compared to single diode ESD protection implementations and/or devices.

5.1.1 Application details of IP4252CZ12-6 and IP4252CZ16-8

Figure 6 shows a typical application of IP4252CZ12-6 and/or IP4252CZ16-8 in an SD-memory card interface including both options for card detection. The grey-colored components are optional and depend on the exact details of the interface implementation. Especially with respect to the card-detect mechanism, either using a mechanical switch in the card holder (preferred, see Ref. 1) or using integrated pull-up resistor at pin DAT3/CD in combination with selectable pull-down / pull-up resistors. The exact resistor values have to be aligned with all details described in Ref. 1.

This schematic does not include details concerning card-supply and typical power-supply decoupling capacitors.

For the basic SD-memory card operation an IP4252CZ12-6 and 4 pull-up resistors (10 kΩ to 100 kΩ) are sufficient for the digital data transmission from and to the SD-memory card. MMCs require higher pull-up resistor values starting at 50 kΩ. The card detection mechanism has to be implemented using a CD channel as shown in Figure 7, based on a mechanical card detection switch, in case SD-memory card and MMC are used with the same interface.

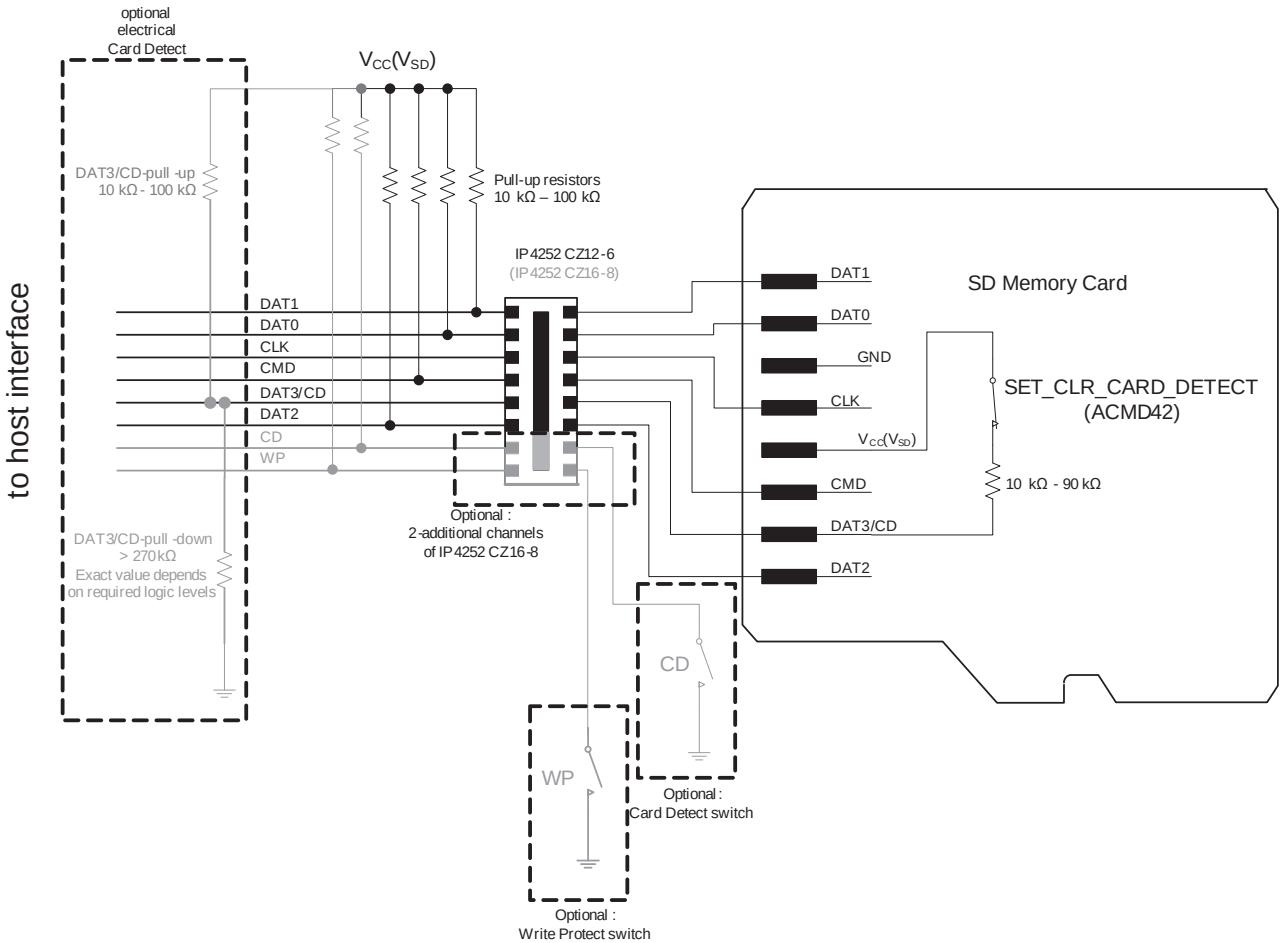


Fig 6. Application diagram of IP4252CZ12-6 and IP4252CZ16-8 in a SD-memory card interface

The implementation of write protection contact is only possible in applications supporting standard-size SD-memory cards. Smaller form-factor versions such as miniSD or microSD do not support this feature. In case the mechanical slider mechanism of the standard-size SD-memory card is used, a pull-up resistor is connected to the host supply and a mechanical contact to ground. This contact is open until a WP slider is closing it (mechanical adaptors converting a micro or mini SD-memory card into a standard SD-card size typically do not support this feature).

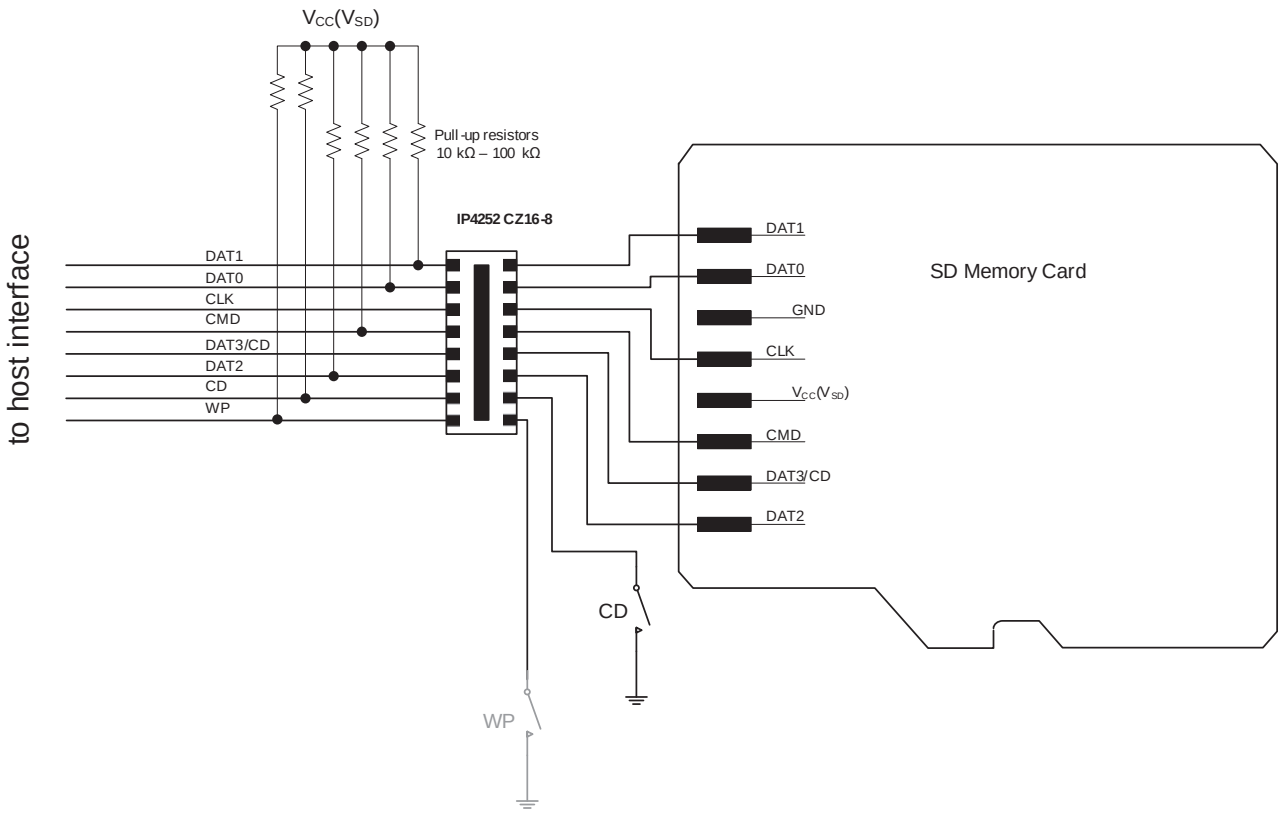


Fig 7. Application diagram of IP4252CZ16-8 using a mechanical card-detect switch

In case a mechanical card detection switch is not possible to apply (for example, due to size constraints for the card holder), an electrical card detection can be used but only for an SD-memory card interface.

After power-up DAT3/CD is connected to a 50 kΩ (nominal value, specified range is 10 kΩ to 90 kΩ) pull-up resistor inside the card. In case DAT3/CD is connected to a high-ohmic pull-down resistor, the connected host can detect a logic level change from low to high level[1]. The card internal pull-up resistor should be disconnected during regular data transmission with SET_CLR_CARD_DETECT (ACMD42) command.

1. It is recommended that pull-down resistor is >270 kΩ to fulfill the logic voltage level requirements. The exact value depends on the logic level requirements.

Figure 8 shows a diagram for this implementation.

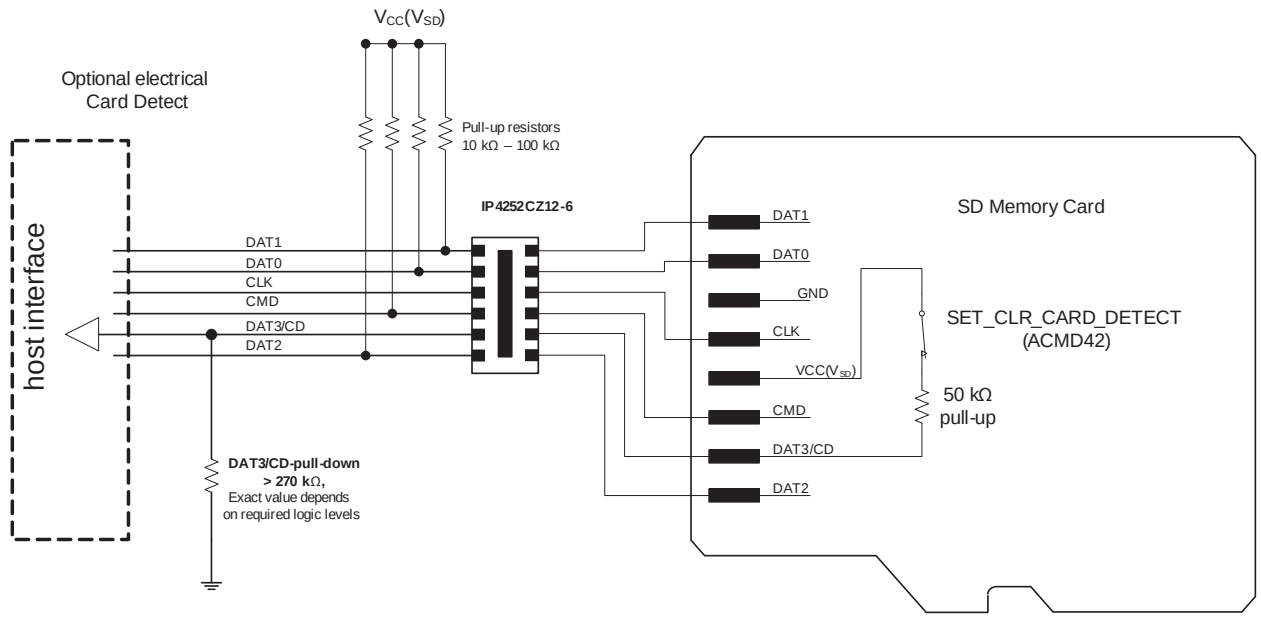


Fig 8. Application diagram of IP4252CZ12-6 using electrical card detection

For the latest 8-bit MMC interface, 10 channels have to be ESD-protected and EMI-filtered. A combination of IP4252CZ8-4 (4-channel) and IP4252CZ12-6 (6-channel) is best-matching filter combination to cover the full interface (see Figure 9).

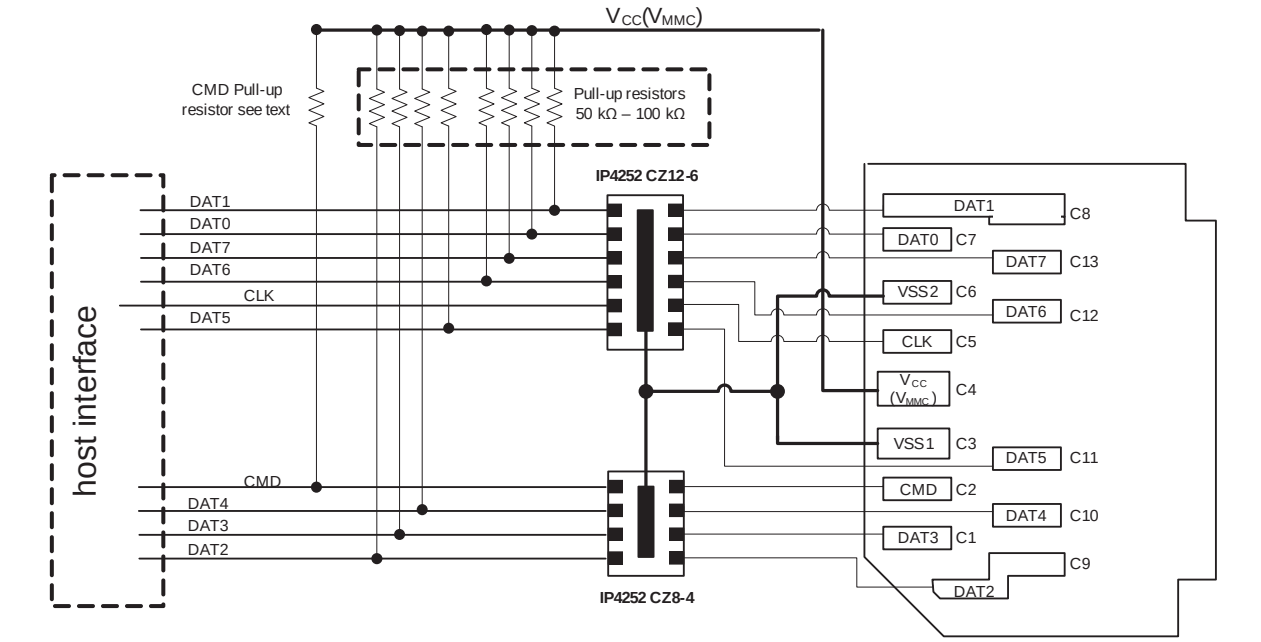


Fig 9. Application schematic diagram of IP4252CZ12-6 and IP4252CZ8-4 in an 8-bit MMC interface

5.2 MicroSD card ESD protection and EMI filter device IP4340CX15

The IP4340CX15 is a 6-channel microSD card ESD protection and EMI filter device with 5 additionally integrated pull-up resistors in a tiny 0.4 mm ball pitch CSP.

The only channel without a pull-up resistor is the clock channel (see Figure 10). Due to the pull-up resistor implementation, the electrical card detection method cannot be used. Detection using a mechanical switch is mandatory.

The maximum filter channel capacitance is 14 pF which makes the device suitable to work in high clock speed applications, too.

Table 12. IP4340CX15 electrical parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		–0.5	-	+5.0	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4, pins on microSD card side				
		contact discharge	–15	-	+15	kV
		air discharge	–15	-	+15	kV
$R_{s(ch)}$	channel series resistance	R1 to R6	36	40	44	Ω
R_{pu}	pull-up resistance	R9 to R12	40	50	60	kΩ
		R13	12	15	18	kΩ
C_{line}	line capacitance	including diode capacitance; V_I = 0 V; f = 1 MHz; V_{CC} = GND	8	11	14	pF

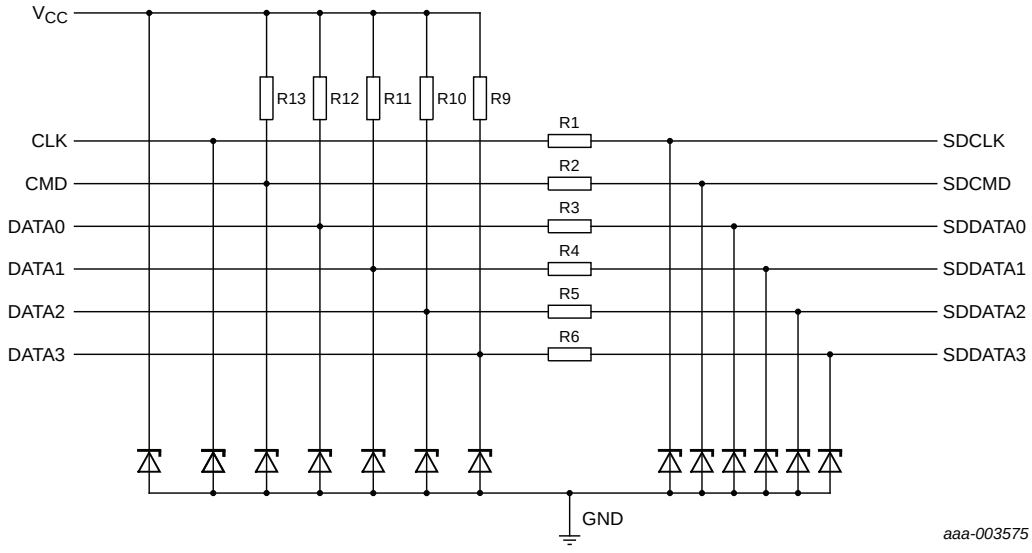


Fig 10. Schematic view for IP4340CX15

5.3 Very highly integrated memory card interface device IP4350CX24

The IP4350CX24 demonstrates the highest level of integration, consisting of ESD protection, EMI filter and biasing resistors in a passive device. As the package is a 0.4 mm pitch CSP type, the total device size is only 1.95 × 2.11 mm^2.

This device fully supports high-speed memory card interfaces working with clock speed up to 52 MHz.

A special diode structure using a rail-to-rail (also known as “crow-bar”) diode concept on the high-level ESD protection side in combination with single diodes on the low-level ESD protection side guarantee a balanced distribution of the channel capacitance. This leads to symmetrical EMI filter performance which is independent from the read/write direction.

IP4350CX24 supports electrical card detection of an SD-memory card using the pins DAT3_PD and R21 connected to GND. Figure 11 shows detailed schematic with the driver and control circuitry required to use electrical card detection. Electrical card-detect is available as long as the “control” inverter output is low and 'driver_pu' is 3-stated, so R21 is acting as a pull-down to GND.

If normal operation is needed, the “control” inverter drives a high signal to enable the 'driver _pu' buffer, drives a high signal at R11 and also drives R21 to a high level to avoid any unnecessary quiescent current.

The maximum voltage at the pin to the host interface may exceed the host supply voltage as it is derived from: $V_{SD} \times (R_{11} / (R_{11} + R_{DAT3/CDpu}))$. In this case a voltage tolerant input has to be selected.

If electrical card detection is not required, DAT3_PU (R11) should be connected to V_{SD} instead.

Since the CMD line is connected to the pull-up resistor R15, which is typically 15 kΩ, IP4350CX24 can also be used in combination with an MMC. The MMC can be initialized using a 400 kHz open-drain mode.

The channels for the mechanical WP, CD and the combined WP+CD require an additional pull-up resistor which is not integrated. Often pull-up resistors integrated into the GPIOs of the host processor are used for this purpose as they can be switched off after detection.

The lower CMD pull-up resistor value and lower total line capacitance value make the IP4350CX24 an excellent match for MMC interfaces in case a compliance with the latest standard specification is mandatory.

Three additional channels support any configuration of CD and WP switches for the various memory card holders (see Figure 11).

The most important electrical parameters are listed in Table 13.

Table 13. IP4350CX24 electrical parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		−0.5	-	+5.0	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4 SDxxx pins to GND				
		contact discharge	−8	-	+8	kV
		air discharge	−15	-	+15	kV
$R_{s(ch)}$	channel series resistance	R1 to R9	12	15	18	Ω
		R11 to R14	35	50	65	kΩ
		R15	3.29	4.7	6.11	kΩ
		R21	329	470	611	kΩ
C_{ch}	channel capacitance	including diode capacitance; V_I = 0 V; f = 100 kHz				
		each data channel from SD card to I/O interface	-	8.8	-	pF
		CLK channel	-	7.8	-	pF

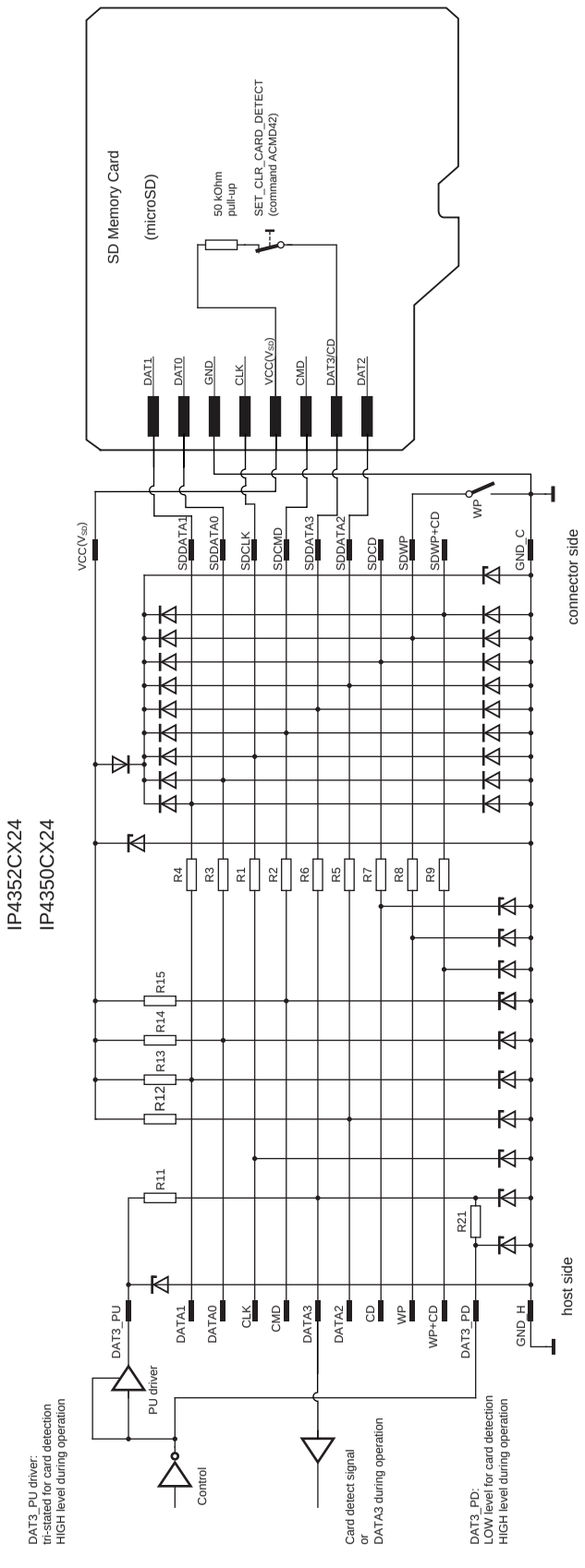


Fig 11. IP4350CX24 connected to an SD-memory card using electrical card-detect

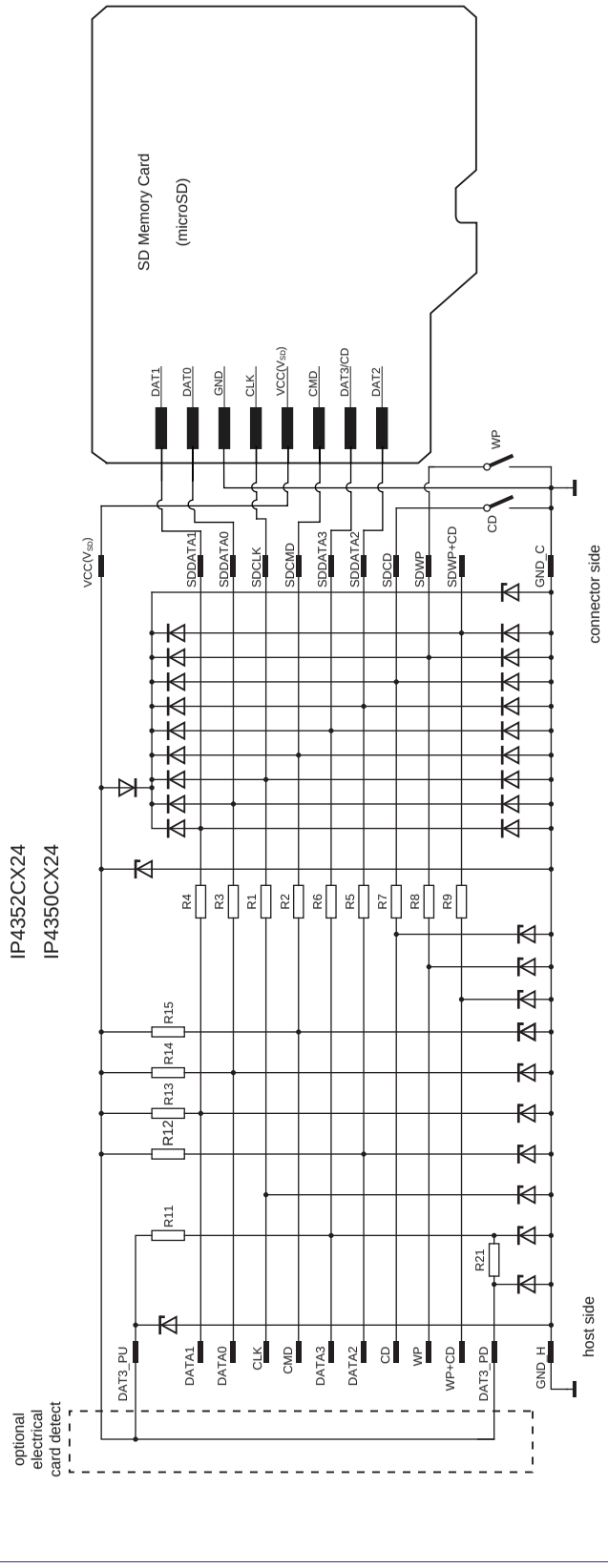


Fig 12. IP4350CX24 connected to an SD-memory card using mechanical card-detect

6. Conclusion

NXP Semiconductors offers a comprehensive portfolio of SD-memory card and MMC compatible interface conditioning and protection devices.

These devices are optimized for compliance with their respective memory card interface in terms of channel capacitance, serial resistance and biasing resistor values.

Passive devices explained in this document protect from destruction from system level ESD and also prevent disturbance of, for example wireless interfaces, from the harmonics of the digital memory interfaces. Integrated biasing resistors contribute to gain the maximum space savings comparing to discrete solutions.

All devices presented support a simple PCB layout, reduce the risk of EMI due to complex layout of scattered discrete components and allow to minimize compliance testing.

The high integration level and the final test of each device before shipment also improve the overall quality. The integrated protection and filter components reduce the number of individual components, solder joints and pick-and-place processes.

7. References

[1] SD specifications, part 1, Physical Layer Specification version 2.00, May 9, 2006

[2] Multi Media Card System Specification version 4.3, JESD84-A43, November 2007

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