



# AN10441

## Level shifting techniques in I<sup>2</sup>C-bus design

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Application note

### Document information

Information	Content
Keywords	I <sup>2</sup> C-bus, level shifting
Abstract	Logic level shifting may be required when interfacing legacy devices with newer devices that use a smaller geometry process. For bidirectional bus systems like the I <sup>2</sup> C-bus, such a level shifter must also be bidirectional, without the need of a direction control signal. The simplest way to solve this problem is by connecting a discrete MOSFET to each bus line.

## 1. Introduction

Present technology processes for integrated circuits with clearances of 0.5  $\mu\text{m}$  and less limit the maximum supply voltage and consequently the logic levels for the digital I/O signals. To interface these lower voltage circuits with existing 5 V devices, a level shifter is needed. For bidirectional bus systems like the I<sup>2</sup>C-bus, such a level shifter must also be bidirectional, without the need of a direction control signal. The simplest way to solve this problem is by connecting a discrete MOSFET to each bus line.

## 2. Bidirectional level shifter for Fast-mode and Standard-mode I<sup>2</sup>C-bus systems

In spite of its surprising simplicity, such a solution not only fulfils the requirement of bidirectional level shifting without a direction control signal, it also:

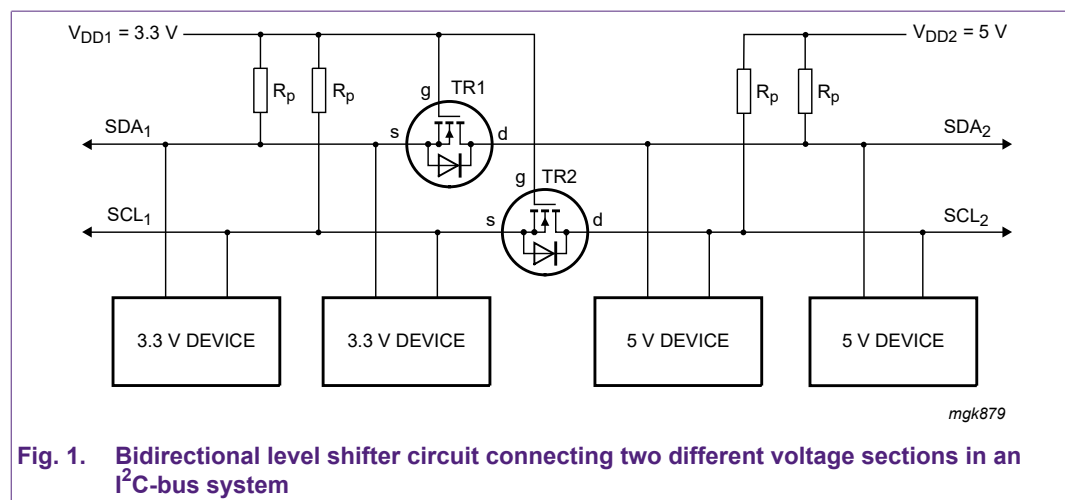
- Isolates a powered-down bus section from the rest of the bus system
- Protects the 'lower voltage' side against high voltage spikes from the 'higher-voltage' side.

The bidirectional level shifter can be used for both Standard-mode (up to 100 kbit/s) or in Fast-mode (up to 400 kbit/s) I<sup>2</sup>C-bus systems. It is not intended for Hs-mode systems, which may have a bridge with a level shifting possibility.

### 2.1. Connecting devices with different logic levels

Different voltage devices could be connected to the same bus by using pull-up resistors to the supply voltage line. Although this is the simplest solution, the lower voltage devices must be 5 V tolerant, which can make them more expensive to manufacture. By using a bidirectional level shifter, however, it is possible to interconnect two sections of an I<sup>2</sup>C-bus system, with each section having a different supply voltage and different logic levels. Such a configuration is shown in Fig. 1. The left 'low-voltage' section has pull-up resistors and devices connected to a 3.3 V supply voltage; the right 'high-voltage' section has pull-up resistors and devices connected to a 5 V supply voltage. The devices of each section have I/Os with supply voltage related logic input levels and an open-drain output configuration.

The level shifter for each bus line is identical and consists of one discrete N-channel enhancement MOSFET; TR1 for the serial data line SDA and TR2 for the serial clock line SCL. The gates (g) have to be connected to the lowest supply voltage  $V_{DD1}$ , the sources (s) to the bus lines of the 'lower-voltage' section, and the drains (d) to the bus lines of the 'higher-voltage' section. Many MOSFETs have the substrate internally connected with its source, if this is not the case, an external connection should be made. Each MOSFET has an integral diode (n-p junction) between the drain and substrate.



**Fig. 1. Bidirectional level shifter circuit connecting two different voltage sections in an I<sup>2</sup>C-bus system**

### 2.1.1. Operation of the level shifter

The following three states should be considered during the operation of the level shifter:

1. No device is pulling down the bus line. The bus line of the 'lower-voltage' section is pulled up by its pull-up resistors  $R_p$  to 3.3 V. The gate and the source of the MOSFET are both at 3.3 V, so its  $V_{GS}$  is below the threshold voltage and the MOSFET is not conducting. This allows the bus line at the 'higher-voltage' section to be pulled up by its pull-up resistor  $R_p$  to 5 V. So the bus lines of both sections are HIGH, but at a different voltage level.
2. A 3.3 V device pulls down the bus line to a LOW level. The source of the MOSFET also becomes LOW, while the gate stays at 3.3 V.  $V_{GS}$  rises above the threshold and the MOSFET starts to conduct. The bus line of the 'higher-voltage' section is then also pulled down to a LOW level by the 3.3 V device via the conducting MOSFET. So the bus lines of both sections go LOW to the same voltage level.
3. A 5 V device pulls down the bus line to a LOW level. The drain-substrate diode of the MOSFET the 'lower-voltage' section is pulled down until  $V_{GS}$  passes the threshold and the MOSFET starts to conduct. The bus line of the 'lower-voltage' section is then further pulled down to a LOW level by the 5 V device via the conducting MOSFET. So the bus lines of both sections go LOW to the same voltage level.

The three states show that the logic levels are transferred in both directions of the bus system, independent of the driving section. State 1 performs the level shift function. States 2 and 3 perform a 'wired-AND' function between the bus lines of both sections as required by the I<sup>2</sup>C-bus specification.

Supply voltages other than 3.3 V for  $V_{DD1}$  and 5 V for  $V_{DD2}$  can also be applied, e.g., 2 V for  $V_{DD1}$  and 10 V for  $V_{DD2}$  is feasible. In normal operation  $V_{DD2}$  must be equal to or higher than  $V_{DD1}$  ( $V_{DD2}$  is allowed to fall below  $V_{DD1}$  during switching power on/off).

## 3. Abbreviations

Table 1. Abbreviations

Acronym	Description
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor

## 4. Revision history

Table 2. Revision history

Rev	Date	Description
AN10441 v.2	20200210	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>
AN10441 v.1	20070618	Initial version

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