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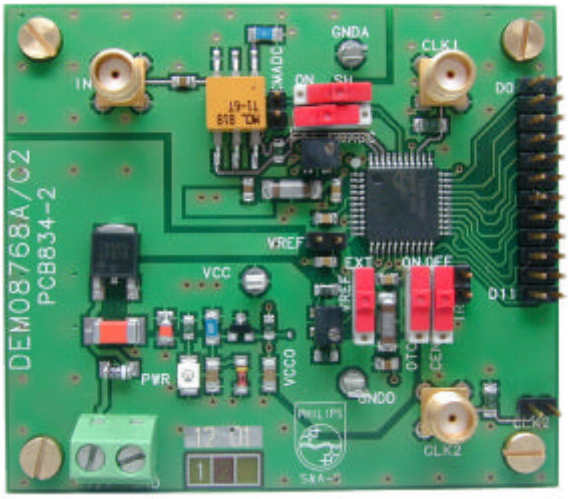
# APPLICATION NOTE

## - TDA8768A/C2 -
## 12-BIT HIGH-SPEED A/D CONVERTER DEMONSTRATION BOARD

**AN/01029**

***VERSION 2.1***

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# APPLICATION NOTE

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## 12-BIT HIGH-SPEED A/D CONVERTER
## DEMONSTRATION BOARD

**AN/01029**

***VERSION 2.1***

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**Date:** July 2001

# REVISION HISTORY

| REVISION | DATE | EDITOR | REFERENCE | REMARKS |
|---|---|---|---|---|
| 1.0 | June 1999 | Raymond MAUGIS | AN/99031 | - TDA8768A - DEMONSTRATION BOARD |
| 2.0 | March 2001 | Stéphane JOUIN | AN/01007 | - TDA8768A/C2 - DEMONSTRATION BOARD (update from C1 to C2 version) |
| 2.1 | July 2001 | Stéphane JOUIN | AN/01029 | - TDA8768A/C2 - DEMONSTRATION BOARD (update pages #6, #9 and #14) |

**Users are responsible for ensuring that they use the correct version of this document.**

# CONTENTS

## SUMMARY

The **TDA8768A** is a 12-bit high-speed **A**nalog-to-**D**igital **C**onverter designed for video data digitizing, high definition TV, imaging, medical imaging and other applications. It converts the analog input signal into 12 bits binary or into two's complement digital words at a maximum sampling rate of 70Msps.

Three versions of this device exist in QFP44 package: the **TDA8768AH/4**, the **TDA8768AH/5** and the **TDA8768AH/7** corresponding respectively to the clock frequency of 40, 55 and 70Msps.

This **A**pplication **N**ote describes the design and the realization of the **Demonstration Board** using the **TDA8768AH/C2** version (PCB n$^{o}$ 834-2) with an application environment.

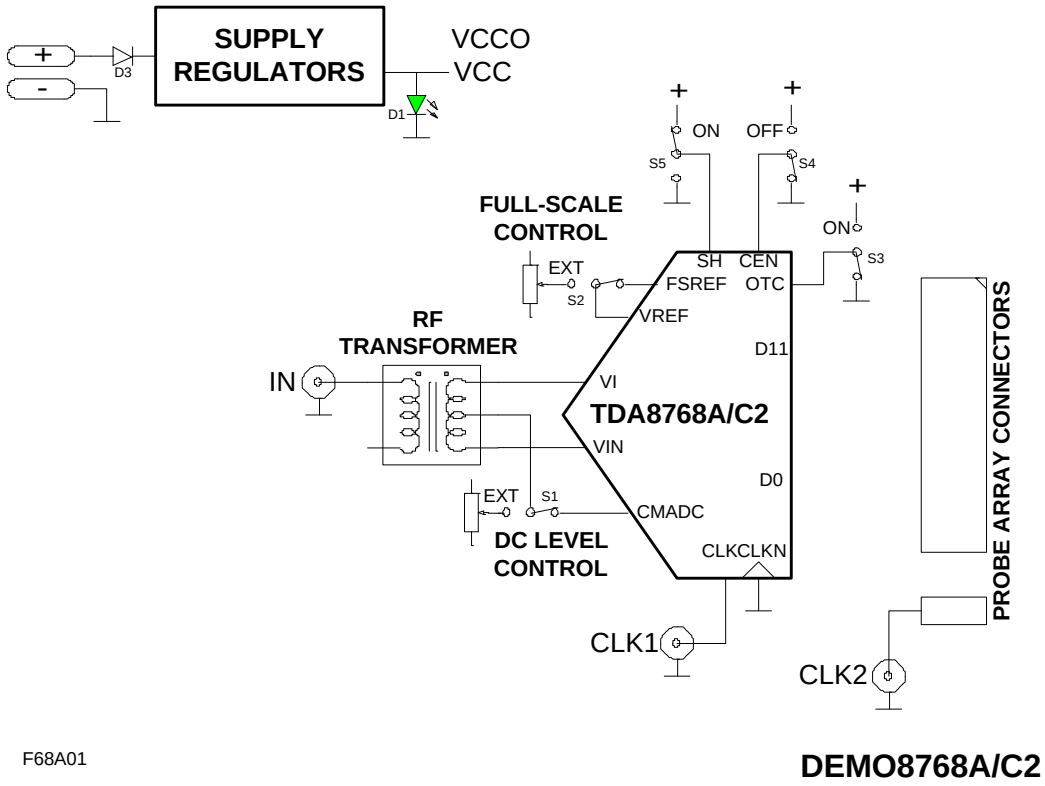
## 1. MAIN FEATURES OF THE TDA8768AH/C2:

The **TDA8768AH/C2** is a 12-bit **A**nalog-to-**D**igital **C**onverter. It can convert a typical analog input signal into 12 bits binary digital words at a maximum sampling rate of 70 Msps with a typical power dissipation of 550mW. The **TDA8768AH/C2** codes the binary or the two's complement digital words with 3.3V CMOS digital outputs. The main specifications points of this device are:

- Clock frequency: 40, 55 or 70Msps
- Output voltage: 3.3V.
- Power dissipation (typical): 550mW.
- Accuracy: 12-bit.
- Supply: 5V with output stages at 3.3V.
- Compatibility: input: TTL and CMOS,
  output: TTL and CMOS (3.3V).

## 2. PRINCIPLE AND DESCRIPTION OF THE BOARD:

The principle of the **Demo**nstration **Board** for the **TDA8768A/C2**, which is described in this **A**pplication **N**ote, is shown on **Figure 1**.




***- Figure 1. Functional block diagram of Demoboard -***

The different blocks of the **Demoboard** are:

- A power **supply regulators** used to supply all the circuitry on the board.
- A **RF transformer** transforming the single analog signal applied on the board into symmetrical differential analog signal on the ADC analog inputs .
- A **DC level control** fixing the ADC common mode voltage of the differential analog inputs from supply regulators.

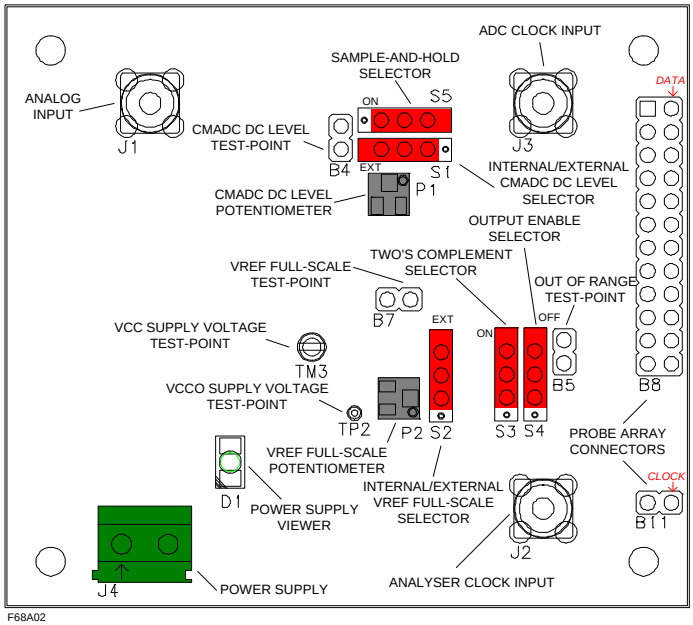
- A **full-scale control** adjusting the ADC full-scale from supply regulators.
- A **probe array connectors** connecting probes of a logic analyser.
- A **TDA8768A/C2** **A**nalog-to-**D**igital **C**onverter converting an analog signal into 12 bits binary digital words.

The **Demoboard** works with a single $+12V_{DC}$ external power supply. All circuitry is protected from reverse polarity. The good supply plugging is indicated by the green LED.

The sample clock signal on the **Demoboard** is available by plugging the square generator in the **CLK1** SMA connector. The output impedance of this generator must be 50Ω.

## 3. OVERVIEW OF THE BOARD:

The whole implantation of the **TDA8768AH/C2 Demoboard** version is shown on **Figure 2**.




***- Figure 2. Overview of Demoboard -***

The different connectors, potentiometers, switches, lights and test-points available on the board are:

- **For the general power supply:**

1. A two-points PHOENIX connector **J4** for **$12V_{DC}$** and **GND**.
2. A test-point **TM3** to control the **VCC** supply voltage.
3. A test-point **TP2** to control the **VCCO** supply voltage used only by the ADC stages outputs.
4. A **PWR** green light **D1** to indicate the good supply plugging.

- **For the DC level control:**

1. A switch **S1** to choose the internal or the **EXT** external common mode ADC.
2. A potentiometer **P1** to adjust the **CMADC** common mode ADC when the switch **S1** is on **EXT**.
3. A test-point **B4** to control the **CMADC** common mode ADC value.

- **For the full-scale control:**

1. A switch **S2** to choose the internal or the **EXT** external reference voltage.
2. A potentiometer **P2** to adjust the **VREF** reference voltage when the switch **S2** is on **EXT**.
3. A test-point **B7** to control the **VREF** reference voltage value.

- **For the evaluation of the TDA8768AH/C2:**

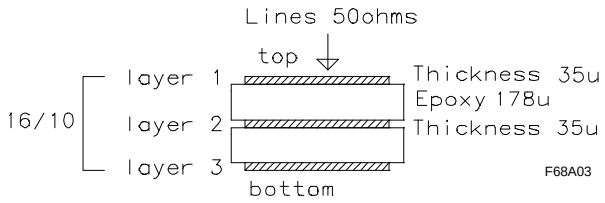
1. A SMA **J1** connector with 50Ω equivalent impedance for the analog input signal **IN**.
2. A SMA **J3** connector with 50Ω for the external clock input **CLK1**.
3. A switch **S3** to choose the ADC two's complement outputs by the input **OTC**.
4. A switch **S4** to enable the ADC outputs by the input **CEN**.
5. A switch **S5** to enable the sample-and-hold by the input **SH**.
6. A test-point **B5** indicating the out of range of the analog input signal.

- **For the reconstruction of the analog input waveform:**

1. Twelve-probe array connectors **B8** corresponding to the ADC digital outputs **D0** to **D11** are available to connect the logic analyser which computes the data.
2. A SMA **J2** connector with 50Ω, connected to probe array connectors **B11**, corresponding to the clock of the logic analyser.

## 4. PCB DESIGN:

The design is made on a multilayer **P**rinted **C**ircuit **B**oard. The technological concept used to make this PCB is given on **Figure 3**.




***- Figure 3. PCB structure -***

Three physical copper layers are used. The first layer is the signal layer which contains the microstrip lines. The second layer is made of the ground planes corresponding to the signal layer. The third layer is designed specially for the power supply wires.

The metallic hole technique is used to make all the necessary interconnections between the layers. The dielectric substrate is an Epoxy Glass resin with a relative permittivity ($e_r$) of 4.7 and a copper thickness of 35µm (≈1.4mils). The substrate thickness is ≈178mm (7mils) between the copper layers.

### *4.1 MICROSTRIP LINES:*

To calculate the width (**W**) of these 50Ω matched lines, the Kaup's relation was used:

$$W = \frac{5.98H}{0.8e^{\frac{Zo\sqrt{e_r+1.41}}{87}}} - \frac{t}{0.8},$$

(Accurate to within 5% when $0.1 < \frac{W}{H} < 3.0$ and $1 < e_r < 15$).

hence:

**W = 10.9mils/≈277mm**,

where:

Zo = 50Ω,
t = 1.4mils/≈35µm,
H = 7mils/≈178mm,
$e_r$ = 4.7.

### *4.2 POWER SUPPLY WIRE:*

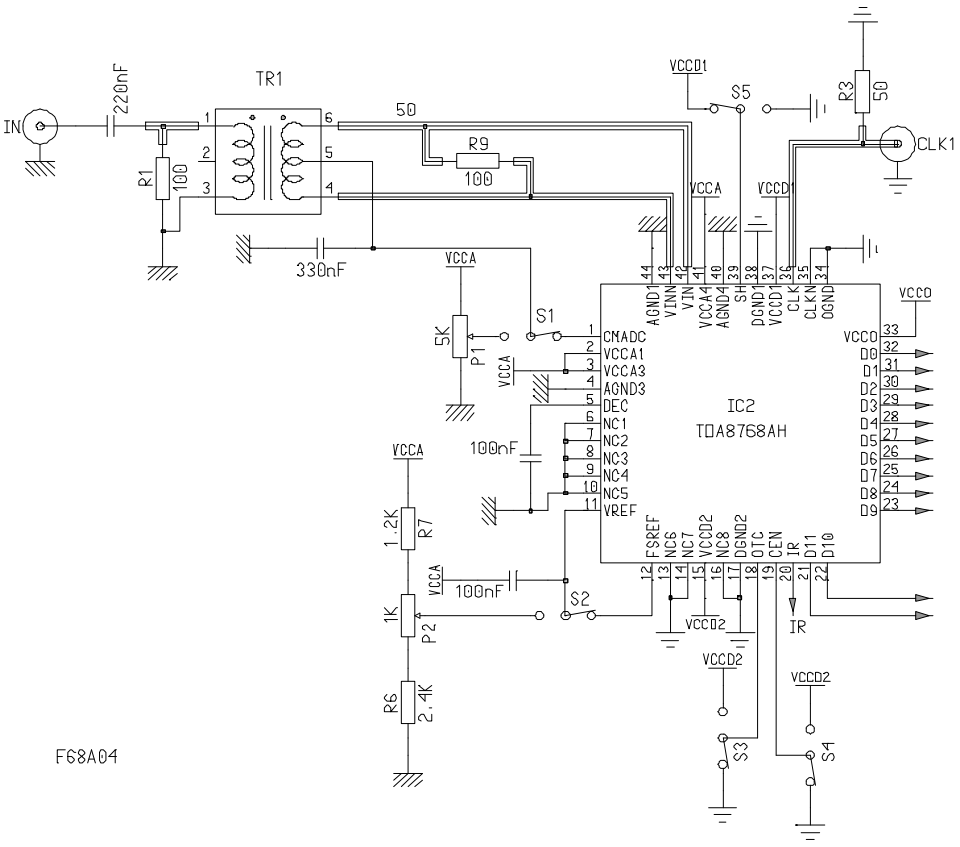
To reduce the voltage fluctuation effects due to switching currents inside the integrated circuits, the power supply wires are designed with a low characteristic impedance of microstrip lines in order to obtain a small equivalent inductance.

### *4.3 ANALOG AND DIGITAL RETURN GROUND POINT:*

To minimise the noise due to capacitive coupling between the analog input and the digital output parts of the ADC, two separate ground planes are designed on all layers and are connected together through an inductor.

## 5. SPECIAL FEATURES OF THE APPLICATION BOARD:

To obtain optimal performances, the recommended application diagram is given on **Figure 4**.




***- Figure 4. TDA8768A/C2 application diagram -***

### *5.1 ADC ANALOG INPUTS VI AND VIN:*

**The dynamic ADC analog signal** **VI** and **VIN** are connected through a 1:1 RF wideband transformer and a 220nF AC coupling to the external generator by the **IN** SMA connector. This connector is adapted by a 50Ω microstrip line and is connected to a 100Ω resistor. This value is calculated to have 50Ω equivalent ending: A 100Ω resistor connected between the both ADC analog inputs ensures a 50Ω matching and creates an analog virtual ground. Thereby with transformer ratio 1:1 and with the two 100Ω resistors, the equivalent impedance ending is 50Ω. The combination of the C capacitor and the R/2 equivalent impedance on the primary transformer forms a high-pass filter whose the -3dB cut-off frequency is determined by the relation:

$$f_{-3dB} = \frac{1}{\pi RC}.$$

The peak-to-peak magnitude nominal value $\mathbf{VI_{p.-p}}$ of the dynamic input signal is dependent on the VREF reference voltage applied on the specific pin of the device. With the typical values of VREF reference (VCC-1.75V), the $\mathbf{VI_{p.-p}}$ of the dynamic input signal is 1.8V. The quantum of the **TDA8768AH/C2** is defined by:

$$q = \frac{VI_{p.-p}}{2^{12} - 1},$$

hence,

$$\mathbf{q \approx 440\mu V}.$$

**The sample-and-hold selection** is chosen with the switch **S5**. The sample-and-hold selection is given on **Table 1**.

| SH | Sample-and-hold | Frequency |
|---|---|---|
| 1 | active | 7MHz ≤ $f_{clk}$ ≤ 70MHz |
| 0 | Inactive; tracking mode | $f_i$ ≤ 1MHz |

***- Table 1: Sample-and-hold selection -***

### *5.2 DATA OUTPUT D0 TO D11:*

All data outputs of the **TDA8768AH/C2** are 3.3V CMOS compatible and they are directly addressed to a probe array connectors. The guaranteed levels with a maximum load capacitance are:

$$V_{OL}max = 0.5V,$$

$$V_{OH}min = VCCO-0.5V,$$

The typical output transients time is:

$$t_{T(10\%-90\%)} = 6ns.$$

The output slew-rate can be estimated from the relation:

$$\frac{dV}{dt} = \frac{80\%(V_{OH} - V_{OL})}{t_{T(10\%-90\%)}},$$

hence:

$$\mathbf{\frac{dV}{dt} \approx 383mV / ns}.$$

From the slew-rate relation, the bit switching current is calculated from the relation:

$$I_o = C_L . \frac{dV}{dt},$$

hence:

$$\mathbf{I_o = 3.83mA / bit},$$

where:

$C_L$ = 10pF.

For the 12-bit ADC, the full-scale transition switching current is given by:

$$I_{FS} = n.I_o,$$

hence:

$$\mathbf{I_{FS} \approx 46mA},$$

where:

n: number of bits.

The output buffers of the TDA8768AH/C2 are designed to support these values. In the case where the load capacitance is higher than 10pF per bit, it is necessary to put a limiting serial resistor to adapt the slew-rate and to protect the ADC output buffers.

The switch **S3** corresponding to the two's complement input **OTC** allows the choice of either the binary or the *two's complement* digital words which correspondence is given on **Table 2** (in fact, *the two's complement* digital words corresponds to the binary digital words with the inverted MSB **D11**). The *two's complement* is enable when the switch **S3** is on **ON**.

| Step | IR | Binary outputs bits D11 to D0 | *Two's complement* output bits D11 to D0 |
|---|---|---|---|
| U/F | 0 | 000000000000 | 100000000000 |
| 0 | 1 | 000000000000 | 100000000000 |
| 1 | 1 | 000000000001 | 100000000001 |
| . | . | . | . |
| 2047 | 1 | 011111111111 | 111111111111 |
| . | . | . | . |
| 4094 | 1 | 111111111110 | 011111111110 |
| 4095 | 1 | 111111111111 | 011111111111 |
| O/F | 0 | 111111111111 | 011111111111 |

***- Table 2: Binary/Two's complement output coding -***

The switch **S4** corresponding to the output enable input **CEN** allows either to enable or to put high impedance state on the data outputs when is on **OFF**.

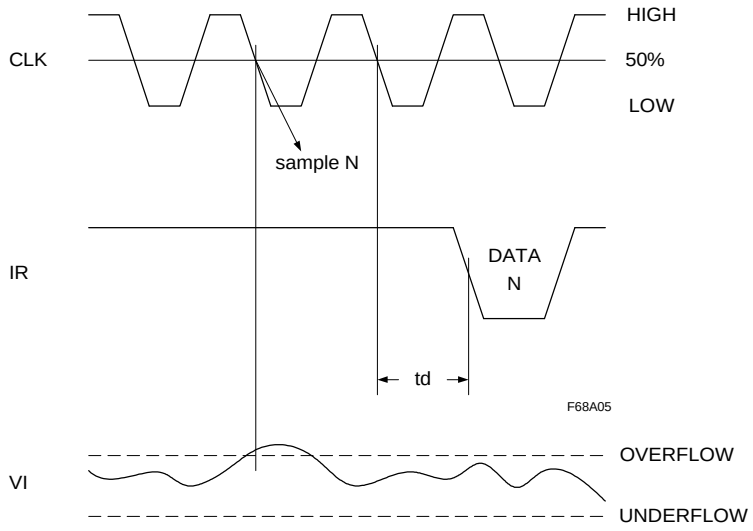
On the **Table 3** is given the relationship between the different choices.

| OTC | CEN | D11 to D0 | IR |
|---|---|---|---|
| X | 1 | high impedance | |
| 0 | 0 | binary | active |
| 1 | 0 | *two's complement* | active |

***- Table 3: Selection mode -***

### *5.3 IR-RANGE OUTPUT IR:*

The in-range output **IR** pin is directly connected to the test-point **B5**. When the underflow or overflow of the **VI** analog input signal is detected, the level on the test-point **B5** is low. The functional diagram is shown on **Figure 5**.




***- Figure 5. IR waveform -***

### *5.4 ADC ANALOG, DIGITAL AND OUTPUT STAGES POWER SUPPLIES:*

Two power supplies of 5V and 3.3V are necessary to supply the **TDA8768A/C2** respectively for the analog and digital pins and for the output stages.

To ensure a good bypassing at low and high frequencies, the use of several different parallel capacitors is required and SMD bypass $\pi$ type filters are implanted on the board near the ADC on each power pins.

### *5.5 DC LEVEL AND FULL-SCALE CONTROL:*

**The DC level control** fixed on the middle point of the transformer secondary is supplied either by the **TDA8768A/C2** (from **CMADC** pin) or by the potentiometer **P2** when the switch **S1** is on **EXT**. The test-point **B4** allows to control the voltage. The value of the common mode voltage is given by:

$$VCMADC = VCC - 1.6V .$$

A 330nF AC coupling is added on the middle point of the transformer secondary to get a good "dynamic" ground.

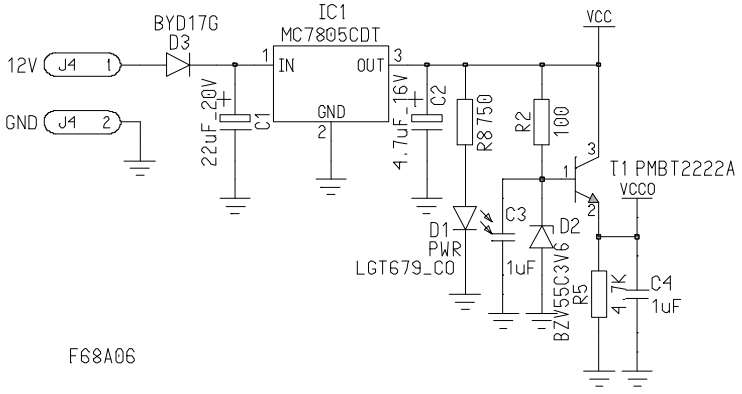
**The full-scale control** is supplied either by the **TDA8768A/C2** (from $\mathbf{FS_{ref}}$ pin) or by the potentiometer **P2** and the resistors **R6** and **R7** when the switch **S2** is on **EXT**. The test-point **B7** allows to control the voltage value of VREF. The value of the reference voltage is given by:

$$VREF = VCC - 1.75V.$$

## 6. ENVIRONMENT CIRCUITS:

### *6.1 GENERAL POWER SUPPLY:*

The electrical diagram is shown on **Figure 6**. An IC voltage regulator **IC1** is used directly mounted on the board and it is supplied from an external DC power unit of $12V_{DC}$/150mA. Nevertheless, the external voltage can range from $10V_{DC}$ to $15V_{DC}$. From the IC voltage regulator, a second voltage is created to supply only the output buffers of the device.




***- Figure 6. Electric diagram of the power supply -***

The regulation and the stabilisation of all circuitry come from the voltage value obtained after the protection diode **D3**. A stabilised voltage **VCC** of 5V is made from the MC7805CDT voltage regulator **IC1**. From the **VCC**, a second voltage **VCCO** of 3.3V, suppling the ADC output buffers, is made from the PMBT222A NPN transistor **T1** and the BZV55C3V6 zener diode **D2**. The **VCCO** voltage value is given by the relation

$$VCCO = V_z - V_{BE},$$

The maximum output current is fixed to 100mA in order to support the full-scale switching current (see chapter 5.2).

The transistor base current is given by the relation:

$$I_B = \frac{I_{FS}}{\beta},$$

where:

$I_{FS}$ = 100mA (full-scale switching current),
$\beta$ = 100.

To ensure a sufficient stability, the current in zener diode is fixed at ten time the transistor base current, hence:

$$I_z = \frac{10.I_{FS}}{\beta},$$

so:

$$R2 = \frac{VCC - V_Z}{I_Z + I_B},$$

hence:

**R2 = 100Ω**.

The distribution of the voltage is:

| **VCC used for:** | **VCCO used for:** |
|---|---|
| ADC digital and analog supply voltages. | ADC output stages supply voltage. |

The BYD17G Silicon diode **D3** ensures the protection of all the circuitry from reverse polarities. The good supply plugging is indicated by a green LED **D1**.

### *6.2 CLOCK GENERATION:*

On the Demoboard, the **CLK1** connector **J3** allows to drive the ADC clock input CLK with TTL/CMOS level. In this case, the complementary clock input CLKN is directly connected to the digital ground.

Nevertheless, the TDA8768AH/C2 can work with several logic families and can work with an AC signal given on **Table 4**.

| Logic family | CLK | CLKN |
|---|---|---|
| PECL | PECL | $3.65V_{DC}$ |
| | $3.65V_{DC}$ | PECL |
| | PECL | PECL |
| TTL/CMOS | TTL/CMOS | GNDD |
| | GNDD | TTL/CMOS |
| AC | $0.5V_{p.-p}$ | $2.5$ to $3.65V_{DC}$ |
| | $2.5$ to $3.65V_{DC}$ | $0.5V_{p.-p}$ |
| | $0.25V_{p.-p}$ | $0.25V_{p.-p}$ |

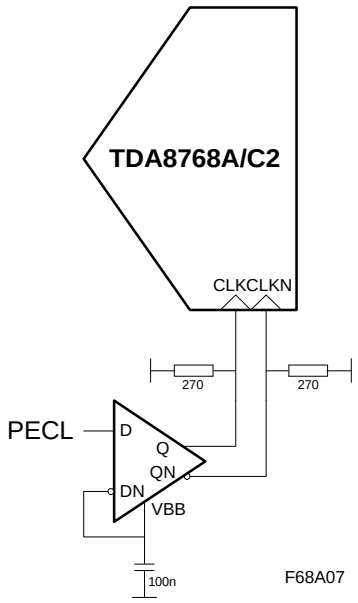
***- Table 4: Logic families and AC signal -***

With:

| **PECL:** | **CMOS:** | **TTL:** | **AC:** |
|---|---|---|---|
| $V_{IL}$ = 3.52V,<br>$V_{IH}$ = 3.83V. | $V_{IL}$ = 0.5V,<br>$V_{IH}$ = VCC-0.5V. | $V_{IL}$ = 0.8V,<br>$V_{IH}$ = 2.0V. | $V = 0.5V_{p.-p}$. |

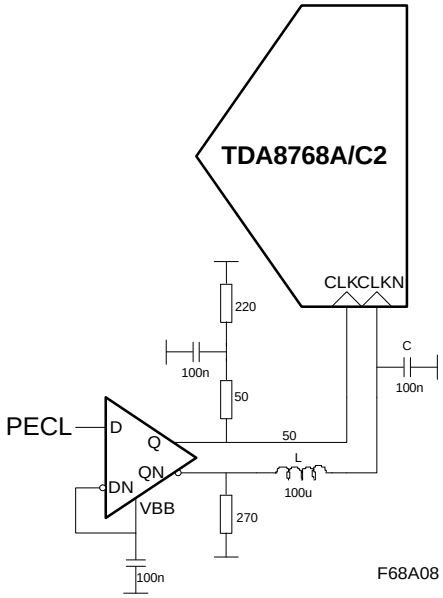
From these logic families, different clock interface circuits can be adopted to drive the clock of the TDA8768AH/C2.

**About the PECL driving**, two examples using a PECL single-ended/differential interface are given on **Figures 7 and 8**.




***- Figure 7: First Example of PECL single-ended/differential interface -***

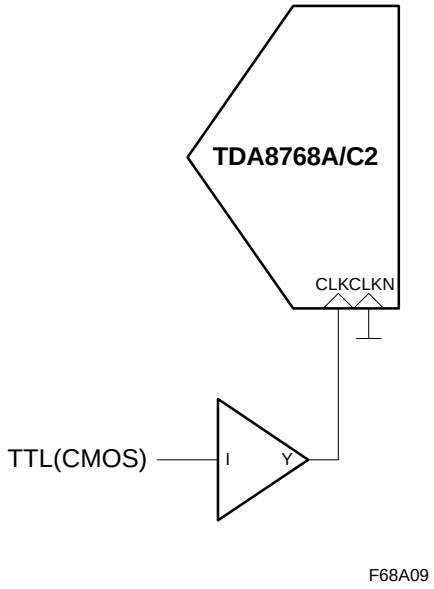
A low skew PECL differential receiver can be used to translate directly the PECL single-ended into PECL differential signal connected to the TDA8768A/C2 clock inputs. To preserve a duty cycle low skew on the differential clock signal, the transmission lines must have the same length which must be lower than 1inch/2.54cm.




***- Figure 8: Second Example of PECL single-ended/differential interface -***

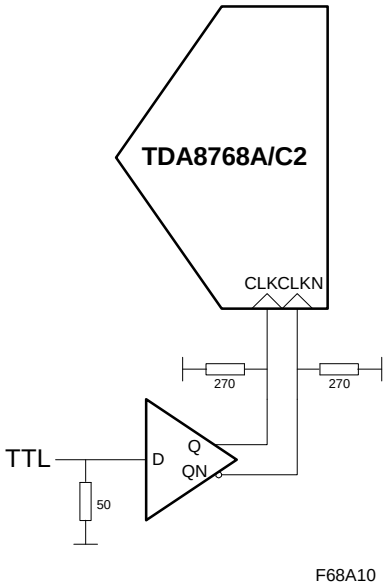
The PECL differential receiver must be located close to the TDA8768A/C2 clock inputs. The offset voltage is restored on the CLKN clock input through the inductance L and the capacitor C from the QN PECL differential receiver output. The transmission line between the Q PECL differential receiver output and the CLK input of the device must be lower than 1inch/2.54cm.

**About the TTL(CMOS) driving**, two examples using a TTL(CMOS)/TLL(CMOS) or a TTL/PECL interface are given on **Figure 9 and 10**.




***- Figure 9: Example of TTL(CMOS)/TTL(CMOS) interface -***

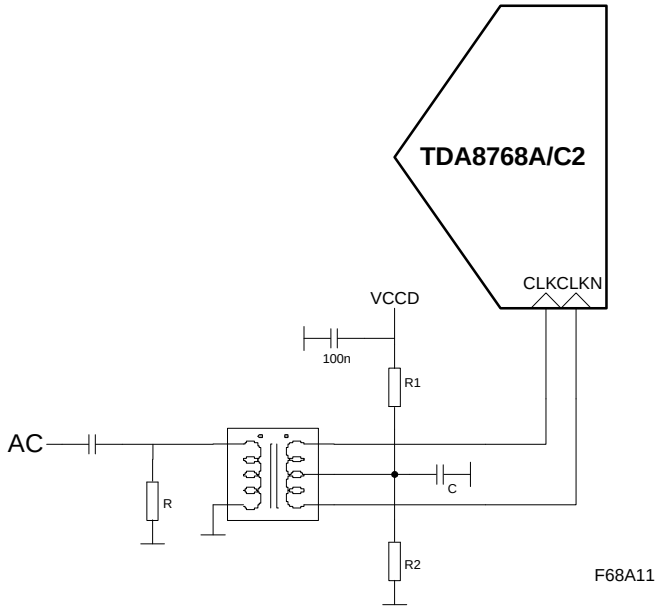
The simple interface uses a TTL(CMOS) buffer/driver connected on the CLK clock input. In this case, the CLKN clock input is connected to the digital ground.




***- Figure 10: Example of TTL/PECL interface -***

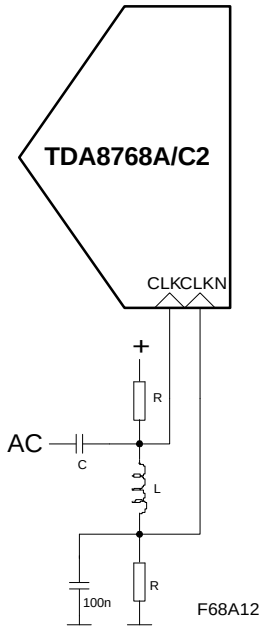
A TTL to differential PECL translator can be used to make the adaptation between the TTL clock and the TDA8768A/C2 clock inputs.

**About the AC driving**, two examples using a AC single-ended/differential or a RLC interface are given on **Figure 11 and 12**.



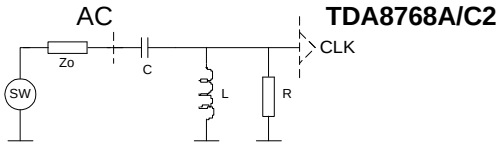

***- Figure 11: Example of AC single-ended/differential interface -***

With the RF transformer of 1:1 ratio, the primary load resistor must be chosen to match the source impedance. In this case, the TDA8768A/C2 input impedance can be eliminate for the calculation. The supplied peak to peak amplitude delivered by the source signal must be higher than $500mV_{p.-p}$. The DC level voltage on the middle point of the transformer secondary is fixed by the resistor bridge R1 and R2. To ensure a stability of the DC level, the current in the resistor bridge must be higher than the specified high level input clock current $I_{IH}$ of the device ($10 \times I_{IH}$ for example). The dynamic ground is ensured on the middle point by a wide-band decoupling C (4.7µF in parallel with a 100nF capacitor for example).




***- Figure 12: Example of RLC interface -***

The dynamic equivalent clock input circuit is given on the **Figure 13**.




***- Figure 13: Equivalent clock input -***

At the clock frequency used, the following condition must be respected:

$$\frac{1}{C\omega_o} \langle\langle |Z_{IN}|,$$

where:

$F_o$ = clock frequency,

$$|Z_{IN}| = \frac{RL\omega_o}{\sqrt{R^2 + L\omega_o^2}}.$$

Therefore, if the resistor value R is sufficiently high, the inductance value L can be chosen in order to obtain the matching impedance on the output generation clock circuit.

**The jitter** value of the clock signal must be low otherwise some sampling errors can appear. The jitter value can be calculated from the slope of the sinewave input signal. The sinewave input signal is given by:

$$v(t) = \frac{vi_{FS}}{2}.\sin(2.p.f_i.t),$$

where:

| | |
|---|---|
| $vi_{FS} = 2^n.q$ | : ADC full scale, |
| n | : ADC bit number, |
| $f_i$: | : input signal frequency. |

So, the slope of the sinewave is:

$$\Delta v(t) = \Delta t.\frac{\P v(t)}{\P t} = \Delta t.\frac{vi_{FS}}{2}.2.p.f_i.\cos(2.p.f_i.t).$$

The slope is maximum at $t_0$=0 (middle of the input full scale):

$$\Delta v(t_0) = \Delta t_0.vi_{FS}.p.f_i,$$

hence:

$$\Delta t_0 = \frac{\Delta v(t_0)}{2^n.q.p.f_i}.$$

For a jitter below the quantum ($\Delta v(t_0)$ = q), it must be inferior at:

$$\mathbf{\Delta t_0 < 2.22ps},$$

with:

n = 12,
$f_i$ = 35MHz.

The variation around the frequency of the sampling clock is given by:

$$\frac{\Delta f_{clk}}{f_{clk}} = \frac{\frac{\Delta t_0 . f_{clk}}{2}}{1 - \left(\frac{\Delta t_0 . f_{clk}}{2}\right)^2},$$

hence:

$$\frac{\mathbf{\Delta f_{clk}}}{\mathbf{f_{clk}}} < \mathbf{\pm 77.7 ppm}.$$

where:

$f_{clk}$ = 70MHz.

## 7. OPERATING MODE:

An external power unit of $12V_{DC}$/150mA is required to supply the **Demoboard**. However, the board is able to work between $10V_{DC}$ and $15V_{DC}$.

All DC voltage of **P1** (CMADC) and **P2** (VREF) are locked in the **Sy**stem **& A**pplication **D**ata **C**onverter in **C**aen before delivery to be in accordance with the product specifications.

So:

**CMADC = VCC-1.6V**,

**VREF = VCC-1.75V**,

But the **VREF** and **CMADC** values may be modified by the user to obtain a different full-scale and DC level of input analog signals.

### *7.1 EXTERNAL SINGLE CLOCK OPERATION:*

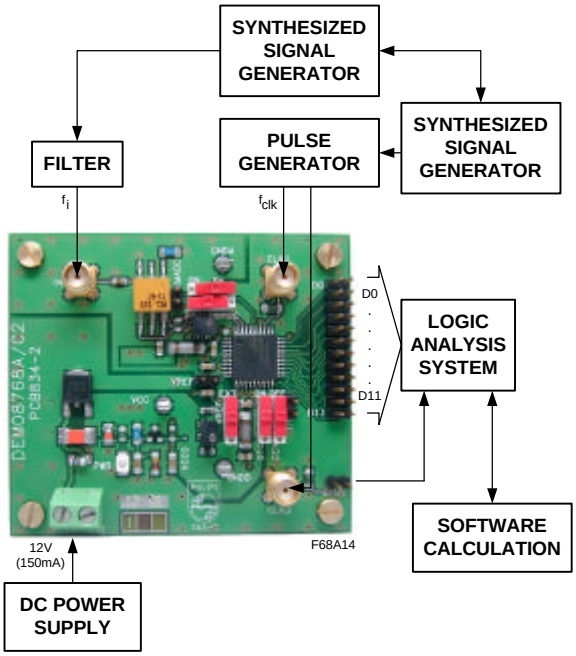
When an external 50Ω square clock generator is connected to **J3** connector, The required clock levels are:

**$V_{CLKH}$ min = 2.0V,**

**$V_{CLKL}$ max = 0.8V**.

## 8. PERFORMANCES:

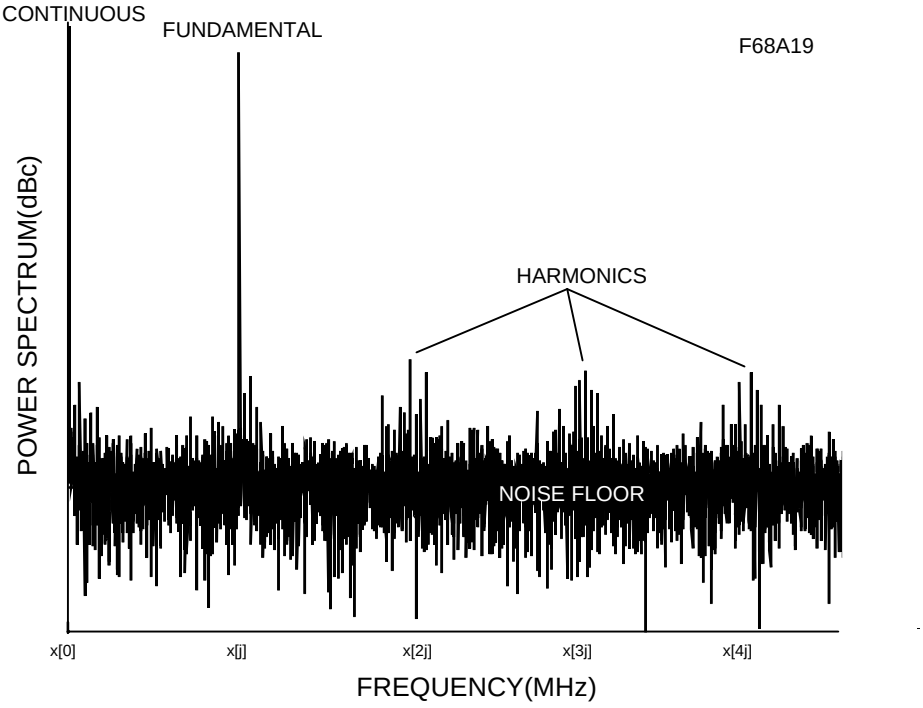
An evaluation of the **TDA8768AH/C2** ADC performances were made with the **Demoboard** environment on CAEN's dynamic bench which block diagram is given on **Figure 14**.




***- Figure 14. CAEN's dynamic bench block diagram -***

### *8.1 DEFINITION OF THE MEASURING PARAMETERS:*

To evaluate the ADC performances on the Demoboard, the CAEN dynamic bench uses the **F**ast **F**ourier **T**ransform for dynamic parameters from the sample signal.




***- Figure 15. FFT -***

According to the FFT shown on **Figure 15**, the main dynamic parameters are:

- The **T**otal **H**armonic **D**istortion is the ratio between the RMS signal amplitude and the RMS sum of the first five harmonics. From the power spectrum of FFT, the **THD** is calculated from the relation:

$$THD_{dBc} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2}^{6} x^2[i \times j]}}.$$

Where:

$x[j]$ : fundamental component corresponding with the j spectrum component,

$x[i \times j]$ : component of harmonic i.

- The **S**purious **F**ree **D**ynamic **R**ange is the ratio between the RMS signal amplitude and the RMS value of the highest spectrum component (harmonic or noise). From the FFT, the **SFDR** is calculated from the relation:

$$SFDR_{dB} = 20 \times \log_{10} \frac{x[j]}{MAX(x[i])}.$$

Where:

$x[i]$: spectrum component i with $i \in [2:\frac{N}{2}]$ (N: number of samples) and $i \neq x[j]$.

- The **SI**gnal to **N**oise **A**nd **D**istortion ratio is the ratio between the RMS signal amplitude and the RMS sum of all the other spectral components. From the FFT, the **SINAD** is calculated from the relation:

$$SINAD_{dB} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2, i \neq j}^{\frac{N}{2}} x[i]}}.$$

- The **S**ignal to **N**oise **R**atio is the ratio between the RMS signal amplitude and the RMS sum of all the other spectral components without harmonic used in the **THD** relation. From the FFT, the **SNR** is calculated from the relation:

$$SNR_{dB} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2, i \neq j \times [1:6]}^{\frac{N}{2}} x[i]}}.$$

- The **E**ffective number of bit is calculated by the relation (valid to NYQUIST condition):

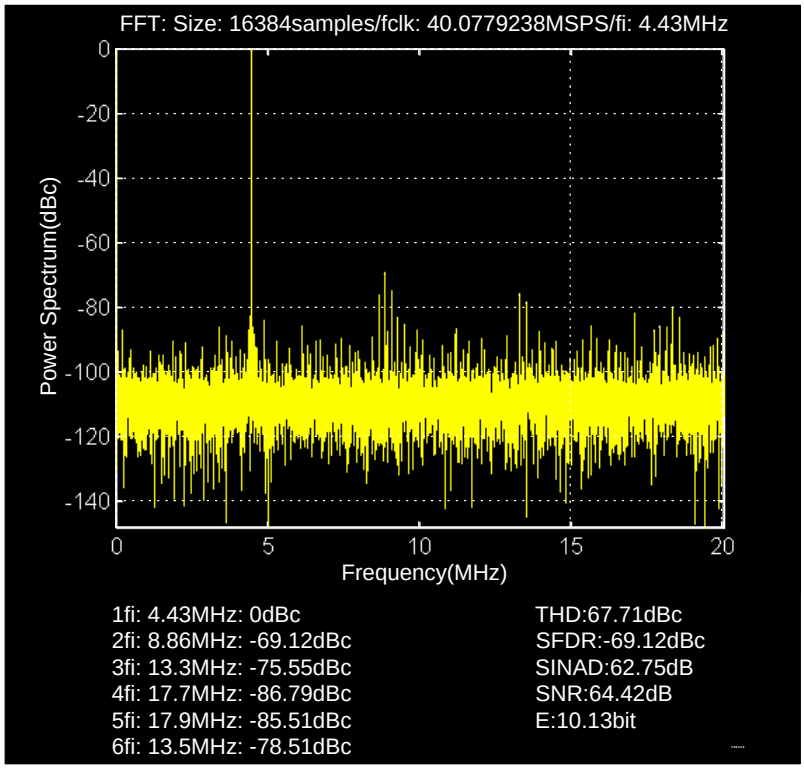
$$E_{BIT} = \frac{SINAD - 10 \times \log_{10} \frac{3}{2}}{20 \times \log 2}.$$

### *8.2 MEASUREMENT OF THE 40MSPS:*

This version of the **Demoboard** is evaluated with the following measurement conditions:

| | |
|---|---|
| Input frequency: | 4.43MHz. |
| Waveform: | Sinewave. |
| Magnitude: | Full Scale. |
| Antialiasing Filter: | Yes |
| Clock frequency: | 40Msps. |
| Output format: | Binary. |

The typical results and the corresponding diagrams obtained with these conditions are given on **Figure 16**



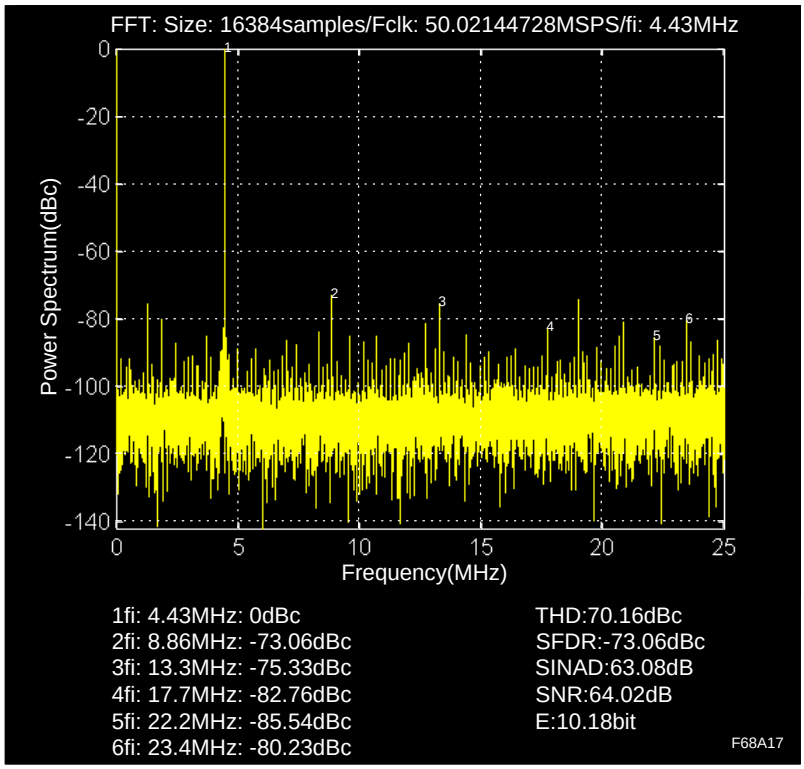

***- Figure 16. FFT results at 4.43MHz@40Msps -***

### *8.3 MEASUREMENT OF THE 55MSPS:*

This version of the **Demoboard** is evaluated with the following measurement conditions:

| | |
|---|---|
| Input frequency: | 4.43MHz. |
| Waveform: | Sinewave. |
| Magnitude: | Full Scale. |
| Antialiasing Filter: | Yes |
| Clock frequency: | 50Msps. |
| Output format: | Binary. |

The typical results and the corresponding diagrams obtained with these conditions are given on **Figure 17**.



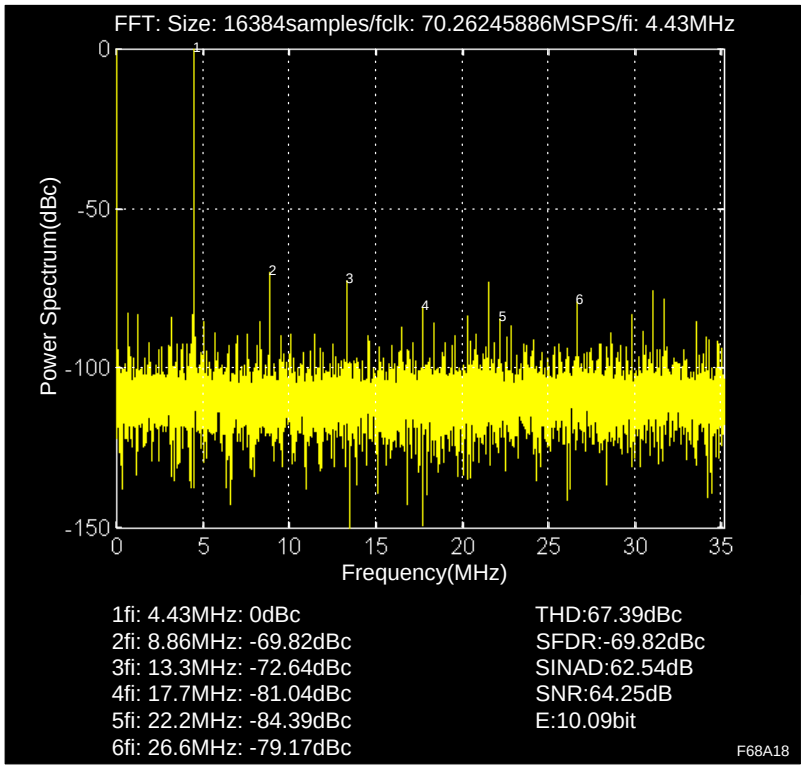

***- Figure 17. FFT results at 4.43MHz@50Msps -***

### *8.4 MEASUREMENT OF THE 70MSPS:*

This version of the **Demoboard** is evaluated with the following measurement conditions:

| | |
|---|---|
| Input frequency: | 4.43MHz. |
| Waveform: | Sinewave. |
| Magnitude: | Full Scale. |
| Antialiasing Filter: | Yes |
| Clock frequency: | 70Msps. |
| Output format: | Binary. |

The typical results and the corresponding diagrams obtained with these conditions are given on **Figure 18**.




***- Figure 18. FFT results at 4.43MHz@70Msps -***

# 9. DEMOBOARD FILES:

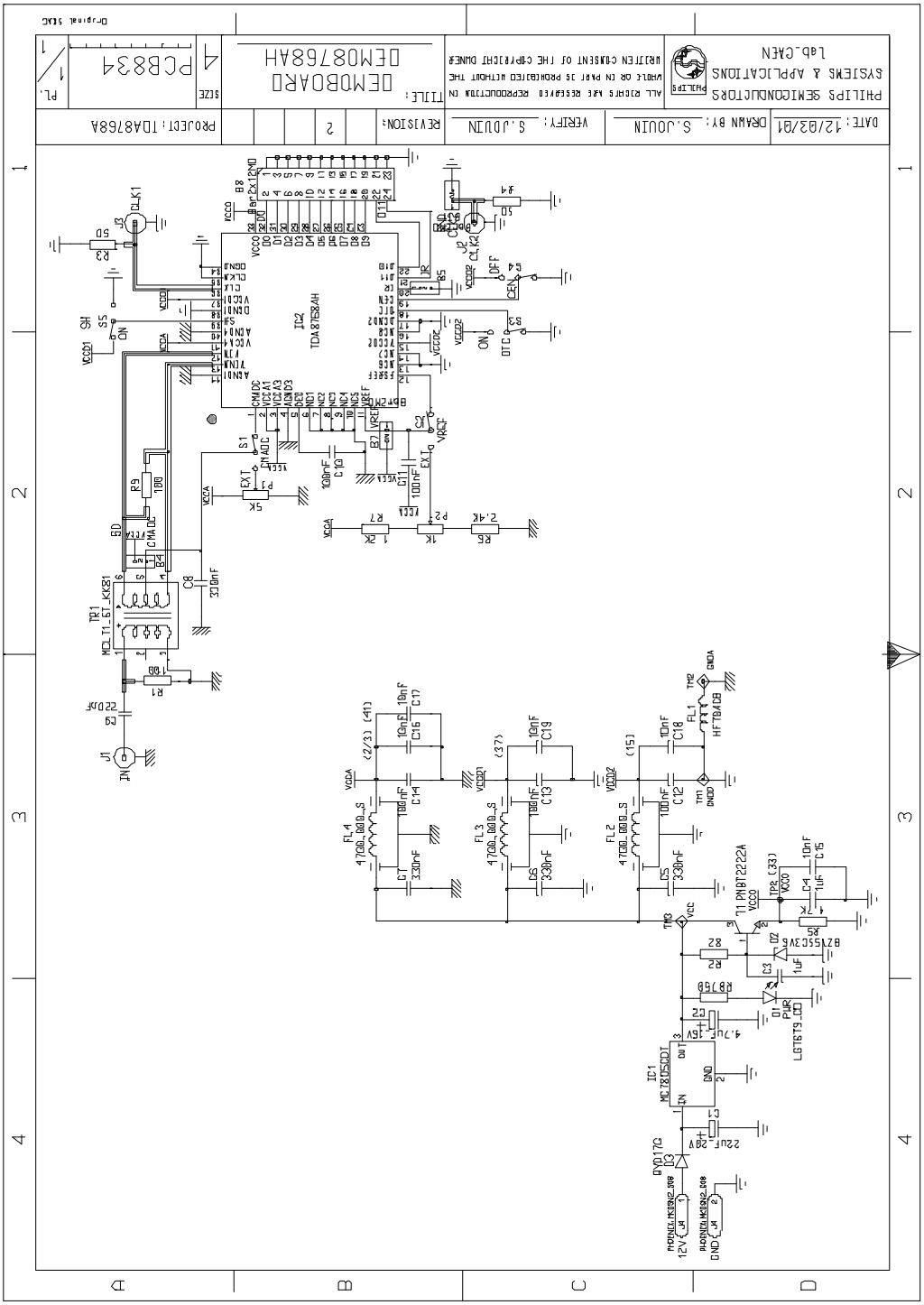
## *9.1 TDA8768A/C2 VERSION:*

All documents needed for the realization of this Demoboard are given on **Figures 19 to 24**.

- Electrical diagram.
- Topside component implantation.
- Underside component implantation.
- Topside component layout 1.
- Internal ground plane layout 2.
- Internal supply layout 3.
- Internal ground plane layout 4.
- Underside component layout 5.

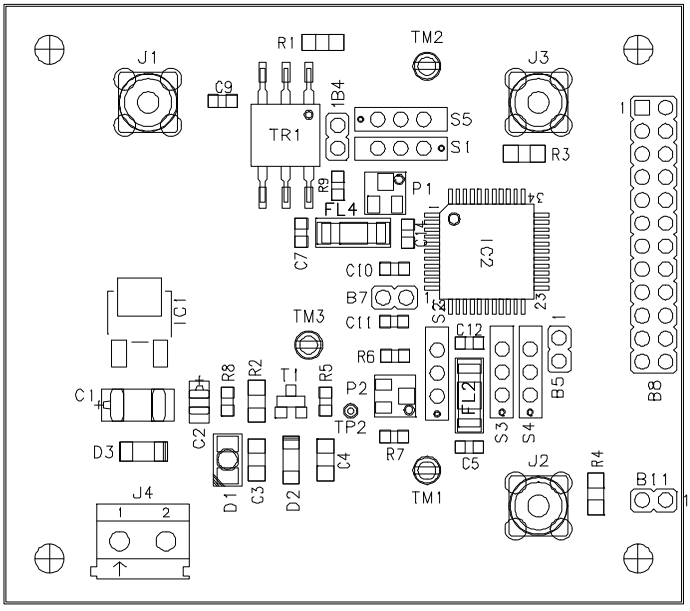
## *9.2 COMPONENTS LIST:*

The all version components list with their values and references is given on **Tables 5 to 6**.



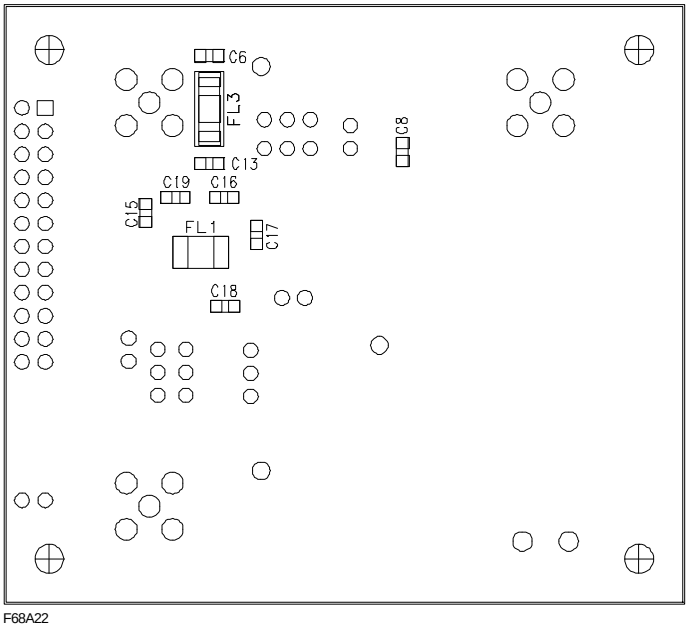
F68A23

***- Figure 19. TDA8768AH/C2 Demoboard electrical diagram -***



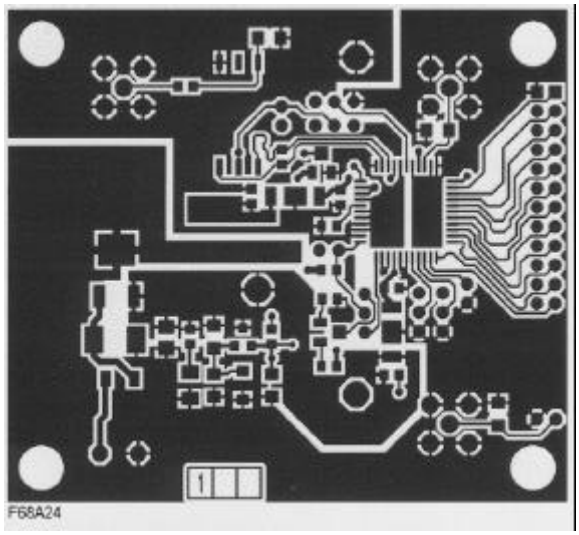

F68A21

*- Figure 20. TDA8768AH/C2 topside component implantation -*

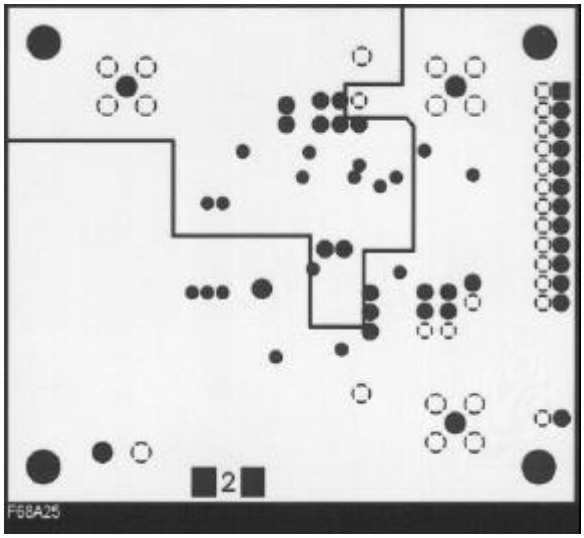



F68A22

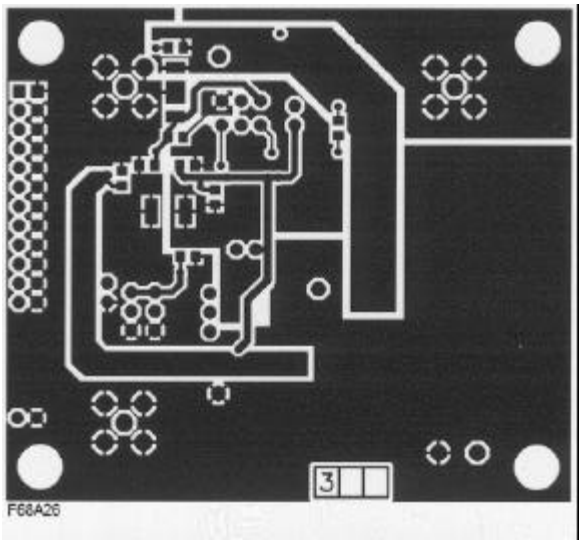
*- Figure 21. TDA8768AH/C2 underside component implantation -*




*- Figure 22. Topside component layout (signal layer 1) -*




*- Figure 23. Internal plane layout (ground layer 2) -*




*- Figure 24. Underside component layout (supply layer 3) -*

| REF | VALUE | COMPONENT | TYPE | MANUFACTURER |
|---|---|---|---|---|
| C1 | 22µF/20V | CAPACITOR | 293D/C | SPRAGUE |
| C2 | 4.7µF/16V | " | 293D/A | " |
| C3 | 1µF | " | C1206 | PHILIPS |
| C4 | 1µF | " | " | " |
| C5 | 330nF | " | C0805 | " |
| C6 | 330nF | " | " | " |
| C7 | 330nF | " | " | " |
| C8 | 330nF | " | " | " |
| C9 | 220nF | " | " | " |
| C10 | 100nF | " | " | " |
| C11 | 100nF | " | " | " |
| C12 | 100nF | " | " | " |
| C13 | 100nF | " | " | " |
| C14 | 100nF | " | " | " |
| C15 | 10nF | " | " | " |
| C16 | 10nF | " | " | " |
| C17 | 10nF | " | " | " |
| C18 | 10nF | " | " | " |
| C19 | 10nF | " | " | " |
| | | | | |
| D1 | | GREEN LED | LGT679-CO | SIEMENS |
| D2 | | ZENER DIODE | BZV55C | PHILIPS |
| D3 | | DIODE | BYD17G | " |
| | | | | |
| T1 | | NPN TRANSISTOR | PMBT2222A | PHILIPS |
| | | | | |
| TR1 | | RF TRANSFORMER | MCLT1-6T-KK81 | MINI-CIRCUIT |
| | | | | |
| FL1 | | HF70ACB-453215T | C1812 | PHILIPS |
| FL2 | 2nF | Π FILTER | 4700-003-S | TUSONIX |
| FL3 | 2nF | " | " | " |
| FL4 | 2nF | " | " | " |
| | | | | |
| IC1 | | VOLTAGE REGULATOR | MC78M05CDT | MOTOROLA |
| IC2 | | ADC | TDA8768AH/C2 | PHILIPS |
| | | | | |
| J1 | 50Ω | CONNECTOR | SMA | RADIALL |
| J2 | 50Ω | " | " | " |
| J3 | 50Ω | " | " | " |
| J4 | | " | MKSD | PHOENIX |
| | | | | |
| S1 | | SWITCH | 1C2P | SECME |

***- Table 5. List of components(1/2) -***

| REF | VALUE | COMPONENT | TYPE | MANUFACTURER |
|---|---|---|---|---|
| S2 | | SWITCH | 1C2P | SECME |
| S3 | | ' | ' | ' |
| S4 | | ' | ' | ' |
| S5 | | ' | ' | ' |
| L1 | | HF70ACB-453215T | C1812 | PHILIPS |
| P1 | 5KΩ | POTENTIOMETER | 3224W | BOURNS |
| P2 | 1KΩ | ' | ' | ' |
| Y1 | 80MHz | OSCILLATOR | IQX0 | KONY |
| R1 | 100Ω | RESISTOR | 1206 | PHILIPS |
| R2 | 82Ω | ' | ' | ' |
| R3 | 50Ω | ' | ' | ' |
| R4 | 50Ω | ' | ' | ' |
| R5 | 4.7kΩ | ' | 0805 | ' |
| R6 | 2.4kΩ | ' | ' | ' |
| R7 | 1.2kΩ | ' | ' | ' |
| R8 | 750Ω | ' | ' | ' |
| R9 | 100Ω | ' | ' | ' |
| TM1 | | MEASUREMENT POINT | | COMATEL |
| TM2 | | ' | | ' |
| TM3 | | ' | | ' |
| B4 | | TEST POINT | 2x1 | COMATEL |
| B5 | | ' | ' | ' |
| B7 | | ' | ' | ' |
| B8 | | ' | 2x12 | ' |
| B11 | | ' | 2x1 | ' |

***- Table 6. List of components(2/2) -***