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Kind regards,

Team Nexperia

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- 100% gate resistance tested
- 100% Ruggedness tested
- Lead-free package
- Logic level compatible
- Optimized for use in DC-to-DC converters
- Very low switching and conduction losses

1.3 Applications

- DC-to-DC converters
- Notebook computers
- Switched-mode power supplies
- Voltage regulators

1.4 Quick reference data

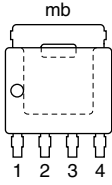
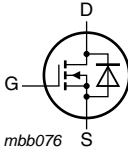
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	25	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 3	[1]	-	100	A
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 12\text{ V}$; see Figure 12 ; see Figure 13	-	8	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 10 ; see Figure 11	-	1.4	1.8	mΩ

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT669 (LFAK)</p>	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PH1825AL	LFAK	plastic single-ended surface-mounted package (LFAK); 4 leads	SOT669

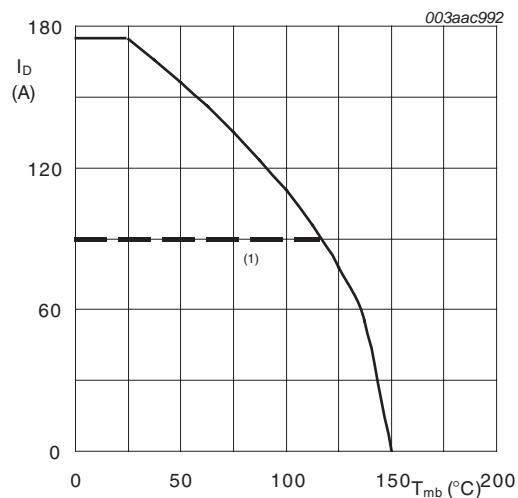
4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	100	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3	[1]	100	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$; see Figure 3	-	697	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	104	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$; [1]	-	100	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	697	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 25\text{ V}$; $t_p = 0.15\text{ ms}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	239	mJ

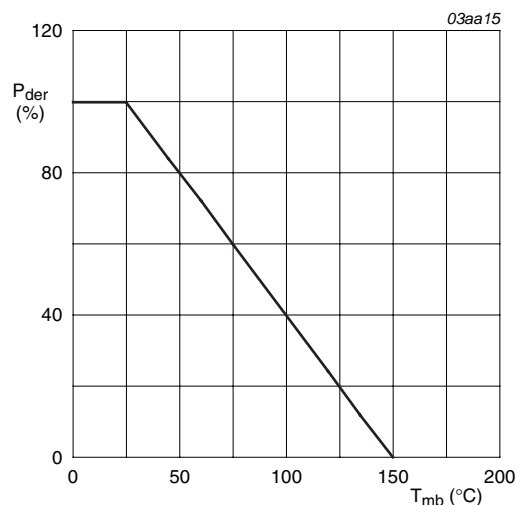
[1] Continuous current is limited by package.



$$V_{GS} \geq 10V$$

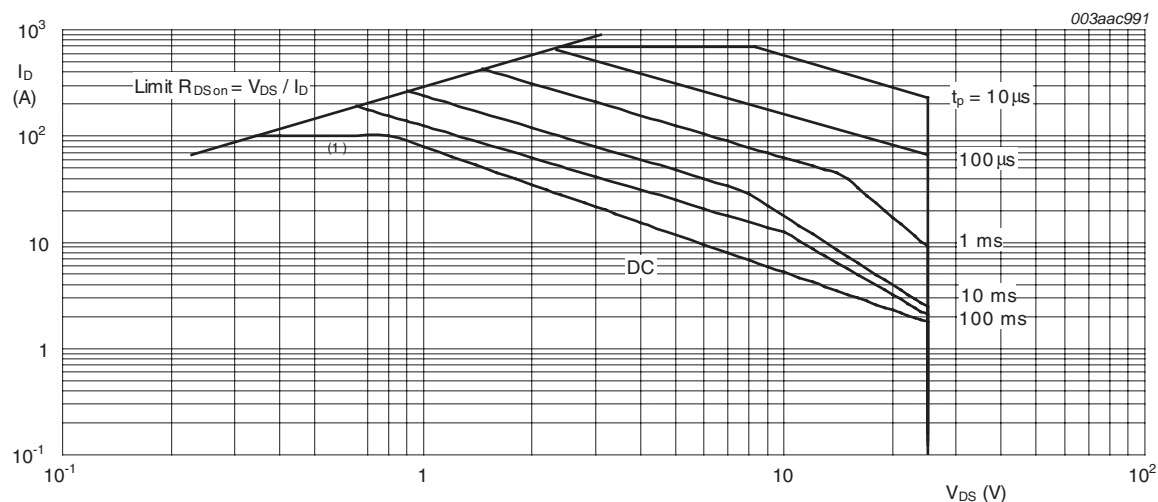
(1) Capped at 100 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$$T_{mb} = 25^\circ C; I_{DM} \text{ is single pulse}$$

(1) Capped at 100 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.2	K/W

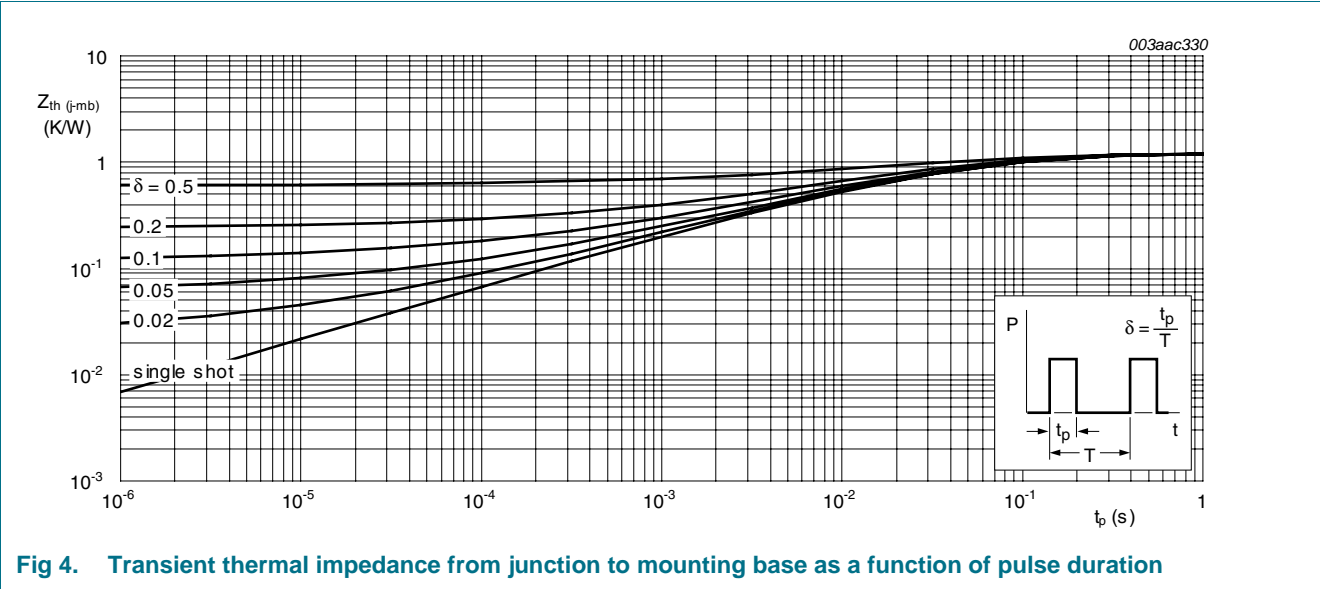


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	25	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = -55 ^\circ C$	23.2	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = 25 ^\circ C$; see Figure 8 ; see Figure 9	1.3	1.7	2.15	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = 150 ^\circ C$; see Figure 8 ; see Figure 9	0.65	-	-	V
		$I_D = 1 mA$; $V_{DS} = V_{GS}$; $T_j = -55 ^\circ C$; see Figure 8 ; see Figure 9	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 25 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	-	1	μA
		$V_{DS} = 25 V$; $V_{GS} = 0 V$; $T_j = 150 ^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	100	nA
		$V_{GS} = -16 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V$; $I_D = 25 A$; $T_j = 25 ^\circ C$; see Figure 10	-	2	2.7	m Ω
		$V_{GS} = 10 V$; $I_D = 25 A$; $T_j = 150 ^\circ C$; see Figure 10	-	2.4	3.1	m Ω
		$V_{GS} = 10 V$; $I_D = 25 A$; $T_j = 25 ^\circ C$; see Figure 10 ; see Figure 11	-	1.4	1.8	m Ω
R_G	gate resistance	$f = 1 MHz$	-	0.95	1.5	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A$; $V_{DS} = 12 V$; $V_{GS} = 4.5 V$; see Figure 12 ; see Figure 13	-	31	-	nC
		$I_D = 0 A$; $V_{DS} = 0 V$; $V_{GS} = 4.5 V$	-	24.5	-	nC
Q_{GS}	gate-source charge	$I_D = 25 A$; $V_{DS} = 12 V$; $V_{GS} = 4.5 V$; see Figure 12 ; see Figure 13	-	10.4	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	5.4	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	5	-	nC
Q_{GD}	gate-drain charge		-	8	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 12 V$; see Figure 12 ; see Figure 13	-	2.54	-	V
C_{iss}	input capacitance	$V_{DS} = 12 V$; $V_{GS} = 0 V$; $f = 1 MHz$; $T_j = 25 ^\circ C$; see Figure 14	-	4300	-	pF
		$V_{DS} = 0 V$; $V_{GS} = 0 V$; $f = 1 MHz$; $T_j = 25 ^\circ C$	-	4800	-	pF
C_{oss}	output capacitance	$V_{DS} = 12 V$; $V_{GS} = 0 V$; $f = 1 MHz$; $T_j = 25 ^\circ C$; see Figure 14	-	1100	-	pF
C_{rss}	reverse transfer capacitance		-	390	-	pF

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{d(on)}	turn-on delay time	V _{DS} = 12 V; R _L = 0.5 Ω; V _{GS} = 4.5 V; R _{G(ext)} = 5.6 Ω	-	47	-	ns
t _r	rise time		-	72	-	ns
t _{d(off)}	turn-off delay time		-	54	-	ns
t _f	fall time		-	29	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 15	-	0.82	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/s; V _{GS} = 0 V;	-	43	-	ns
Q _r	recovered charge	V _{DS} = 25 V	-	53	-	nC

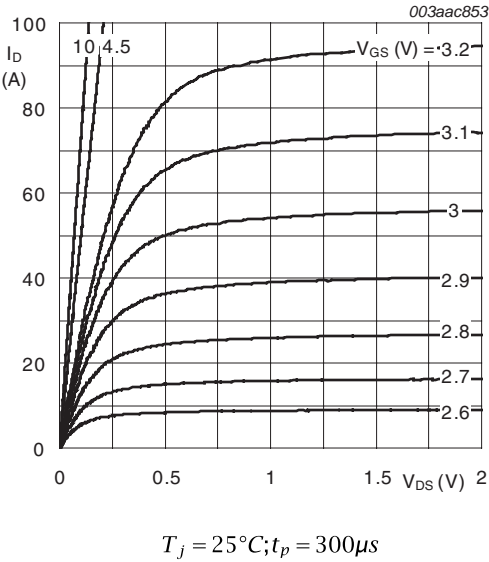


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

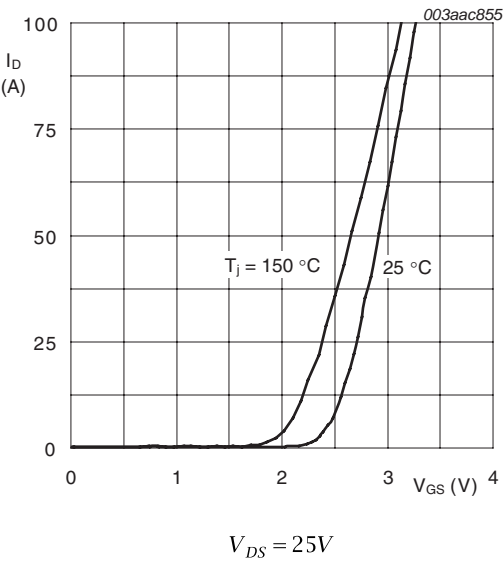
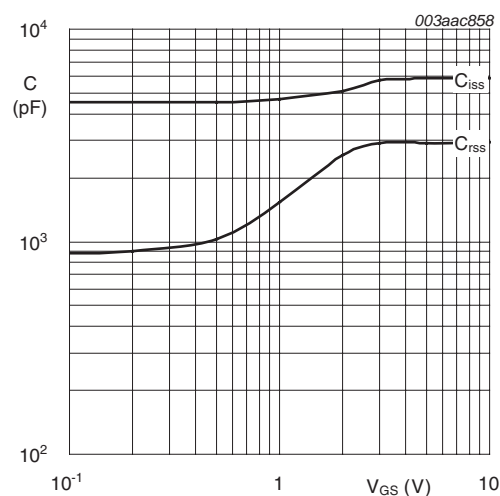
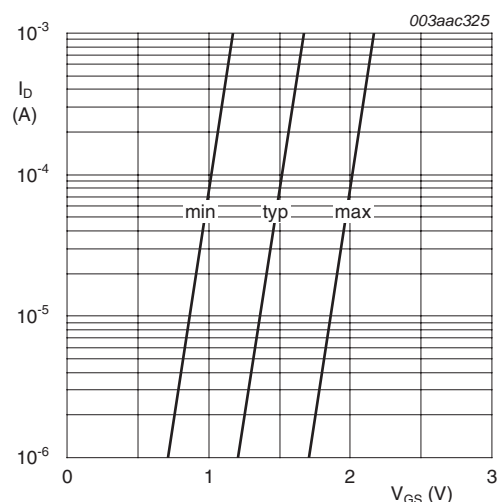


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



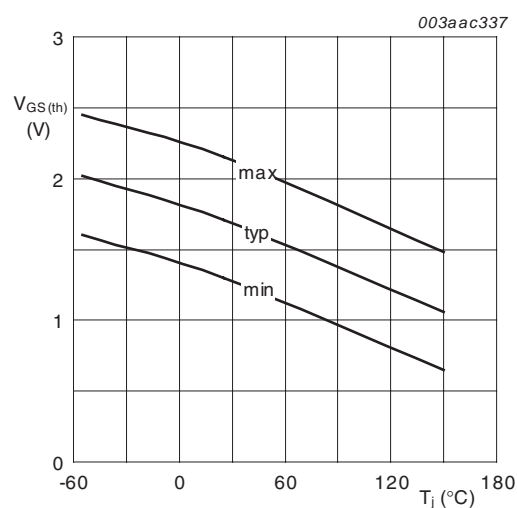
$$V_{DS} = 0V; f = 1MHz$$

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



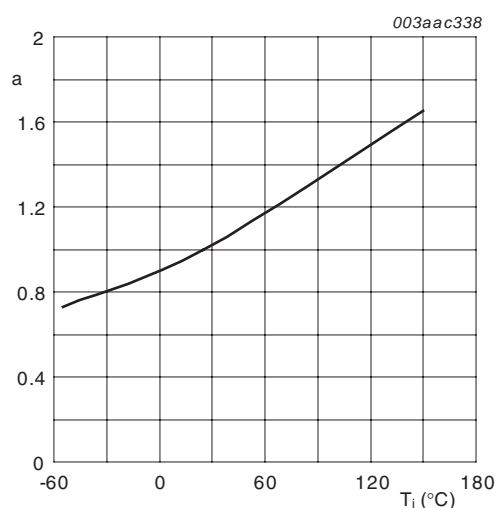
$$T_j = 25^\circ C; V_{DS} = 25V$$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



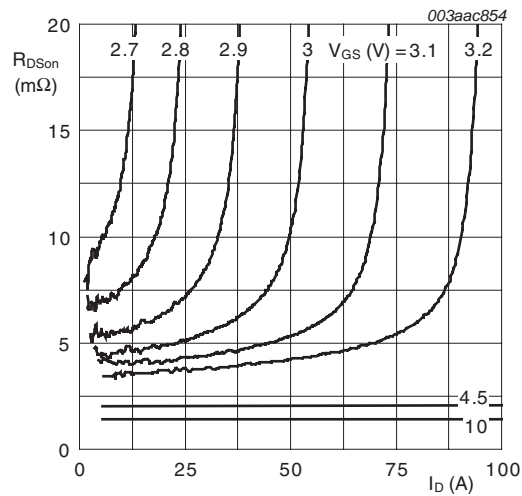
$$I_D = 1mA; V_{DS} = V_{GS}$$

Fig 9. Gate-source threshold voltage as a function of junction temperature



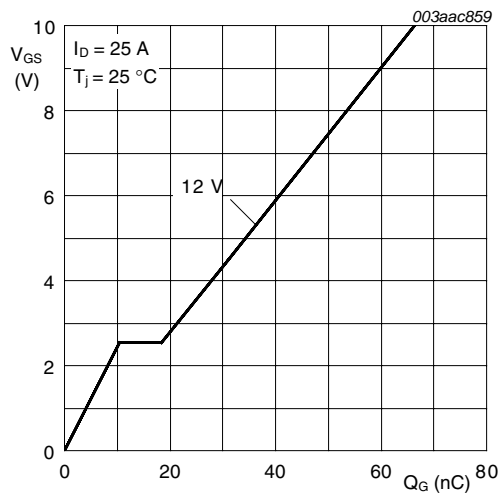
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^\circ C$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values.



$T_j = 25^\circ C; I_D = 25 A$

Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values.

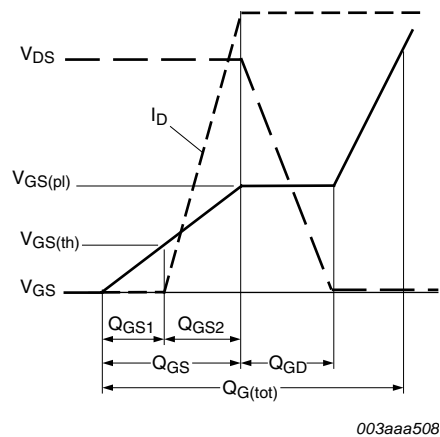
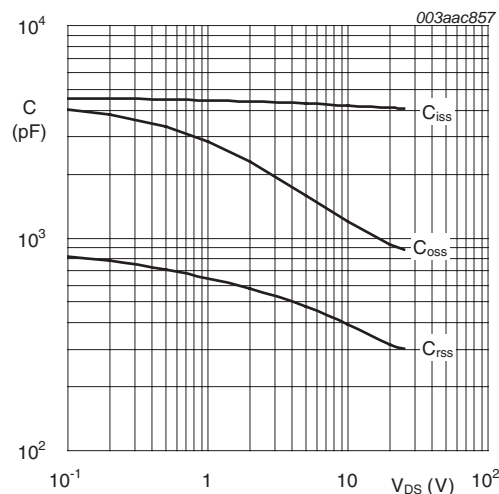


Fig 12. Gate charge waveform definitions



$V_{GS} = 0V; f = 1MHz$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

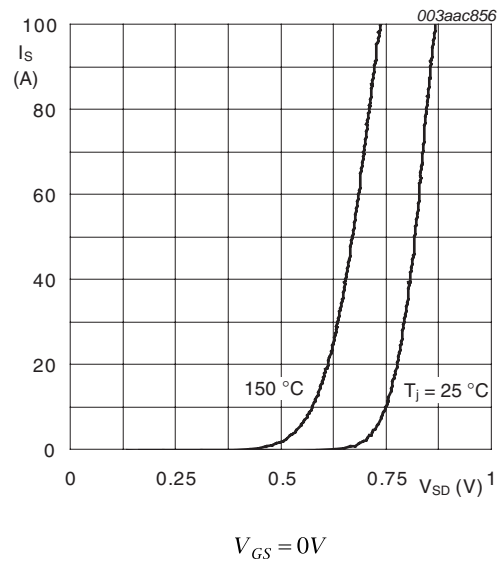


Fig 15. Source current as a function of source drain voltage; typical values.

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

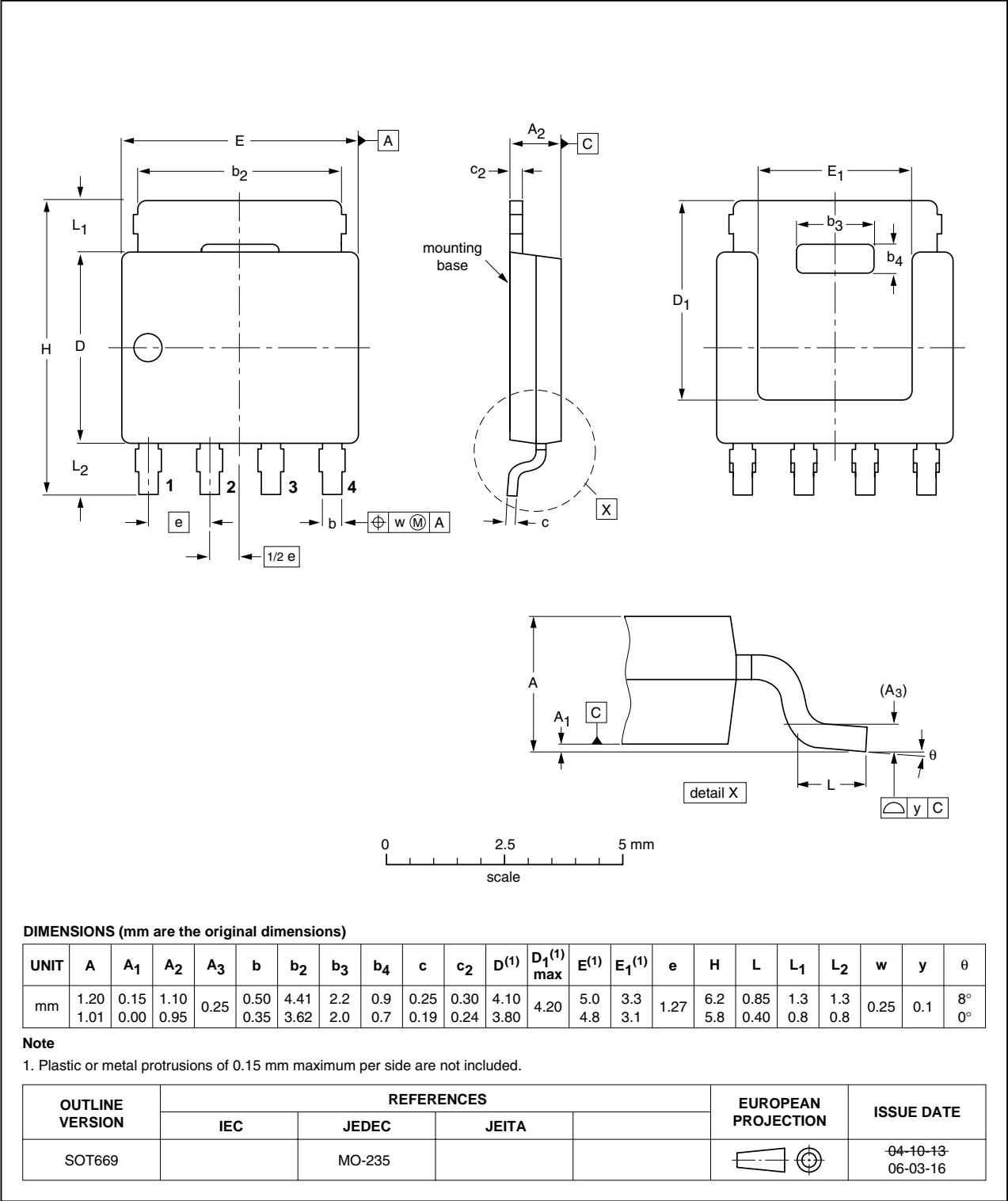


Fig 16. Package outline SOT669 (LPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH1825AL_1	20090422	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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